LM3481-Q1 昇圧、SEPIC、およびフライバック DC/DC コンバータ用、高効率コントローラ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃、T_A
- 10 ピン VSSOP パッケージ
- 1A のピーク電流能力を備えたプッシュプル ドライバを内蔵
- 電流制限とサーマル シャットダウン
- コンデンサと抵抗により周波数補償を最適化
- 内部ソフトスタート
- 電流モード動作
- 調整可能なヒステリシス付き低電圧誤動作防止
- 軽負荷時のパルス スキップ
- 主な仕様
  - 広い電源電圧範囲:2.97V～48V
  - 調整および同期可能なクロック周波数:100kHz～1MHz
  - 内部基準電圧の精度は全温度範囲で ±1.5 パーセント
  - シャットダウン時の消費電流 (全温度範囲):10μA
- WEBENCH Power Designer により、LM3481-Q1 を使用したカスタム設計を作成

2 アプリケーション

- トラクション インバータ および オンボード充電器の絶縁型電源 (フライバック)
- ADAS - 運転者監視
- デジタル コックピット および ヘッド ユニット

3 概要

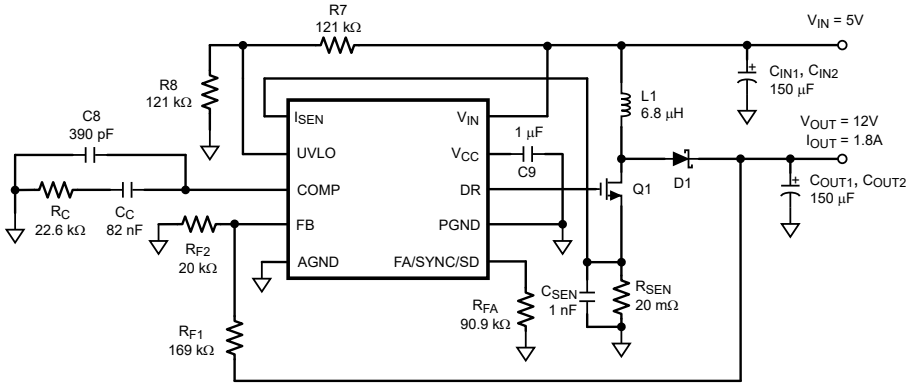
LM3481-Q1 デバイスは、さまざまな用途に使用できる、スイッチング レギュレータ用の高性能なローサイド N-FET コントローラです。このデバイスは、昇圧、SEPIC、フライバックの各コンバータ、およびプライマリ スイッチとしてローサイド FET を必要とするトポロジでの使用向けに設計されています。さらに、LM3481-Q1 デバイスは、非常に高いスイッチング周波数で動作可能なため、ソリューション全体を小型化できます。LM3481-Q1 デバイスのスイッチング周波数は、1 個の外付け抵抗を使用するか、または外部クロックと同期させることにより、100kHz～1MHz の任意の値に調整できます。電流モード制御を使うと、サイクルごとの電流制限が可能になることに加えて、広い帯域幅と優れた過渡応答が得られます。電流制限は、1 個の外付け抵抗で設定できます。

LM3481-Q1 デバイスには、サーマル シャットダウン、短絡保護、過電圧保護などの保護機能が組み込まれています。省電力シャットダウン モードにより、合計消費電流は 5μA に低減され、電源シーケンスを実行できます。内部ソフトスタートにより、スタートアップ時の突入電流が制限されます。内蔵の電流スロープ補償によって、設計が簡素化されています。さらに、特定のアプリケーションで必要な場合は、1 個の抵抗を使用して補償機能を強化できます。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM3481-Q1	VSSOP (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



5V～12V 昇圧コンバータの代表的なアプリケーション

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4 Pin Configuration and Functions

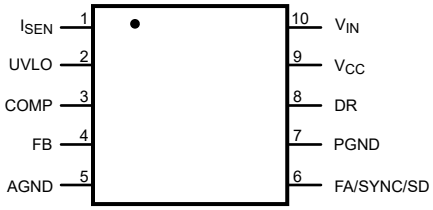

図 4-1. 10-Pin VSSOP Package Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	I_{SEN}	A	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
2	UVLO	A	Under voltage lockout pin. A resistor divider from V_{IN} to ground is connected to the UVLO pin. The ratio of these resistances determine the input voltage which allows switching and the hysteresis to disable switching.
3	COMP	A	Compensation pin. A resistor and capacitor combination connected to this pin provides compensation for the control loop.
4	FB	A	Feedback pin. Inverting input of the error amplifier.
5	AGND	G	Analog ground pin. Internal bias circuitry reference. Should be connected to PGND at a single point.
6	FA/SYNC/SD	I/A	Frequency adjust, synchronization, and shutdown pin. A resistor connected from this pin to ground sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the frequency of the clock. A high level on this pin for ≥ 30 µs will turn the device off and the device will then draw 5 µA from the supply typically.
7	PGND	G	Power ground pin. External power circuitry reference. Should be connected to AGND at a single point.
8	DR	O	Drive pin of the IC. The gate of the external MOSFET should be connected to this pin.
9	V_{CC}	O	Driver supply voltage pin. A bypass capacitor must be connected from this pin to PGND. See *セクション 7.2.1.2.9* section. Do not bias externally.
10	V_{IN}	P	Power supply input pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Pin Voltage	–0.4	50	V
FB	Pin Voltage	–0.4	6	V
FA/SYNC/SD	Pin Voltage	–0.4	6	V
COMP	Pin Voltage	–0.4	6	V
UVLO	Pin Voltage	–0.4	6	V
V_{CC}	Pin Voltage	–0.4	7	V
DR	Pin Voltage	–0.4	7	V
I_{SEN}	Pin Voltage	–400	600	mV
	Peak Driver Output Current		1	A
	Power Dissipation	Internally Limited		
	Junction Temperature		150	°C
Lead Temperature (only applies to operating conditions)	DGS Package		220	°C
Peak Body Temperature (2)			260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. セクション 5.3 indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions, see the セクション 5.5. The ensured specifications apply only for the test conditions.
(2) Part is MSL1-260C qualified

5.2 ESD Ratings: LM3481-Q1

				MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	+2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 5, 6, and 10)	–750	+750	
			Other pins	–750	+750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage	2.97	48	V
Junction Temperature Range	–40	125	°C
Switching Frequency Range	100	1000	kHz

5.4 Thermal Information

THERMAL METRIC (1)		LM3481-Q1 VSSOP 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	83.5	
ψ_{JT}	Junction-to-top characterization parameter	7.5	
ψ_{JB}	Junction-to-board characterization parameter	82.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

V_{IN}= 12 V, R_{FA}= 40 kΩ, T_J = 25°C, unless otherwise indicated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage	V_{COMP} = 1.4 V, 2.97 ≤ V_{IN} ≤ 48 V		1.275		V
		V_{COMP} = 1.4 V, 2.97 ≤ V_{IN} ≤ 48 V, –40°C ≤ T_J ≤ 125°C	1.256		1.294	
ΔV_{LINE}	Feedback Voltage Line Regulation	2.97 ≤ V_{IN} ≤ 48 V		0.003		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{EAO} Source/Sink		±0.5		%/A
$V_{UVLOSEN}$	Undervoltage Lockout Reference Voltage	V_{UVLO} Ramping Down		1.430		V
		V_{UVLO} Ramping Down, –40°C ≤ T_J ≤ 125°C	1.345		1.517	
I_{UVLO}	UVLO Source Current	Enabled		5		µA
		Enabled, –40°C ≤ T_J ≤ 125°C	3		6	
V_{UVLOSD}	UVLO Shutdown Voltage		0.55	0.7	0.82	V
I_{COMP}	COMP pin Current Source	V_{FB} = 0V		640		µA
V_{COMP}		V_{FB} = 1.275V		1.4		V
f_{nom}	Nominal Switching Frequency	R_{FA} = 40 kΩ		475		kHz
		R_{FA} = 40 kΩ, –40°C ≤ T_J ≤ 125°C	406		550	
$V_{sync-HI}$	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization Voltage Rising		1.4		V
$V_{sync-LOW}$	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization Voltage Falling		0.7		V
$R_{DS1\ (ON)}$	Driver Switch On Resistance (top)	I_{DR} = 0.2A, V_{IN}= 5 V		4		Ω
$R_{DS2\ (ON)}$	Driver Switch On Resistance (bottom)	I_{DR} = 0.2A		2		Ω
$V_{DR\ (max)}$	Maximum Drive Voltage Swing(1)	V_{IN} < 6V		V_{IN}		V
		V_{IN} ≥ 6V		6		
D_{max}	Maximum Duty Cycle	R_{FA}=40 kΩ	81	85		%
t_{min} (on)	Minimum On Time			250	363	ns
		worst case over temperature			571	ns
I_{SUPPLY}	Supply Current (switching)	See(2)		3.7		mA
		See(2), –40°C ≤ T_J ≤ 125°C			5.0	
I_Q	Quiescent Current in Shutdown Mode	$V_{FA/SYNC/SD}$ = 3 V(3), V_{IN} = 12 V		9		µA
		$V_{FA/SYNC/SD}$ = 3 V(3), V_{IN} = 12 V, –40°C ≤ T_J ≤ 125°C			15	
		$V_{FA/SYNC/SD}$ = 3 V(3), V_{IN} = 5 V		5		
		$V_{FA/SYNC/SD}$ = 3 V(3), V_{IN} = 5 V, –40°C ≤ T_J ≤ 125°C			10	
V_{SENSE}	Current Sense Threshold Voltage			160		mV
		–40°C ≤ T_J ≤ 125°C	100		190	
V_{SC}	Short Circuit Current Limit Sense Voltage			220		mV
		–40°C ≤ T_J ≤ 125°C	157		275	
V_{SL}	Internal Compensation Ramp Voltage			90		mV
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage)(4)	V_{COMP} = 1.4 V		85		mV
		V_{COMP} = 1.4 V, –40°C ≤ T_J ≤ 125°C	26		135	
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis	V_{COMP} = 1.4 V		70		mV
		V_{COMP} = 1.4 V, –40°C ≤ T_J ≤ 125°C	28		106	
Gm	Error Amplifier Transconductance	V_{COMP} = 1.4 V		450		µS
		V_{COMP} = 1.4 V, –40°C ≤ T_J ≤ 125°C	216		690	
A_{VOL}	Error Amplifier Voltage Gain	V_{COMP} = 1.4 V, I_{EAO} = 100 µA (Source/Sink)		60		V/V
		V_{COMP} = 1.4 V, I_{EAO} = 100 µA (Source/Sink), –40°C ≤ T_J ≤ 125°C	35		66	

V_{IN}= 12 V, R_{FA}= 40 kΩ, T_J = 25°C, unless otherwise indicated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 1.4 V, V_{FB} = 0 V		640		µA
		Source, V_{COMP} = 1.4 V, V_{FB} = 0 V, –40°C ≤ T_J ≤ 125°C	475		837	
		Sink, V_{COMP} = 1.4 V, V_{FB} = 1.4 V		65		µA
		Sink, V_{COMP} = 1.4 V, V_{FB} = 1.4 V, –40°C ≤ T_J ≤ 125°C	31		100	
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit: V_{FB} = 0 V, COMP Pin Floating		2.70		V
		Upper Limit: V_{FB} = 0 V, COMP Pin Floating, –40°C ≤ T_J ≤ 125°C	1.8		2.93	
		Lower Limit: V_{FB} = 1.4 V		0.60		V
		Lower Limit: V_{FB} = 1.4 V, –40°C ≤ T_J ≤ 125°C	0.32		0.90	
t_{SS}	Internal Soft-Start Delay	V_{FB} = 1.2 V, COMP Pin Floating	8.7	15	21.3	ms
t_r	Drive Pin Rise Time	Cgs = 3000 pf, V_{DR} = 0 V to 3 V		25		ns
t_f	Drive Pin Fall Time	Cgs = 3000 pf, V_{DR} = 3 V to 0 V		25		ns
V_{SD}	Shutdown signal threshold(5)FA/SYNC/SD pin	Output = High (Shutdown)		1.31		V
		Output = High (Shutdown), –40°C ≤ T_J ≤ 125°C			1.40	
		Output = Low (Enable)		0.68		V
		Output = Low (Enable), –40°C ≤ T_J ≤ 125°C	0.40			
I_{SD}	Shutdown Pin Current FA/SYNC/SD pin	V_{SD} = 5 V		−1		µA
		V_{SD} = 0 V		20		
T_{SD}	Thermal Shutdown			165		°C
T_{sh}	Thermal Shutdown Hysteresis			10		°C

(1) The drive pin voltage, V_{DR}, is equal to the input voltage when input voltage is less than 6 V. V_{DR} is equal to 6 V when the input voltage is greater than or equal to 6 V.
(2) For this test, the FA/SYNC/SD Pin is pulled to ground using a 40-kΩ resistor.
(3) For this test, the FA/SYNC/SD Pin is pulled to 3 V using a 40-kΩ resistor.
(4) The overvoltage protection is specified with respect to the feedback voltage. This is because the overvoltage protection tracks the feedback voltage. The overvoltage threshold can be calculated by adding the feedback voltage (V_{FB}) to the overvoltage protection specification.
(5) The FA/SYNC/SD pin should be pulled high through a resistor to turn the regulator off. The voltage on the FA/SYNC/SD pin must be above the max limit for the Output = High longer than 30 µs to keep the regulator off and must be below the minimum limit for Output = Low to keep the regulator on.

5.6 Typical Characteristics

Unless otherwise specified, V_{IN} = 12 V, T_J = 25°C.

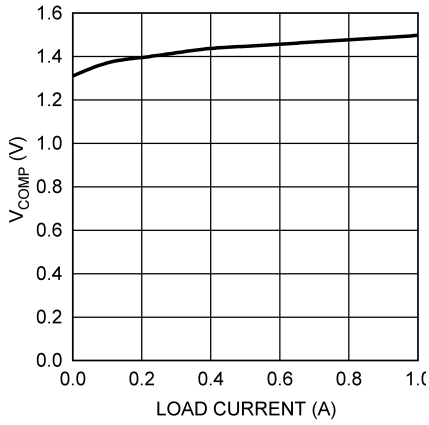

図 5-1. Comp Pin Voltage vs. Load Current

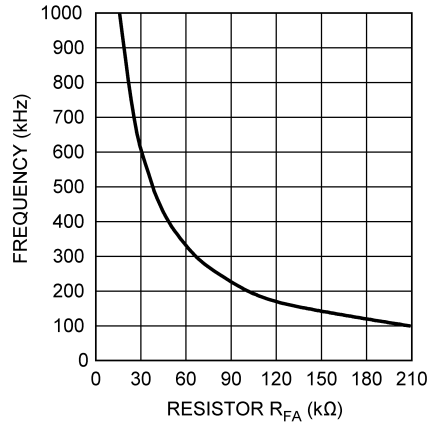

図 5-2. Switching Frequency vs. R_{FA}

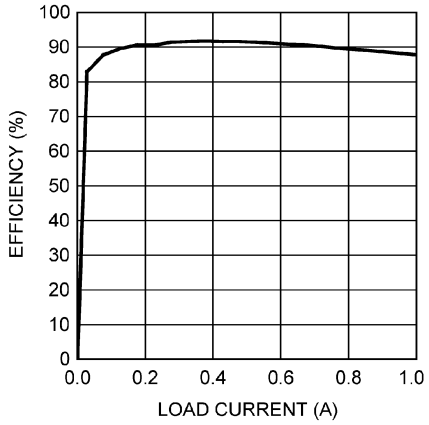

図 5-3. Efficiency vs. Load Current (3.3 V_{IN} and 12 V_{OUT})

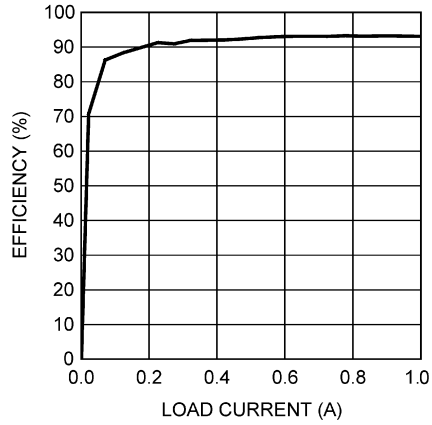

図 5-4. Efficiency vs. Load Current (5 V_{IN} and 12 V_{OUT})

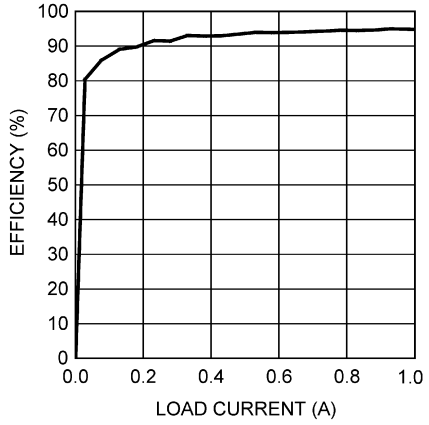

図 5-5. Efficiency vs. Load Current (9 V_{IN} and 12 V_{OUT})

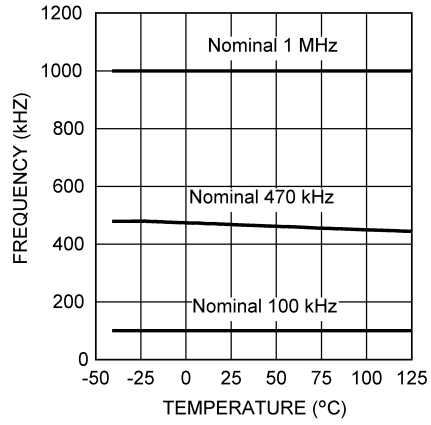

図 5-6. Frequency vs. Temperature

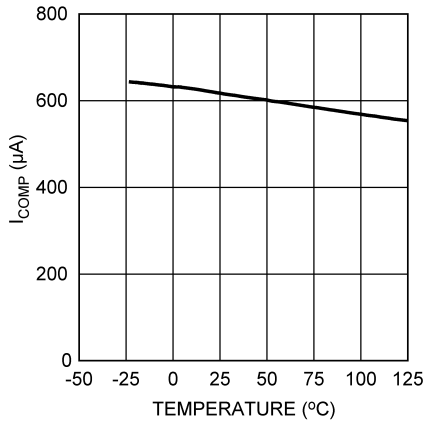

図 5-7. COMP Pin Source Current vs. Temperature

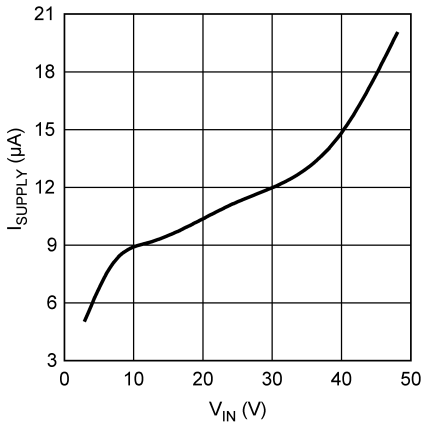

図 5-8. I_{Supply}vs. Input Voltage (Nonswitching)

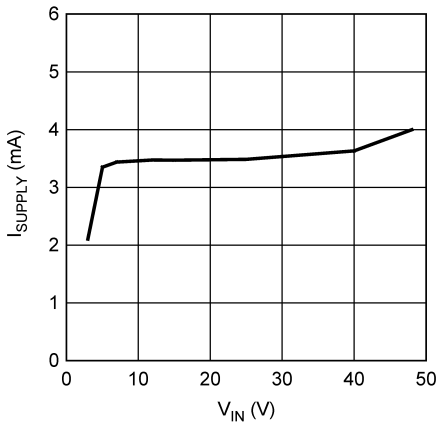

図 5-9. I_{Supply} vs. Input Voltage (Switching)

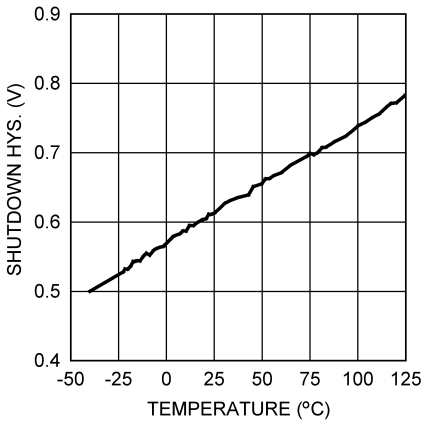

図 5-10. Shutdown Threshold Hysteresis vs. Temperature

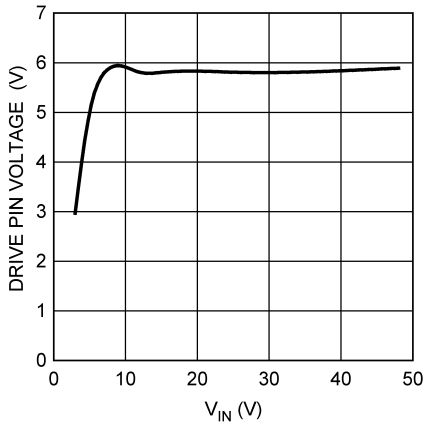

図 5-11. Drive Voltage vs. Input Voltage

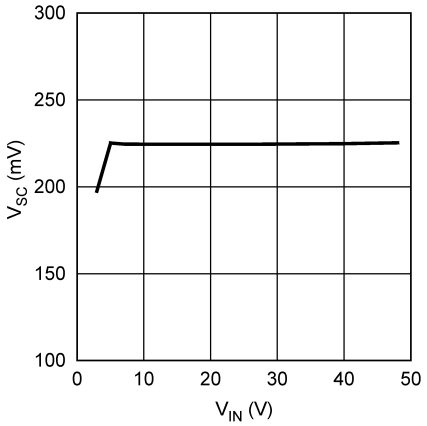

図 5-12. Short Circuit Protection vs. V_{IN}

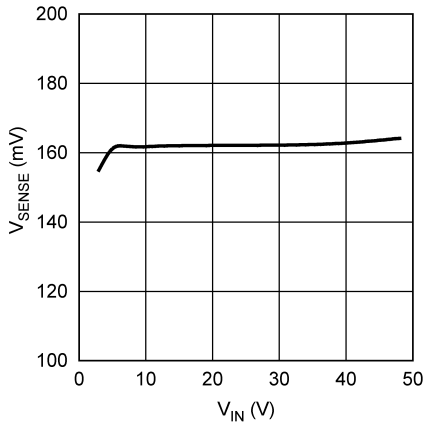

図 5-13. Current Sense Threshold vs. Input Voltage

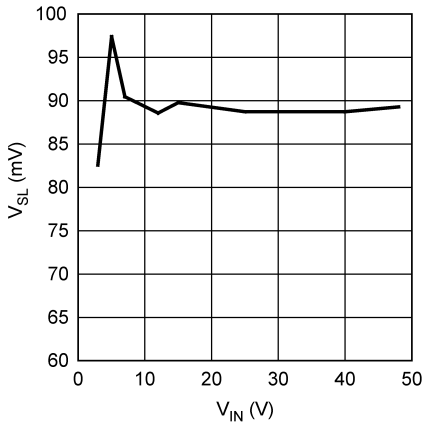

図 5-14. Compensation Ramp Amplitude vs. Input Voltage

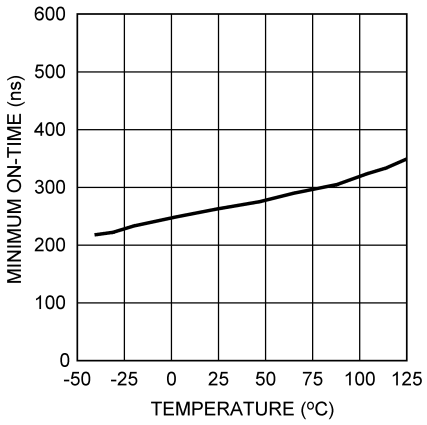

図 5-15. Minimum On-Time vs. Temperature

6 Detailed Description

6.1 Overview

The LM3481-Q1 device uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier (EA) negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets the RS latch using the SET/Blank-out and switch logic blocks. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in 図 6-1. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration, called the blank-out time, is typically 250 ns and is specified as t_{min} (on) in the セクション 5.5 section.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blank-out time is more than what is delivered to the load. An overvoltage comparator inside the LM3481-Q1 prevents the output voltage from rising under these conditions by sensing the feedback (FB pin) voltage and resetting the RS latch. The latch remains in a reset state until the output decays to the nominal value. Thus the operating frequency decreases at light loads, resulting in excellent efficiency.

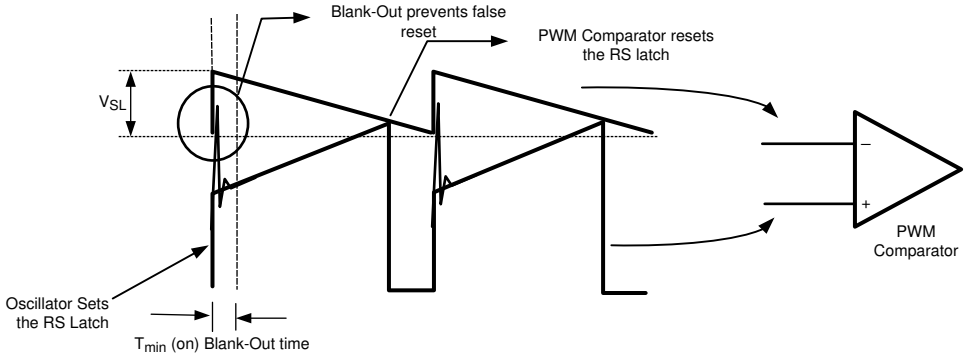

図 6-1. Basic Operation of the PWM Comparator

6.2 Functional Block Diagram

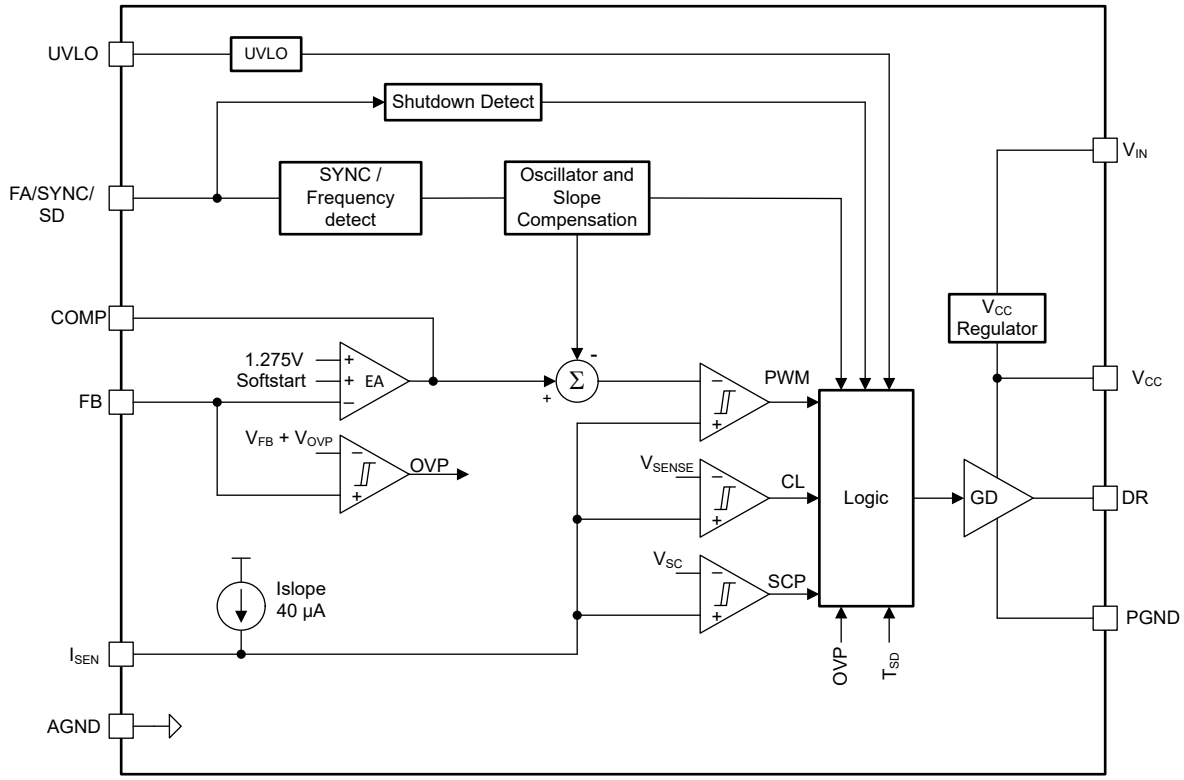

図 6-2. LM3481-Q1 Simplified Functional Block Diagram

6.3 Feature Description

6.3.1 Overvoltage Protection

The LM3481-Q1 has overvoltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at anytime the voltage at the feedback pin rises to V_{FB} + V_{OVP}, OVP is triggered. See the セクション 5.5 section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin (DR) to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3481-Q1 will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See the セクション 5.5 section for limits on $V_{OVP(HYS)}$. The Error Amplifier is operational during OVP events.

6.3.2 Bias Voltage

The internal bias of the LM3481-Q1 comes from either the internal bias voltage generator or directly from the voltage at the VIN pin. At input voltages lower than 6 V the internal IC bias is the input voltage and at voltages above 6 V the internal bias voltage generator of the LM3481-Q1 provides the bias. The gate-driver supply voltage VCC requires an external bypass capacitor (0.47µF to 4.7µF depending on the FET requirements). Do not bias the VCC pin by an external voltage source.

6.3.3 Slope Compensation Ramp

The LM3481-Q1 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is easy to parallel power stages using current mode control because current sharing is automatic. However there is a natural instability that will occur for duty cycles, D, greater than 50% if additional slope compensation is not addressed as described below.

The current mode control scheme samples the inductor current, I_L, and compares the sampled signal, V_{samp}, to a internally generated control signal, V_c. The current sense resistor, R_{SEN}, as shown in the 図 6-3, converts the sampled inductor current, I_L, to the voltage signal, V_{samp}, that is proportional to I_L such that:

$$V_{samp} = I_L \times R_{SEN} \quad (1)$$

The rising and falling slopes, M_1 and $-M_2$ respectively, of V_{samp} are also proportional to the inductor current rising and falling slopes, M_{on} and $-M_{off}$ respectively. Where M_{on} is the inductor slope during the switch on-time and $-M_{off}$ is the inductor slope during the switch off-time and are related to M_1 and $-M_2$ by:

$$M_1 = M_{on} \times R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} \times R_{SEN} \quad (3)$$

For the boost topology:

$$M_{on} = V_{IN} / L \quad (4)$$

$$-M_{off} = (V_{IN} - V_{OUT}) / L \quad (5)$$

$$M_1 = [V_{IN} / L] \times R_{SEN} \quad (6)$$

$$-M_2 = [(V_{IN} - V_{OUT}) / L] \times R_{SEN} \quad (7)$$

$$M_2 = [(V_{OUT} - V_{IN}) / L] \times R_{SEN} \quad (8)$$

Current mode control has an inherent instability for duty cycles greater than 50%, as shown in 図 6-3, where the control signal slope, M_C, equals zero. In 図 6-3, a small increase in the load current causes the sampled signal to increase by ΔV_{samp0}. The effect of this load change, ΔV_{samp1}, at the end of the first switching cycle is :

$$\Delta V_{samp1} = -\left(\frac{M_2}{M_1}\right) \Delta V_{samp0} = -\left(\frac{D}{1-D}\right) \Delta V_{samp0} \quad (9)$$

From 式 9, when D > 0.5, ΔV_{samp1} will be greater than ΔV_{samp0}. In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase. To ensure that the perturbed signal converges we must maintain:

$$\left|-\frac{M_2}{M_1}\right| < 1 \quad (10)$$

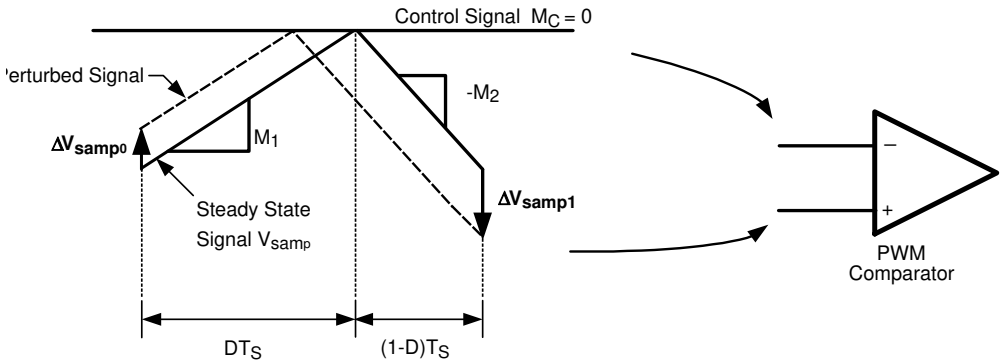

図 6-3. Subharmonic Oscillation for D>0.5

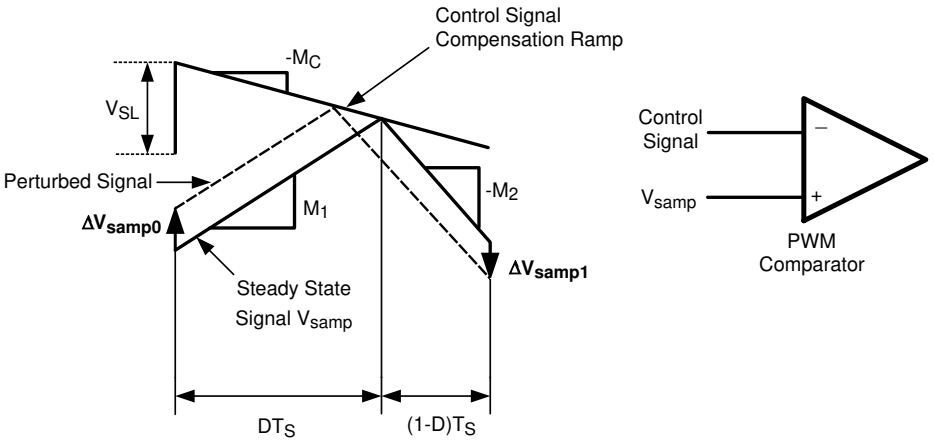

図 6-4. Compensation Ramp Avoids Subharmonic Oscillation

To prevent the subharmonic oscillations, a compensation ramp is added to the control signal, as shown in 図 6-4.

With the compensation ramp, ΔV_{samp1} and the convergence criteria are expressed by,

$$\Delta V_{samp1} = -\left(\frac{M_2 - M_C}{M_1 + M_C}\right)\Delta V_{samp0} \quad (11)$$

$$\left|-\frac{M_2 - M_C}{M_1 + M_C}\right| < 1 \quad (12)$$

The compensation ramp has been added internally in the LM3481-Q1. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$M_C = V_{SL} \times f_S \quad (13)$$

In 式 13, V_{SL} is the amplitude of the internal compensation ramp and f_S is the controller's switching frequency. Limits for V_{SL} have been specified in the セクション 5.5 section.

To provide the user additional flexibility, a patented scheme has been implemented inside the IC to increase the slope of the compensation ramp externally, if the need arises. Adding a single external resistor, R_{SL}(as shown in 図 6-6) increases the amplitude of the compensation ramp as shown in 図 6-5.

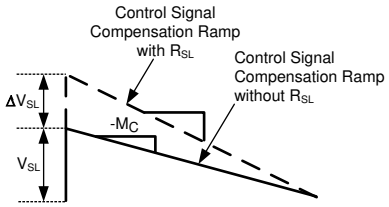

図 6-5. Additional Slope Compensation Added Using External Resistor R_{SL}

Where,

$$\Delta V_{SL} = K \times R_{SL} \quad (14)$$

K = 40 µA typically and changes slightly as the switching frequency changes. 図 6-7 shows the effect the current K has on $\Delta V_{SL}$and different values of R_{SL} as the switching frequency changes.

A more general equation for the slope compensation ramp, M_C, is shown below to include ΔV_{SL} caused by the resistor R_{SL}.

$$M_C = (V_{SL} + \Delta V_{SL}) \times f_S \quad (15)$$

It is good design practice to only add as much slope compensation as needed to avoid subharmonic oscillation. Additional slope compensation minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current.

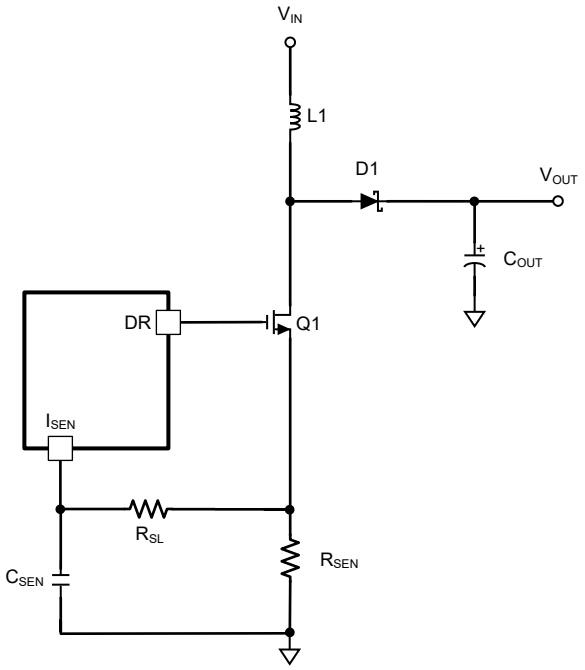

図 6-6. Increasing the Slope of the Compensation Ramp

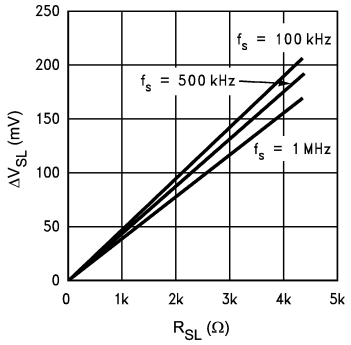

図 6-7. ΔV_{SL} vs R_{SL}

6.3.4 Frequency Adjust, Synchronization, and Shutdown

The switching frequency of the LM3481-Q1 can be adjusted between 100 kHz and 1 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground, as shown in 図 6-8. Refer to the セクション 5.6 to determine the value of the resistor required for a desired switching frequency.

式 16 can also be used to estimate the frequency adjust resistor.

Where f_S is in kHz and R_{FA} in kΩ.

$$R_{FA} = \frac{22 \times 10^3}{f_S} - 5.74 \quad (16)$$

The LM3481-Q1 can be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in 図 6-9. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

It is recommended to have the width of the synchronization pulse wider than the duty cycle of the converter and to have the synchronization pulse width ≥ 300 ns.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (refer to the セクション 5.5 section for definition of high signal) appears on the FA/SYNC/SD pin, the LM3481-Q1 stops switching and goes into a low current mode. The total supply current of the device reduces to 5 µA, typically, under these conditions.

図 6-10 and 図 6-11 show an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode, respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30 µs shuts down the device.

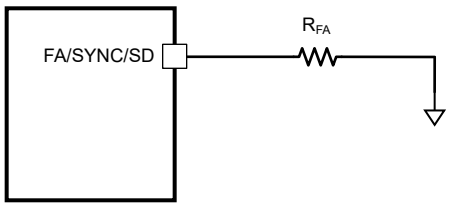

図 6-8. Frequency Adjust

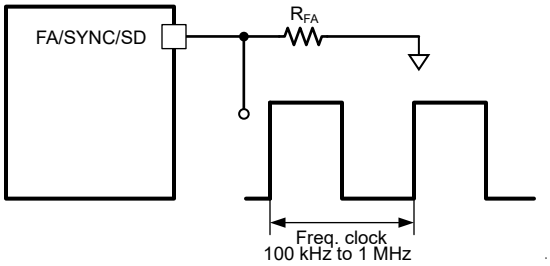

図 6-9. Frequency Synchronization

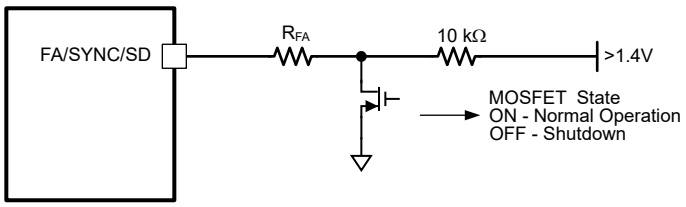

図 6-10. Shutdown Operation in Frequency Adjust Mode

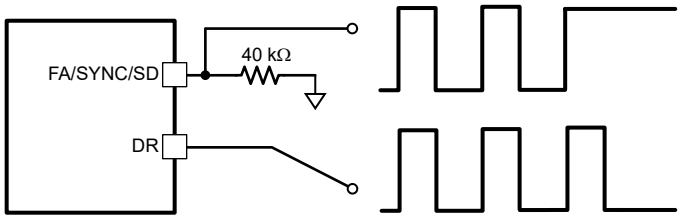

図 6-11. Shutdown Operation in Synchronization Mode

6.3.5 Undervoltage Lockout (UVLO) Pin

The UVLO pin provides user programmable enable and shutdown thresholds. The UVLO pin is compared to an internal reference of 1.43 V (typical), and a resistor divider programs the enable threshold, V_{EN}. When the IC is enabled, a 5-µA current is sourced out of the UVLO pin, which effectively causes a hysteresis, and the UVLO shutdown threshold, V_{SH}, is now lower than the enable threshold. Setting these thresholds requires two resistors connected from the V_{IN} pin to the UVLO pin and from the UVLO pin to GND (see 図 6-12). Select the desired enable, V_{EN}, and UVLO shutdown, V_{SH}, threshold voltages and use the 式 17 and 式 18 to determine the resistance values:

$$R8 = \frac{1.43V}{I_{UVLO}} \times \left(1 + \frac{1.43V - V_{SH}}{V_{EN} - 1.43V}\right) \quad (17)$$

$$R7 = R8 \times \left(\frac{V_{EN}}{1.43V} - 1\right) \quad (18)$$

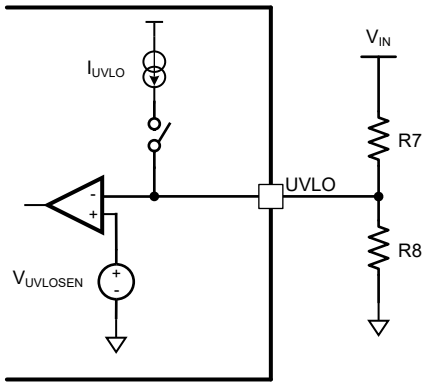

図 6-12. UVLO Pin Resistor Divider

If the system is designed to work over wide input voltages, the voltage at the UVLO pin could exceed the voltage limit for the UVLO pin. In this case a zener diode can be connected between the UVLO pin and ground to prevent the UVLO voltage from rising above the maximum value.

If the UVLO pin function is not desired, select R8 and R7 of equal magnitude greater than 100 kΩ. This will allow V_{IN} to be in control of the UVLO thresholds. The UVLO pin may also be used to implement the enable/disable function. If a signal pulls the UVLO pin below the 1.43 V (typical) threshold, the converter will be disabled.

6.3.6 Short-Circuit Protection

When the voltage across the sense resistor (measured on the I_{SEN} Pin) exceeds 220 mV, short-circuit current limit gets activated. A comparator inside the LM3481-Q1 reduces the switching frequency by a factor of 8 and maintains this condition until the short is removed.

6.4 Device Functional Modes

The device is set to run as soon as the input voltage crosses above the UVLO set point and at a frequency set according to the FA/SYNC/SD pin pull-down resistor or to run at a frequency set by the waveform applied to the FA/SYNC/SD pin.

If the FA/SYNC/SD pin is pulled high, the LM3481-Q1 enters shut-down mode.

7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LM3481-Q1 may be operated in either continuous or discontinuous conduction mode. The following applications are designed for continuous conduction operation. This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

7.2 Typical Applications

7.2.1 Boost Converter

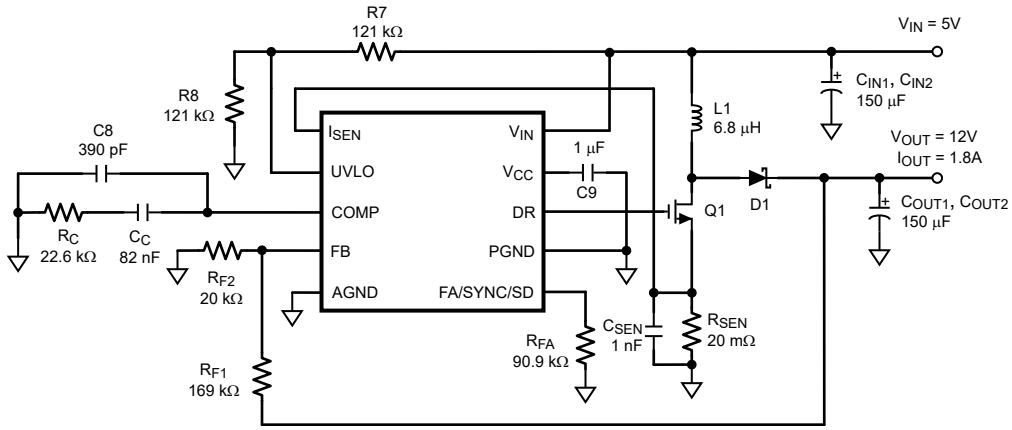


図 7-1. Typical High Efficiency Step-Up (Boost) Converter using LM3481-Q1

The most common topology for the LM3481-Q1 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in 図 7-2. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitor, C_{OUT}.

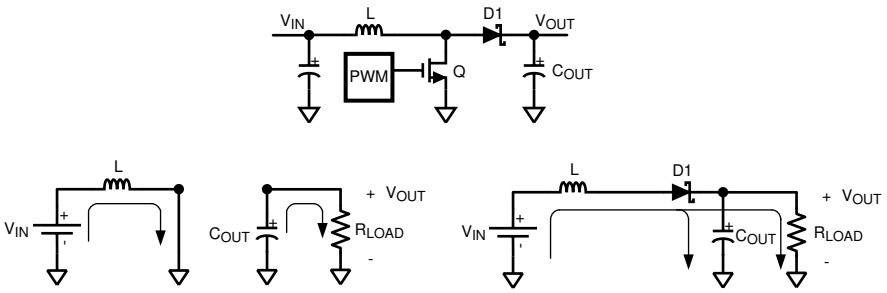
In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1\text{-}D} \tag{19}$$

(ignoring the voltage drop across the MOSFET and the diode), or

$$V_{OUT} + V_{D1} - V_Q = \frac{V_{IN} - V_Q}{1\text{-}D} \tag{20}$$

where D is the duty cycle of the switch, V_{D1} is the forward voltage drop of the diode, and V_Q is the drop across the MOSFET when it is on. The following sections describe selection of components for a boost converter.



A. First Cycle of Operation
B. Second Cycle of Operation

図 7-2. Simplified Boost Converter Diagram

7.2.1.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: Input voltage range, output voltage, output current range and required switching frequency. These four main parameters will affect the choices of component available to achieve a proper system behavior.

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM3481-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

7.2.1.2.2 Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter. 図 7-3 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified as:

$$V_L(t) = L \frac{di_L(t)}{dt} \quad (21)$$

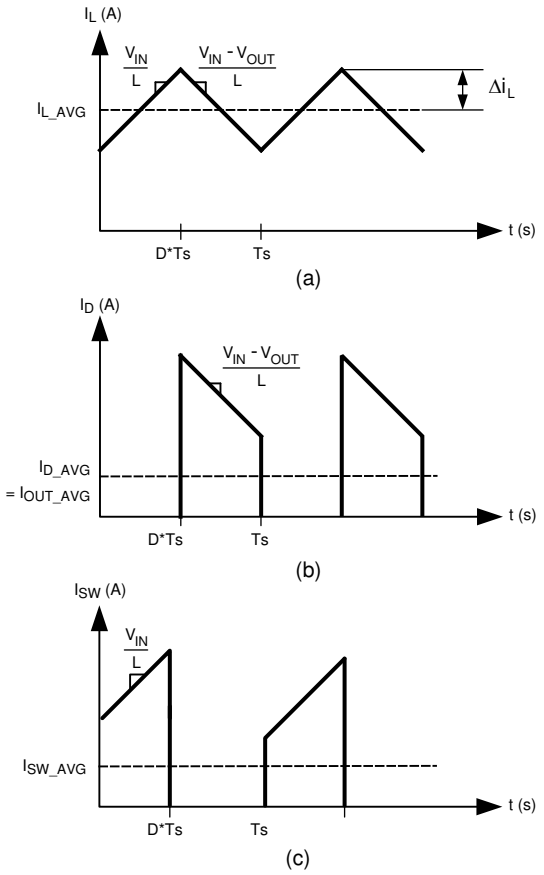


図 7-3. (a) Inductor Current (b) Diode Current (c) Switch Current

If $V_L(t)$ is constant, $di_L(t)/dt$ must be constant. Hence, for a given input voltage and output voltage, the current in the inductor changes at a constant rate.

The important quantities in determining a proper inductance value are I_L (the average inductor current) and Δi_L (the inductor current ripple difference between the peak inductor current and the average inductor current). If Δi_L is larger than I_L, the inductor current drops to zero for a portion of the cycle and the converter operates in discontinuous conduction mode. If Δi_L is smaller than I_L, the inductor current stays above zero and the converter operates in continuous conduction mode. All the analysis in this data sheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the following conditions must be met:

$$I_L > \Delta i_L \tag{22}$$

$$\frac{I_{OUT}}{1-D} > \frac{DV_{IN}}{2f_S L} \tag{23}$$

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S} \tag{24}$$

Choose the minimum I_{OUT} to determine the minimum L. A common choice is to set (2 x Δi_L) to 30% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter,

$$I_L = \frac{I_{OUT}}{1-D} \tag{25}$$

$$I_{L\_peak} = I_L(max) + \Delta i_L(max) \quad (26)$$

$$\Delta i_L = \frac{DV_{IN}}{2Lf_S} \quad (27)$$

A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency.

The LM3481-Q1 can be set to switch at very high frequencies. When the switching frequency is high, the converter can operate with very small inductor values. With a small inductor value, the peak inductor current can be extremely higher than the output currents, especially under light load conditions.

The LM3481-Q1 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated above.

7.2.1.2.3 Programming the Output Voltage and Output Current

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in 図 7-4. The resistors are selected such that the voltage at the feedback pin is 1.275 V. R_{F1} and R_{F2} can be selected using the equation,

$$V_{OUT} = 1.275\ (1 + \frac{R_{F1}}{R_{F2}}) \quad (28)$$

A 100-pF capacitor may be connected between the feedback and ground pins to reduce noise.

The maximum amount of current that can be delivered at the output can be controlled by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. Limits for V_{SENSE} have been specified in the セクション 5.5 section. This can be expressed as:

$$I_{sw(peak)} \times R_{SEN} = V_{SENSE} - D \times V_{SL} \quad (29)$$

The peak current through the switch is equal to the peak inductor current.

$$I_{sw(peak)} = I_L(max) + \Delta i_L \quad (30)$$

Therefore for a boost converter,

$$I_{sw(peak)} = \frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)} \quad (31)$$

Combining the two equations yields an expression for R_{SEN},

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{\left[\frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}\right]} \quad (32)$$

Evaluate R_{SEN} at the maximum and minimum V_{IN} values and choose the smallest R_{SEN} calculated.

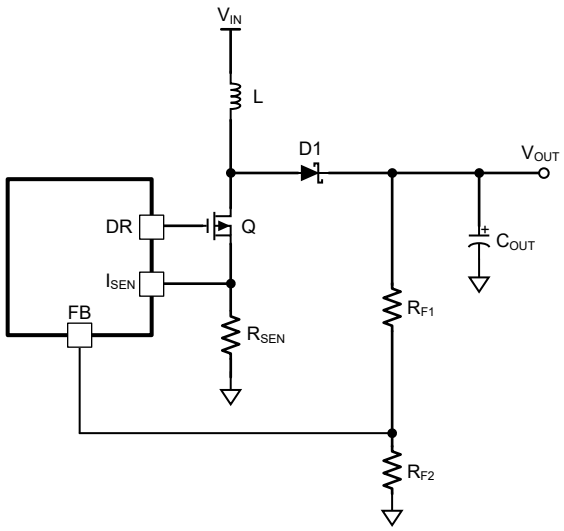


図 7-4. Adjusting the Output Voltage

7.2.1.2.4 Current Limit With Additional Slope Compensation

If an external slope compensation resistor is used (see 図 6-6) the internal control signal will be modified and this will have an effect on the current limit.

If R_{SL} is used, then this will add to the existing slope compensation. The command voltage, V_{CS}, will then be given by:

$$V_{CS} = V_{SENSE} - D \times (V_{SL} + \Delta V_{SL}) \quad (33)$$

Where V_{SENSE} is a defined parameter in the セクション 5.5 section and ΔV_{SL} is the additional slope compensation generated as discussed in the セクション 6.3.3 section. This changes the equation for R_{SEN} to:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{\frac{I_{OUT(max)}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}} \quad (34)$$

Note that because $\Delta V_{SL} = R_{SL} \times K$ as defined earlier, R_{SL}can be used to provide an additional method for setting the current limit. In some designs R_{SL} can also be used to help filter noise to keep the I_{SEN} pin quiet.

7.2.1.2.5 Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than the inductor peak current. The peak diode current can be calculated using the formula:

$$I_{D(Peak)} = [I_{OUT} / (1-D)] + \Delta i_L \quad (35)$$

In 式 35, I_{OUT} is the output current and Δi_L has been defined in 図 7-3.

The peak reverse voltage for a boost converter is equal to the regulator output voltage. The diode must be capable of handling this peak reverse voltage. To improve efficiency, a low forward drop Schottky diode is recommended.

7.2.1.2.6 Power MOSFET Selection

The drive pin, DR, of the LM3481-Q1 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected

to the ground. The drive pin voltage, V_{DR}, depends on the input voltage (see セクション 5.6). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub-logic level MOSFET should be used.

The selected MOSFET directly controls the efficiency. The critical parameters for selection of a MOSFET are:

- Minimum threshold voltage, $V_{TH(MIN)}$
- On-resistance, $R_{DS(ON)}$
- Total gate charge, Q_g
- Reverse transfer capacitance, C_{RSS}
- Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and ac switching or transition losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND}, is the I^2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND(MAX)} = \left(\frac{I_{OUT(max)}}{1 - D_{MAX}}\right)^2 D_{MAX} R_{DS(ON)} \tag{36}$$

where D_{MAX} is the maximum duty cycle.

$$D_{MAX} = \left(1 - \frac{V_{IN(MIN)}}{V_{OUT}}\right) \tag{37}$$

At high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often, the individual MOSFET datasheet does not give enough information to yield a useful result. 式 38 and 式 39 give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{Lmax} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL}) \tag{38}$$

$$t_{LH} = \left(Qgd + \frac{Qgs}{2}\right) \times \frac{R_{Gate}}{V_{DR} - Vgs_{th}} \tag{39}$$

7.2.1.2.7 Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular, as shown in 図 7-3. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \left(\frac{(V_{OUT} - V_{IN})V_{IN}}{\sqrt{12}\, V_{OUT} L f_S}\right) \tag{40}$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 100 µF to 200 µF. If a value lower than 100 µF is used, then problems with impedance interactions or switching noise can affect the LM3481-Q1 . To improve performance, especially with V_{IN} below 8 V, it is recommended to use a 20Ω resistor at the input to provide a RC filter. This resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see 図 7-5). A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

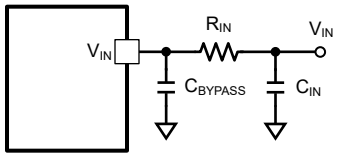


図 7-5. Reducing IC Input Noise

7.2.1.2.8 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum rms current. The rms current in the output capacitor is:

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2 \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]} \quad (41)$$

Where

$$\Delta i_L = \frac{DV_{IN}}{2Lf_S} \quad (42)$$

and D, the duty cycle is equal to $(V_{OUT} - V_{IN})/V_{OUT}$.

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output.

7.2.1.2.9 Driver Supply Capacitor Selection

A good quality ceramic bypass capacitor must be connected from the V_{CC} pin to the PGND pin for proper operation. This capacitor supplies the transient current required by the internal MOSFET driver, as well as filtering the internal supply voltage for the controller. A value of between 0.47 µF and 4.7 µF is recommended.

7.2.1.2.10 Compensation

For detailed explanation on how to select the right compensation components to attach to the compensation pin for a boost topology please see *AN-1286 Compensation for the LM3478 Boost Controller* (SNVA067). When calculating the Error Amplifier DC gain, A_{EA}, R_{OUT} = 152 kΩ for the LM3481-Q1 .

7.2.1.3 Application Curve

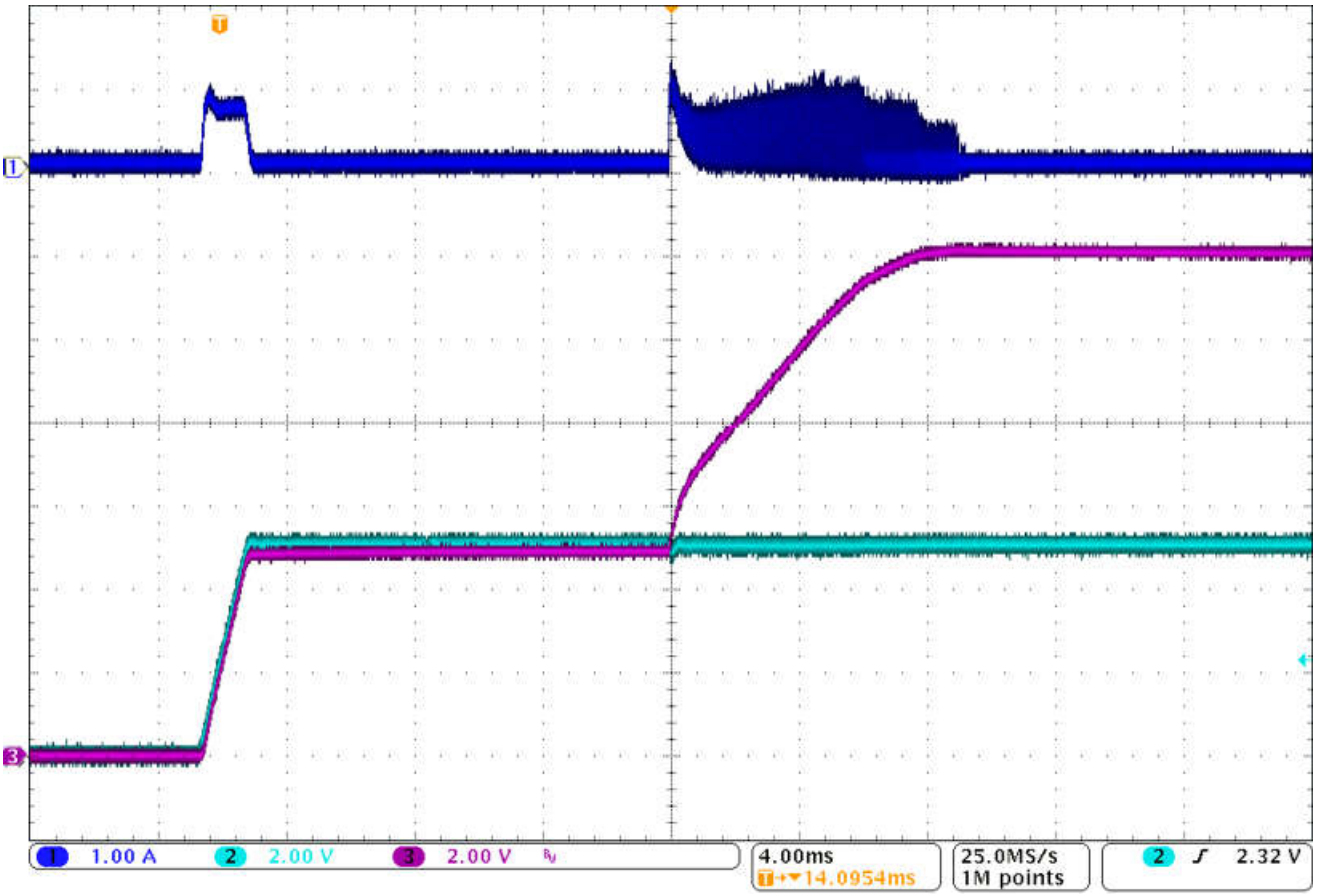


図 7-6. Start-Up Pattern for a 5-Vin, 12-Vout Boost Converter Using LM3481 Boost Evaluation Module (C1: Inductor Current, C2: Vin, C3:Vout)

7.2.2 Typical SEPIC Converter

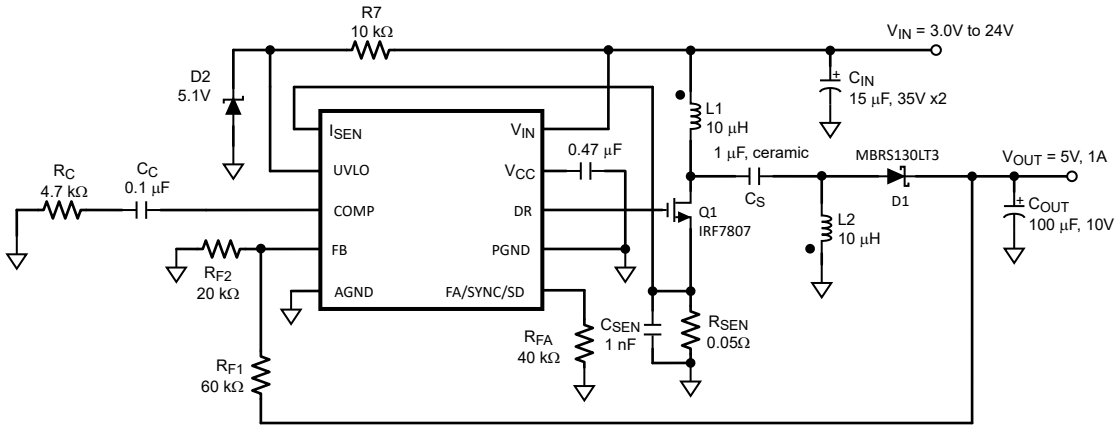


図 7-7. Typical SEPIC Converter using LM3481-Q1

Because the LM3481-Q1 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of SEPIC using the LM3481-Q1 is shown in 図 7-7. As shown in 図 7-7, the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors

to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled transformer because equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom transformer. The input ripple can be reduced along with size by using the coupled windings of transformer for L1 and L2.

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of SEPIC over a boost converter is the inherent input to output isolation. The capacitor C_S isolates the input from the output and provides protection against shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given by:

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \quad (43)$$

In 式 43, V_Q is the on-state voltage of the MOSFET, Q1, and V_{DIODE} is the forward voltage drop of the diode.

7.2.2.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: Input voltage range, output voltage, output current range and required switching frequency. These four main parameters will affect the choices of component available to achieve a proper system behavior.

7.2.2.2 Detailed Design Procedure

7.2.2.2.1 Power MOSFET Selection

As in a boost converter, the parameters governing the selection of the MOSFET are the minimum threshold voltage, $V_{TH(MIN)}$, the on-resistance, $R_{DS(ON)}$, the total gate charge, Q_g, the reverse transfer capacitance, C_{RSS}, and the maximum drain to source voltage, $V_{DS(MAX)}$. The peak switch voltage in a SEPIC is given by:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE} \quad (44)$$

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)} \quad (45)$$

The peak switch current is given by:

$$I_{SWPEAK} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2} \quad (46)$$

Where ΔI_{L1} and ΔI_{L2} are the peak-to-peak inductor ripple currents of inductors L1 and L2 respectively.

The rms current through the switch is given by:

$$I_{SWRMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right] D} \quad (47)$$

7.2.2.2.2 Power Diode Selection

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN} + V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

7.2.2.2.3 Selection of Inductors L1 and L2

Proper selection of the inductors L1 and L2 to maintain constant current mode requires calculations of the following parameters.

Average current in the inductors:

$$I_{L1AVE} = \frac{DI_{OUT}}{1-D} \quad (48)$$

$$I_{L2AVE} = I_{OUT} \quad (49)$$

Peak-to-peak ripple current, to calculate core loss if necessary:

$$\Delta I_{L1} = \frac{(V_{IN} - V_O)\, D}{(L1) f_S} \quad (50)$$

$$\Delta I_{L2} = \frac{(V_{IN} - V_O)\, D}{(L2) f_S} \quad (51)$$

Maintaining the condition $I_L > \Delta I_L/2$ to ensure continuous conduction mode yields the following minimum values for L1 and L2:

$$L1 > \frac{(V_{IN} - V_O)(1-D)}{2 I_{OUT} f_S} \quad (52)$$

$$L2 > \frac{(V_{IN} - V_O) D}{2 I_{OUT} f_S} \quad (53)$$

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1PK} = \frac{DI_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2} \quad (54)$$

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2} \quad (55)$$

I_{L1PK} must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended value to reduce input ripple and output ripple. However, once ΔI_{L1} is less than 20% of I_{L1AVE}, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommendation, ΔI_{L2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \text{ESR} \quad (56)$$

where ESR is the effective series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then L1 = L2 = L. All the equations above will hold true if the inductance is replaced by 2L.

7.2.2.2.4 Sense Resistor Selection

The peak current through the switch, I_{SWPEAK}, can be adjusted using the current sense resistor, R_{SEN}, to provide a certain output current. Resistor R_{SEN} can be selected using the formula:

$$R_{SEN} = \frac{V_{SENSE} - D \times (V_{SL} + \Delta V_{SL})}{I_{SWPEAK}} \quad (57)$$

7.2.2.2.5 SEPIC Capacitor Selection

The selection of SEPIC capacitor, C_S, depends on the rms current. The rms current of the SEPIC capacitor is given by:

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + \left(I_{L1PK}^2 - I_{L1PK}\Delta I_{L1} + \Delta I_{L1}^2\right)(1-D)} \quad (58)$$

The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the rms current through the capacitor is small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. Tantalum capacitors are the best choice for SMT, having high rms current ratings relative to size. Ceramic capacitors could be used, but the low C values will tend to cause larger changes in voltage across the capacitor due to the large currents, and high C value ceramics are expensive. Electrolytic capacitors work well for through hole applications where the size required to meet the rms current rating can be accommodated. There is an energy balance between C_S and L1, which can be used to determine the value of the capacitor. The basic energy balance equation is:

$$\frac{1}{2} C_S \Delta V_S^2 = \frac{1}{2} (L1) \Delta I_{L1}^2 \quad (59)$$

Where

$$\Delta V_S = \left(\frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}\right) \frac{I_{OUT}}{f_S C_S} \quad (60)$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{(L1) f_S} \quad (61)$$

is the ripple current through the inductor L1. The energy balance equation can be solved to provide a minimum value for C_S:

$$C_S \geq L1 \frac{I_{OUT}^2}{(V_{IN} - V_Q)^2} \quad (62)$$

7.2.2.2.6 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta I_{L1} / \sqrt{12} = \frac{D}{2\sqrt{3}} \left(\frac{V_{IN} - V_Q}{(L1) f_S}\right) \quad (63)$$

The input capacitor should be capable of handling the rms current. Although the input capacitor is not as critical in a SEPIC application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 100 µF to 200 µF. If a value lower than 100 µF is used, then problems with impedance interactions or switching noise can affect the LM3481-Q1. To improve performance, especially with V_{IN} below 8 V, it is recommended to use a 20Ω resistor at the input to provide a RC filter. This resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see 図 7-5). A 0.1 µF or 1 µF ceramic

capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

7.2.2.2.7 Output Capacitor Selection

The output capacitor of the SEPIC sees very large ripple currents similar to the output capacitor of a boost converter. The rms current through the output capacitor is given by:

$$I_{RMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right](1\text{-}D) - I_{OUT}^2} \quad (64)$$

The ESR and ESL of the output capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo- OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

7.2.2.3 Application Curve

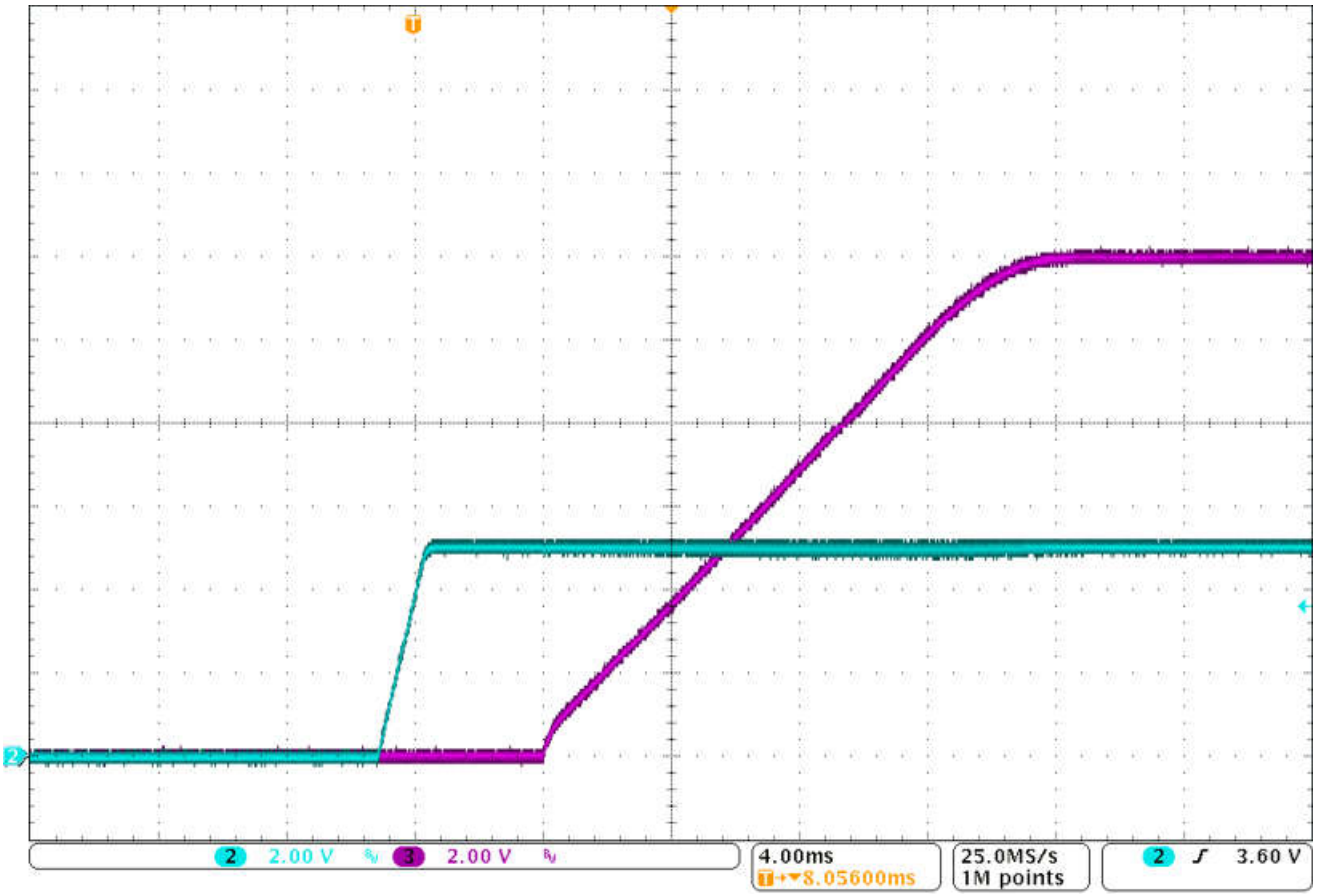


図 7-8. Start-Up Pattern for a 5-Vin, 12-Vout SEPIC Converter on LM3481 SEPIC Evaluation Module (C2: Vin, C3:Vout)

7.3 Power Supply Recommendations

The LM3481-Q1 is designed to operate from various DC power supply including a car battery. If so, VIN input should be protected from reversal voltage and voltage dump over 48 Volts. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input

supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

Good board layout is critical for switching controllers such as the LM3481-Q1. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted Ldi/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. Although the LM3481-Q1 has 250ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time.

The most important layout rule is to keep the AC current loops as small as possible. 図 7-9 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. These currents are the most critical currents because current is changing in very short time periods. The dotted lined traces of the bottom schematic are the once to make as short as possible.

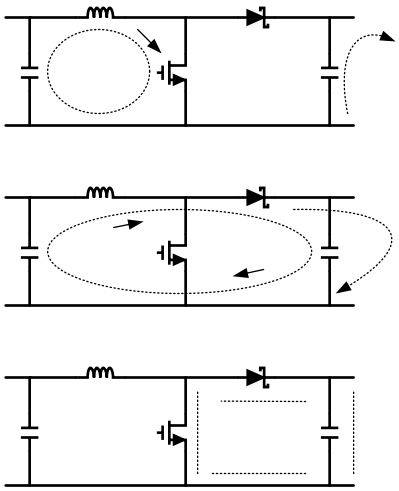


図 7-9. Current Flow in a Boost Application

The PGND and AGND pins have to be connected to the same ground very close to the device. To avoid ground loop currents attach all the grounds of the system only at one point.

A ceramic input capacitor should be connected as close as possible to the Vin pin and grounded close to the GND pin.

For a layout example please see AN-2094 LM3481 SEPIC Evaluation Board. For more information about layout in switch mode power supplies refer to AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines.

7.4.2 Layout Example

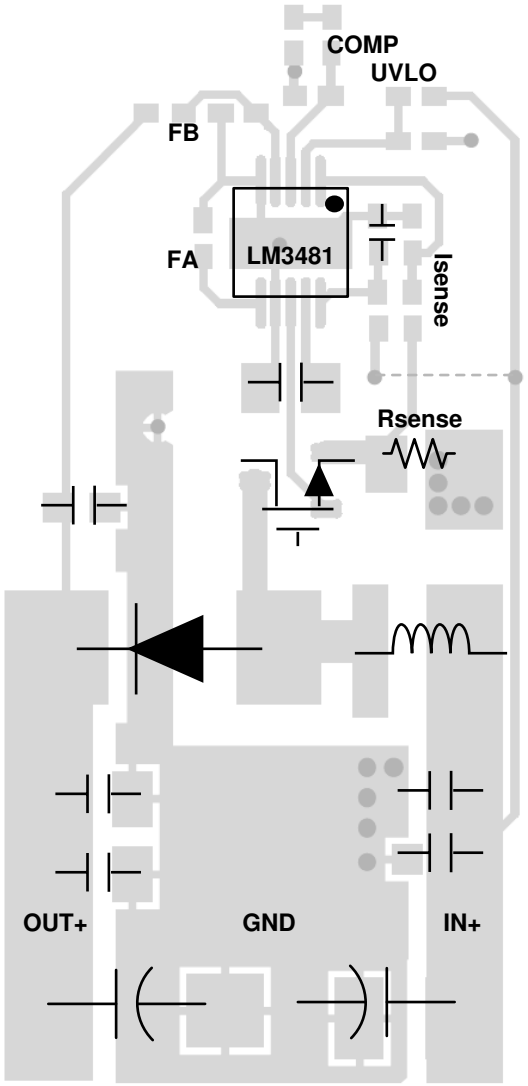


図 7-10. Typical Layout for a Boost Converter

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the LM3481-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT} and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

8.1.2 Related Documentation

- *Documentation Overview*
- *AN-1286 Compensation for the LM3478 Boost Controller*
- *AN-2094 LM3481 SEPIC Evaluation Board*
- *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines*
- *330mW AC or DC Tiny Flyback Converter Power Supply*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

8.4 Trademarks

WEBENCH® is a registered trademark of Texas Instruments.
SIMPLE SWITCHER® is a registered trademark of Ti.
すべての商標は、それぞれの所有者に帰属します。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2024) to Revision B (December 2024)	Page
• Updated thermal information	4

Changes from Revision * (November 2023) to Revision A (October 2024)	Page
• LM3481_SNVS346G データシートから LM348-Q1_SNVSCL9 を削除	1
• Updated Absolute Maximum Ratings	4
• Updated parameter value of V_{COMP} and V_{EAO}, updated parameter description of $I_{COMP}$and V_{SC}, updated test condition of I_{EAO}	5
• Simplified Functional Block Diagram	11
• Updated 図 6-10 and 図 6-11	14

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3481QMM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SUAB
LM3481QMM/NOPB.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUAB
LM3481QMMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	SUAB
LM3481QMMX/NOPB.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	SUAB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF LM3481-Q1 :

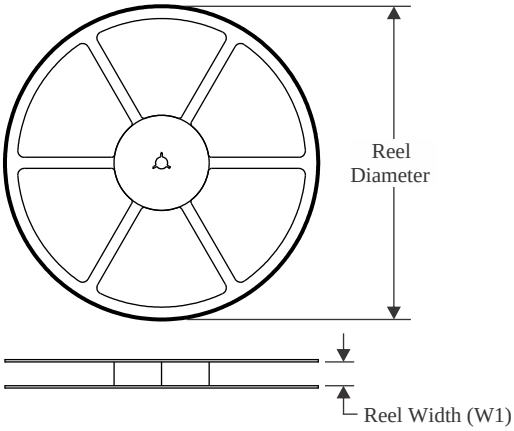
- Catalog : LM3481

NOTE: Qualified Version Definitions:

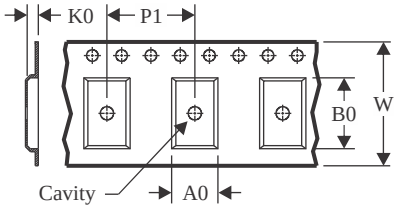
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

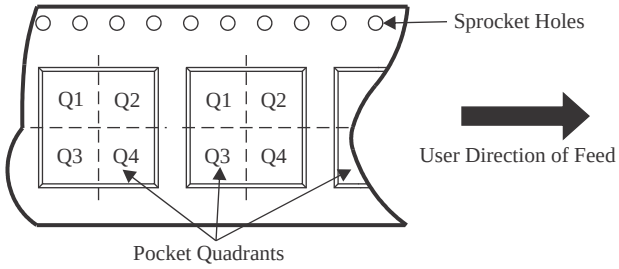


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

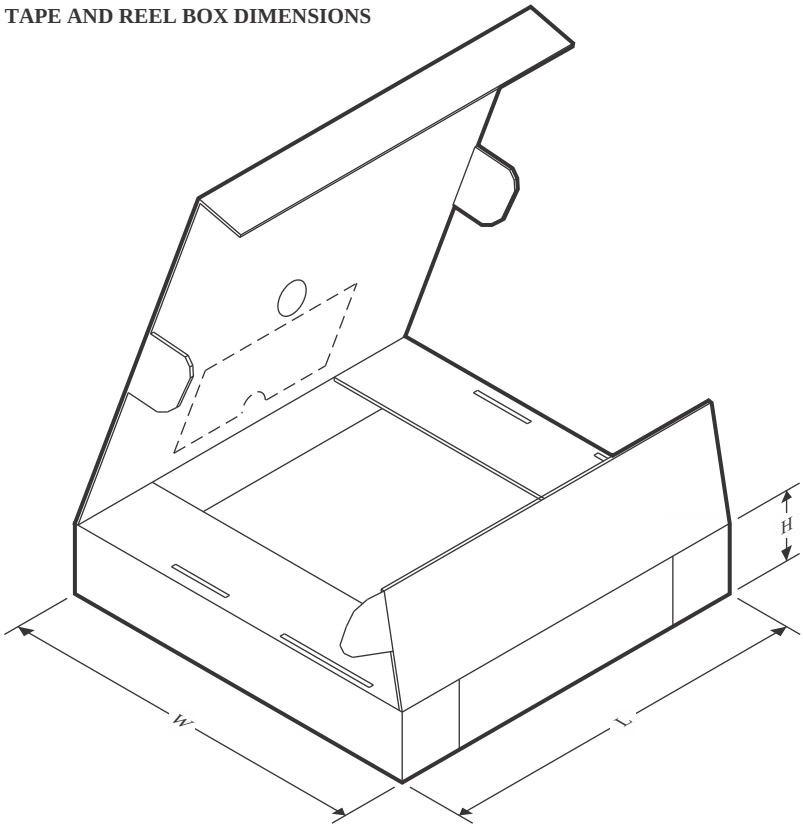
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3481QMM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3481QMMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

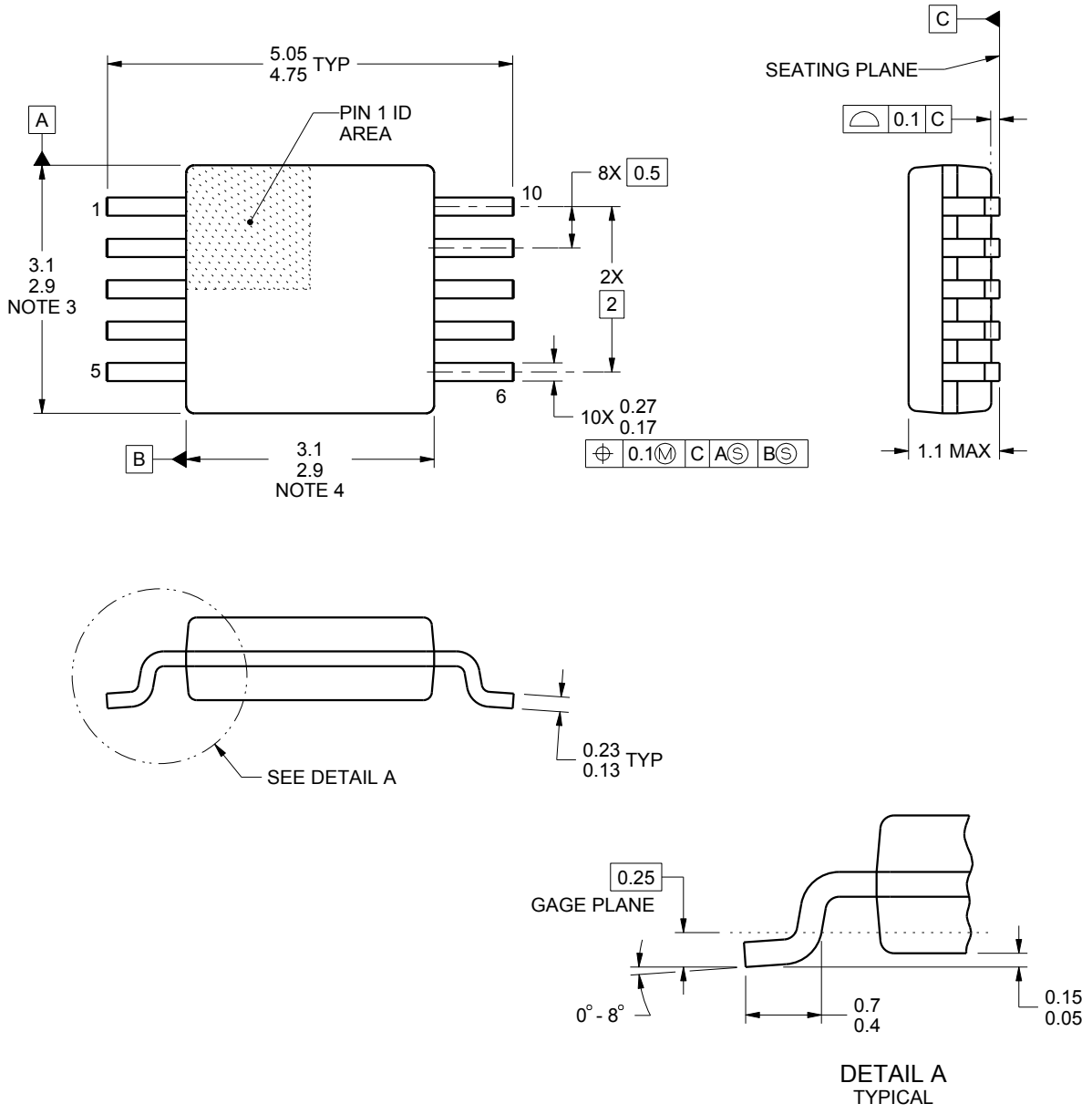
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3481QMM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LM3481QMMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

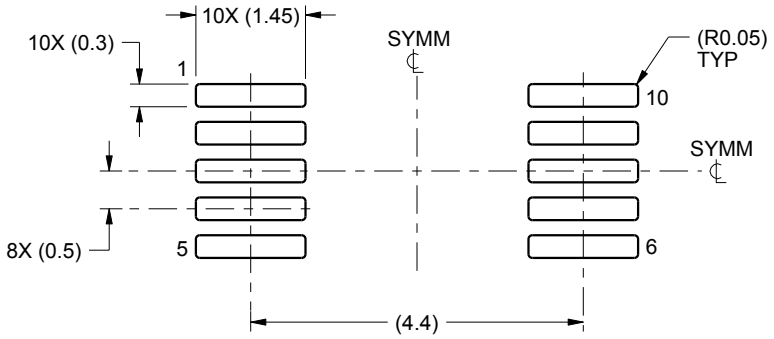
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

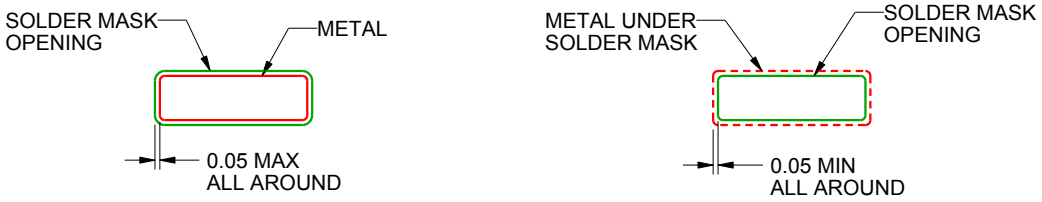


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

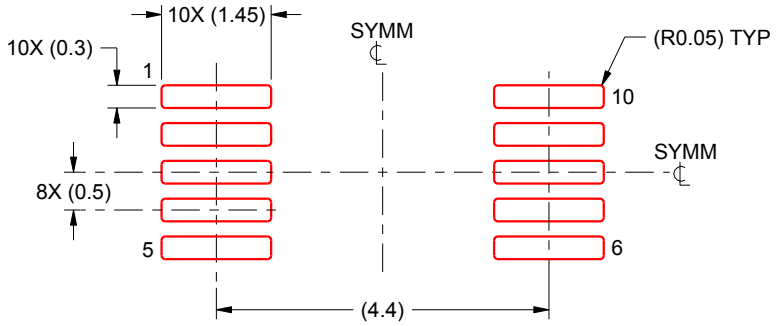


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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