参考資料

TI Designs: TIDA-00928
EMI準拠、125℃、10/100Mbpsイーサネット・ブリック、ツイストペアまたは光ファイバ・インターフェイスのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、低消費電力トランシーバDP83822Iを使用する10/100Mbps銅線または100Mbps光ファイバ・インターフェイス用のソリューションで、産業用アプリケーション向けにコストが最適化されています。DP83822Iは、標準のツイストペアまたは光ファイバ・トランシーバ(SC、ST、またはLC)上でデータの送受信を行うために必要なすべての物理レイヤ機能を備えています。このデザインには、アナログおよびI/O電源用に、LDOを使用して電源電圧レベルを設定するオプションがあります。このブリックは、MII用に構成された内蔵MACでTM4C129X Tiva™MCUと接続します。このリファレンス・デザインは、放射、ESD、EFTについて事前認証テスト済みです。

リソース

TIDA-00928	デザイン・フォルダ
DP83822I	プロダクト・フォルダ
DP83822IF	プロダクト・フォルダ
TM4C129XNCZAD	プロダクト・フォルダ
DP83849IF	プロダクト・フォルダ
TPS75418	プロダクト・フォルダ
TPS75433	プロダクト・フォルダ
TL1963A	プロダクト・フォルダ
TPD4E05U06	プロダクト・フォルダ

TI E2E™ Community

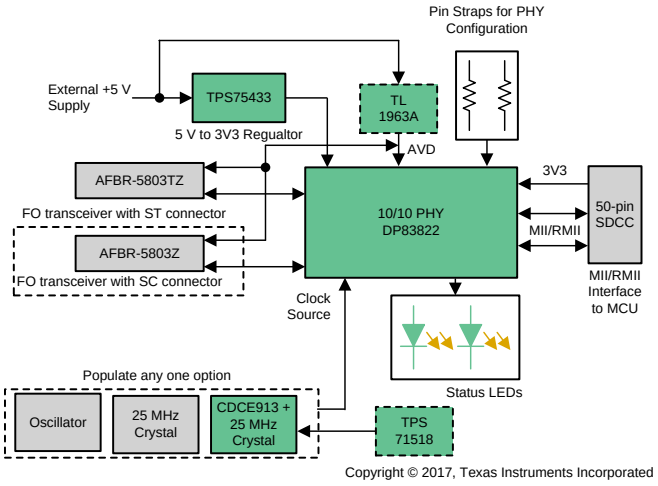
E2E™エキスパートに質問

特長

- DP83822IまたはDP83822IFイーサネットPHYを基礎とし、ファイバ(100BASE-FX)またはツイストペア(銅線: 100BASE-TXおよび10BASE-Te)インターフェイス付き
- アナログとI/Oの電源電圧レベルを別々に設定可能
- 電源電圧オプションと規定電力: 1.8V AVD < 120mW、3.3V AVD < 220mW
- リンクと動作用のプログラマブルLEDのサポート
- 事前認証テスト済み
  - EN55011 Class-B放射要件に適合
  - IEC 61000-4-2レベル4、基準Bに適合
  - IEC 61000-4-4レベル4、基準Bに適合
  - IEC 61000-4-4レベル3、基準Aに適合
  - IEC 61000-4-3、IEC 61000-4-6のテスト要件と受け入れ基準Aに適合
- 事前認証テスト済み: EN55011 Class-B放射要件に適合
- ホストMCUインターフェイス: TM4C129XNCZAD 32ビット Arm® Cortex®-M4F MCUによる性能評価およびシステム実装
- 外部絶縁型変圧器のPHY側コモンモード・チョークによりEMIおよびEMC性能を改善
- DP83822Hの温度範囲: -40℃～+125℃

アプリケーション

- サーキット・ブレーカ、保護リレー、スマート・メータ(AMI)などの産業用アプリケーション
- RTU、IED、ベイ・コントローラなどの基地局自動化製品
- マージング・ユニット、プロトコル・コンバータ、リモートI/O
- モータ・ドライブやファクトリ・オートメーション用のEthercatアプリケーション



1 System Description

Protection relays are intelligent electronic devices (IEDs) that receive measured signals from the secondary side of current transformers (CTs) and voltage transformers (VTs). The relays detect whether or not the protected unit is in a stressed condition and send a trip signal to the circuit breaker to disconnect the fault from the system. A key requirement in all protection relays is communication. Legacy protection relays use the RS-485 as the standard communication interface. Next generation protection relay platforms are migrating from RS-485 to Ethernet as the standard interface due to the need for higher data rates, networking, and remote monitoring.

1.1 Power Systems Automation

Power system automation is an important aspect in an electrical power network. In power system automation, data acquisition systems play a major role as a base of the power system automation. From the recent trends and developments in power system automation, computerized system automation is most efficient compared to normal systems. A computerized power network for a data acquisition system helps the system and controller to meter and monitor the values for further manipulations for full-scale power system automation and system controlling.

1.2 Classification of Power System Automation

Power systems automation is broadly classified into the following categories:

- Substation automation
- Distribution automation

1.3 Migration From Serial Communication to Ethernet

Serial communications were traditional in utilities installations; they were well understood and proven, available in robust packaging, and with adequate speed for their time. They required continuous point-to-point connections for operation. However, serial lines have been often associated with proprietary protocols and limited speed. Ethernet connectivity is becoming more popular because it offers standards-based interoperability and performance, along with the hardened characteristics required for many utilities installations. As older substations with serial communications are upgraded, serial interfaces are being replaced by Ethernet connections. Ethernet's simple and effective design has made it the most popular networking solution at the physical and data link levels. With high-speed options and a variety of media types from which to choose, Ethernet is efficient and flexible. These factors and the low cost of Ethernet hardware have made Ethernet an attractive option for industrial networking applications. Also, the opportunity to use open protocols such as TCP/IP over Ethernet networks offers the possibility of a level of standardization and interoperability. The result has been an ongoing shift toward the use of Ethernet for Grid Infrastructure applications. Ethernet is increasingly replacing proprietary communications.

1.4 Advantages With Ethernet

Because Ethernet is a standard, it is the most affordable way to have connectivity. Being a standard means more products that can connect together and a greater potential for reasonably priced replacement components and long-term support. As a standard, Ethernet is the protocol of choice for new technologies that are being introduced in industrial facilities such as factories and substations. It is more profitable today for developers of technologies such as programmable controllers, dual-ported IEDs, and low-cost security cameras to introduce a product that works with a large variety of installed communications devices than to go to the expense of developing specific versions to meet proprietary communications requirements. Further, with Ethernet using fiber cabling, bandwidth is essentially free because it is practically unlimited for a one-time installation cost. An added benefit is that industrial Ethernet is compatible with IT facilities and eliminates a conversion bottleneck where factory and corporate networks meet.

1.5 Ethernet Interface Based End Equipment Application

Whether copper or fiber, Ethernet is one of the most common wired interface that is used in grid applications for remote monitoring, automation, and implementing redundant protocols.

1.5.1 Circuit Breakers, Protection Relays, and Smart Meters

Circuit breakers, protection relay, and smart meters are connected to the network for remote monitoring using Ethernet. Devices are provided with multiple Ethernet ports for implementing HSR or PRP redundancy protocols and automation protocols.

1.5.2 RTU, IEDs, Bay Controllers, and Merging Units

Substation automation of power systems are based on end equipments at the process level, bay level, and station level. Most of the end equipments on the process level and bay level are connected to the network using Ethernet interface copper or fiber and IEC61850 standard. The stations level equipments are connected to the control station using Ethernet or serial interface and IEC61850 standard.

1.5.3 Protocol Converters and Remote I/Os

Protocol converters are used to connect Legacy devices, which do not have Ethernet connectivity to the Ethernet enabled network. Remote I/Os provide option to expand the number of I/Os used by protection relay for running the required protection algorithm.

1.6 Ethernet Fiber Optic

Copper-based Ethernet connections are limited to a data transmission distance of only 100 meters when using an unshielded twisted-pair (UTP) cable. By using a fiber conversion solution, fiber-optic cabling can be used to extend data transmission over greater distances. An Ethernet with fiber can also be used where there is a high level of EMI, which is a common phenomenon found in industrial plants. This interference can cause corruption of data over copper-based Ethernet links. Data transmitted over fiber-optic cable, however, is completely immune to this type of noise. Because fiber can transport more data over longer distances than copper cabling, increased distances provide the ability to reach more users and equipment. Fiber has complete immunity to electrical interference and provides higher security than copper cabling because fiber has no electromagnetic emission. These characteristics have made fiber an ideal medium for commercial, utility, government, and financial networks. Distances supported by a fiber network infrastructure are limited mostly by the optical power, or brightness, supplied by the active hardware interface. Fiber distances can range from 300 meters to 140 kilometers, depending on the type of media converter, cable, wavelength, and data rate. The use of Ethernet fiber-optics in LANs has increased due to the inherent advantages of fiber and high data rates can be maintained without electromagnetic (or radio-frequency) interference. Fiber offers higher voltage isolation, intrinsic safety, and elimination of ground loops in geographically large installations.

1.7 TI Design Advantage

The TIDA-00928 design demonstrates the advanced performance of the PHY in harsh industrial environments. This TI Design provides an IEEE 802.3u compliant 100BASE-FX, 100BASE-TX, and 10BASE-Te solution. The board operates from a single 5-V power supply with use of onboard regulators. The Ethernet Brick design enables Texas Instruments' customers to quickly evaluate, design, and release to market systems using the DP83822I Industrial Ethernet PHY. A 50-pin interface is provided to interface with a 32-bit Cortex M4 processor-based controller board. The board is designed in a small (2 inches × 3 inches) form factor, which makes it easy to fit into any of the present products. The Ethernet Brick reference design is compliant to EN55011 Class-A EMI requirements and immune to IEC61000-4-2 Level-4 electrostatic discharge (ESD).

The following products are used in the Ethernet Brick reference design:

- DP83822I or DP83822IF
- TPS75433 or TPS75418
- TL1963 or TL1963A
- TPS71518
- TPD4E05U06
- CDCE913

1.8 Key System Specifications

The primary objective of this TI Design is to create a platform that helps evaluate the DP83822I or DP83822IF in a compact form-factor board. The DP83822IF addresses the quality and reliability for footprint sensitive applications in industrial temperature rated systems. The DP83822IF also offers performance exceeding IEEE802.3u specifications with superior interoperability and cable reach. The design features in this reference design are listed in 表 1:

表 1. Ethernet Brick Design Features

FUNCTION	DESCRIPTION
Ethernet PHY	DP83822I Ethernet PHY features:
	Media independent interface (MII), reduced media independent interface (RMII), or reduced gigabit media independent interface (RGMII): resistor strapping options
	Configurable PHY addresses: resistor strapping options
	Single register access for complete PHY status
	Industrial temperature rating: –40°C to 85°C and –40°C to 125°C
	QFN 32-pin 5-mm×5-mm package
Power supply	Possible power input options are: • 5 V from external two-terminal connector • 5-V DC input from MII connector and onboard regulator to generate 3.3 V • 3.3-V DC input from MII with no onboard regulator • AVD (core) supply: 3.3 V or 1.8 V (using programmable LDO) • VDDIO I/O supply: 3.3 V, 2.5 V, or 1.8 V (using programmable LDO)
Specified PHY power consumption	1.8-V AVD < 120 mW, 3.3-V AVD < 220 mW
Ethernet fiber-optic interface	1300 nm, multimode, Ethernet 100 base-FX, Duplex SC or ST connector interface
Ethernet copper interface	CONN MOD JACK R/A 8P8C SHIELDED
MAC controller interface	50-terminal MII connector
Clock	This TI Design has three options to provide clock to DP83822I: • 25-MHz crystal with internal oscillator • External oscillator to generate the clock (not populated) • Using TI's CDCE913PW and a 25-MHz crystal to generate the clock over I^2C lines (not populated)
Status LEDs	Two LEDs (link and activity with option to configure as pullup or pulldown)
EMC	ESD as per IEC 61000-4-2: Level 4, Criterion B EFT as per IEC 61000-4-4: Level 3, Criteria A RS as per IEC 61000-4-3, 10 V/M, Criteria A CS as per IEC 61000-4-6, 10 V/M, Criteria A
Radiated emission	EN55011, Class B

2 System Overview

This reference design is intended for all industrial applications where Ethernet is used. The design files include schematics, bill of materials (BOM), layer plots, Altium files, Gerber files, and test results. 図 1 shows the system block diagram of this reference design. The 10/100 Ethernet PHY is connected to the RJ-45 connector through the isolation transformer or to the fiber-optic (FO) interface using the transceiver. On the interface side, it is connected to a 50-pin connector to interface with a controller. Two status LEDs are provided to indicate link and activity. The PHY is configured using different strap options. The PHY can be powered by power coming from the MII connector or using an external 5-V supply. Currently, the PHY is provided with a clock signal using a crystal, but there are other options also available for clocking.

2.1 Block Diagram

The Ethernet brick TI Design has the following hardware options:

- DP83822I with a twisted-pair (TP) copper interface for 10/100 Mbps
- DP83822IF with an FO transceiver interface for 100 Mbps

The customer can choose the design architecture based on the interface requirements.

2.1.1 DP83822I With TP Copper Interface for 10/100 Mbps

The block diagram for a TP copper interface consists of the following functional blocks:

- Ethernet transceiver with a TP copper interface
- Analog and I/O power supply
- TP interface with ESD protection
- Optional clock for RMII
- MII or RMII connector for host interface

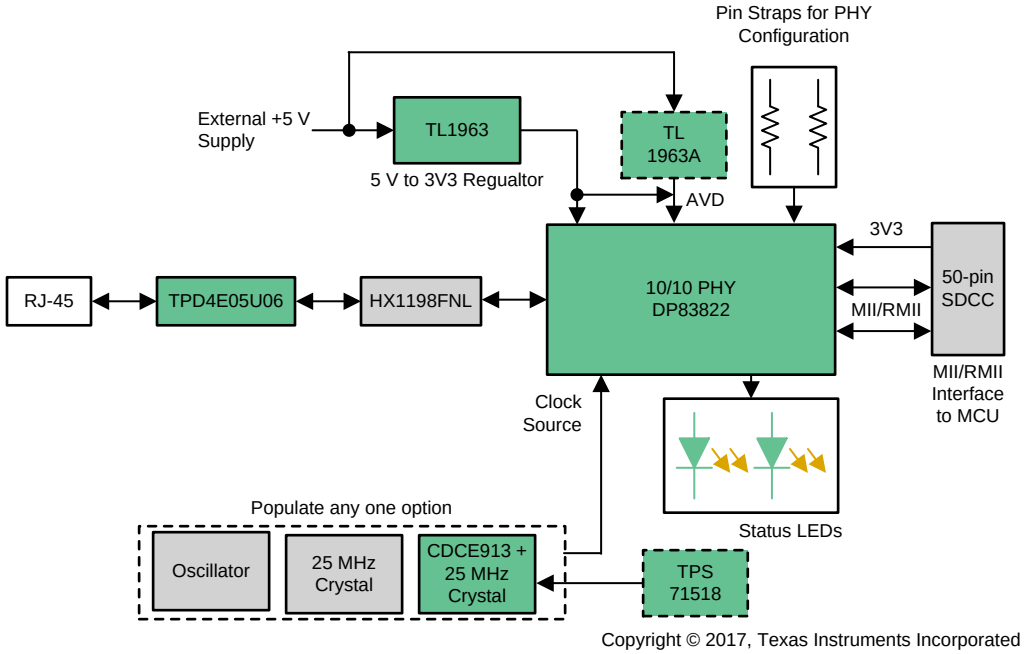


図 1. Ethernet Brick With Copper Interface

2.1.2 DP83822IF With FO Transceiver Interface for 100 Mbps

図 2 shows the Ethernet brick configured for an FO interface. This block diagram consists of the following functional blocks:

- Ethernet transceiver with a fiber interface
- Analog and I/O power supply
- FO transceiver SC or ST type
- Optional clock for RMII
- MII or RMII connector for the host interface

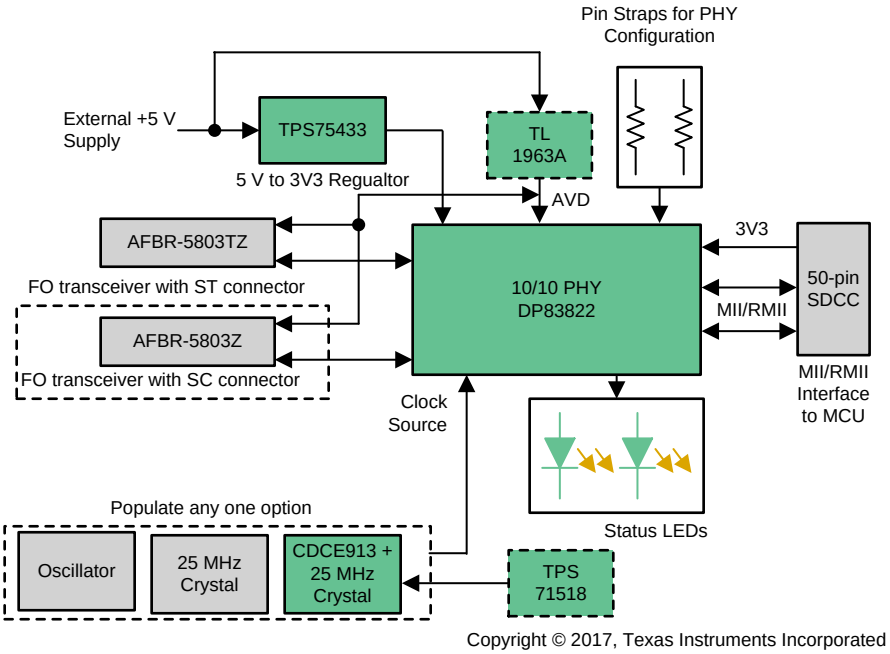


図 2. Ethernet Brick With FO Interface

2.1.3 Ethernet Transceiver DP83822I or DP83822IF

The following subsections detail the different ethernet transceivers that can be considered in the TIDA-00928 design.

2.1.3.1 Device Comparison Table

表 2 lists the different devices and the provided functions:

表 2. DP83822 Family Comparison

PART NUMBER	100BASE-FX SUPPORT	OPERATING TEMPERATURE
DP83822HF	Yes	–40ºC to 125ºC
DP83822H	No	–40ºC to 125ºC
DP83822IF	Yes	–40ºC to 85ºC
DP83822I	No	–40ºC to 85ºC

2.1.4 Analog and I/O Power

The device is designed for power supply flexibility by allowing for a range of I/O voltage interfaces (3.3 V, 2.5 V, or 1.8 V) and options for analog voltage (1.8 V or 3.3 V) to reduced power consumption. Automatic supply configuration within the DP83822 allows for any combination of VDDIO supply and AVD supply without the need for additional configuration settings.

2.1.5 Ethernet—Fiber Transceiver—100BASE-FX

The Ethernet brick is interfaced to the following fast Ethernet transceivers. These transceivers for 2-km multimode fiber backbones are supplied in the small 1×9 duplex SC or ST package style. 表 3 provides information on the part number used for the Ethernet FO interface.

表 3. Ethernet FO Interface Transceiver Part Numbers

PART NUMBER	DESCRIPTION	DETAILS
AFBR-5803TZ	FO transceiver module	ST, 100 Mbps, 1300 nm
AFBR5803Z	FO transceiver module	SC, 100 Mbps, 1300 nm

2.1.5.1 Transmitter Sections

The transmitter section of the AFBR-5803Z uses 1300-nm surface-emitting, InGaAsP LEDs. These receiver sections are packaged in the optical subassembly portion of the transmitter section. These LEDs are driven by a custom silicon device, which converts differential PECL logic signals, ECL referenced (shifted) to a 3.3-V supply, into an analog LED drive current.

2.1.5.2 Receiver Sections

The receiver sections of the AFBR-5803Z use InGaAsPIN photodiodes coupled to transimpedance preamplifier devices. These devices are packaged in the optical subassembly portion of the receiver. These pin and preamplifier combinations are coupled to a custom quantizer device that provides the final pulse shaping for the logic output and the signal detect function. The data output is differential. The signal detect output is single-ended. Both data and signal-detect outputs are PECL compatible, ECL referenced (shifted) to a 3.3- or 5-V power supply.

In 100BASE-FX mode, the device-transmit pins connect to an industry-standard fiber transceiver with PECL signaling through a capacitive-coupled circuit. In FX mode on the TX path, the device bypasses the scrambler and the MLT3 encoder, enabling the transmission of serialized 5B4B-encoded, NRZI data at 125 MHz. On the RX path, the device bypasses the MLT3 decoder and the descrambler, enabling the reception of serialized 5B4B-encoded, NRZI data at 125 MHz. The only added functionality in the aspect of data transmission for 100BASE-FX (compared to 100BASE-TX) is the support of far-end fault detection and transmission.

2.1.6 Host MCU Interface

The Ethernet transceiver is interfaced to the host MCU through MII or RMII. The TM4C129XNCZAD high-performance 32-bit ARM Cortex-M4F based MCU with 10/100 Ethernet MAC is used for testing the communication interface with the Ethernet transceiver. The DP83822I supports two modes of operation MII Mode and RMII Mode. The modes of operation can be selected by strap options or register control. For RMII mode, it is required to use the strap option because it requires a 50-MHz clock instead of the normal 25-MHz clock. In the each of these modes, the IEEE 802.3 serial management interface is operational for device configuration and status. The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHYs.

In this TI Design, the Ethernet PHY is interfaced to MAC through MII. The DP83822I incorporates the MII as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100-Mb/s systems. This section describes the nibble wide MII data interface. The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC). 表 4 shows the signaling for MII. See "Section 8.4.1 MAC Interfaces" of the device datasheet for more details.

The MII is a synchronous, 4-bit wide nibble data interface that connects the PHY to the MAC in 100BASE-TX and 10BASE-Te modes. The MII is fully compliant with IEEE802.3-2002 clause 22. The MII signals are summarized in 表 4:

表 4. MII Signals

FUNCTION	SIGNALS
Data signals	TX_D[3:0]
	RX_D[3:0]
Transmit and receive signals	TX_EN, RX_DV
Line-status signals	CRS
	COL

2.1.6.1 TM4C129XNCZAD MCU

Tiva C Series microcontrollers integrate a large variety of rich communication features to enable a new class of highly connected designs with the ability to allow critical, real-time control between performance and power. The microcontrollers feature integrated communication peripherals along with other high performance analog and digital functions to offer a strong foundation for many different target uses, spanning from human machine interface to networked system management controllers. In addition, Tiva C Series microcontrollers offer the advantages of ARM's widely available development tools, System-on-Chip (SoC) infrastructure, and a large user community. Additionally, these microcontrollers use ARM's Thumb®-compatible Thumb-2 instruction set to reduce memory requirements and, thereby, cost. Finally, the TM4C129XNCZAD microcontroller is code-compatible to all members of the extensive Tiva C Series, providing flexibility to fit precise needs.

For more information, see the TM4C129XNCZAD product page.

2.1.7 Programming

A JTAG interface is used to program the MCU. A 10-pin connector is provided to program the MCU.

2.2 Highlighted Products—System Design

This section describes the TI products used in this TI Design with design calculations.

2.2.1 Ethernet Transceiver DP83822I or DP83822IF

The following subsections detail the MCU interface as used in this TI Design.

2.2.1.1 DP83822I or DP83822IF Transceiver, Reset Operation, and Clock

The DP83822I transceiver has been configured for oscillator and MII in this TI Design. The analog supply and the I/O supply have been set to 3.3 V. The DP83822I includes an internal power-on reset (POR) function and does not need to be explicitly reset for normal operation after power-up. If required during normal operation, the device can be reset by a hardware or software reset.

2.2.1.1.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse (TTL level) with a duration of at least 1 μs to the RESET_N. This pulse resets the device such that all registers are reinitialized to their default values and the hardware configuration values are re-latched into the device (similar to the power-up and reset operation). This reference design has an option to do hardware reset by populating R16 on the board as shown in 図 3.

図 3 also shows the connection of a crystal resonator circuit with the DP83822I. The oscillator circuit is designed to drive a parallel resonance AT cut crystal with a minimum drive level of 100 μW and a maximum of 500 μW. If a crystal is specified for a lower drive level, a current limiting resistor must be placed in series between X2 and the crystal. This TI Design uses load capacitors equal to 33 pF and series resistors equal to 0 Ω.

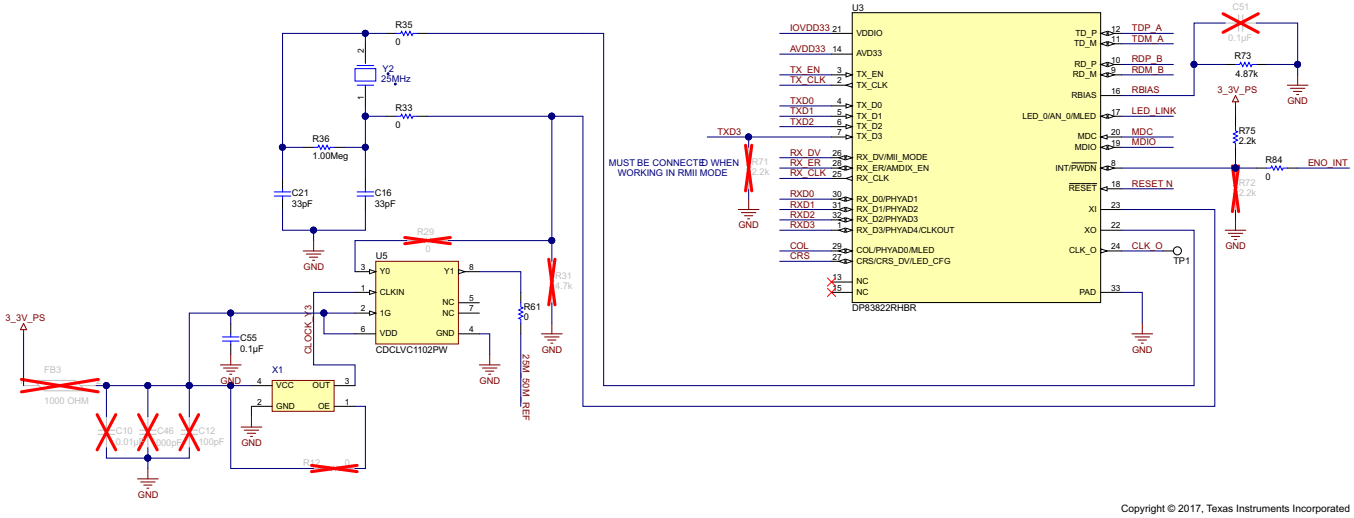


図 3. DP83822I or DP83822IF Transceiver Configuration

The DP83822I is a low-power, single-port, 10/100-Mbps Ethernet PHY. The device provides all physical layer functions needed to transmit and receive data over both standard TP cables or connect to an external FO transceiver. Additionally, the DP83822I provides flexibility to connect to a MAC through a standard MII, RMII, or RGMII. The DP83822I offers integrated cable diagnostic tools, built-in self-test and loopback capabilities for ease of use. The device supports multiple industrial buses with its fast link-down timing as well as Auto-MDIX in forced modes. The DP83822I is a feature rich and pin-to-pin ungradable option for the TLK105, TLK106, TLK105L, and TLK106L 10/100-Mbps Ethernet PHYs. The DP83822I comes in a QFN 32-pin, 5-mm×5-mm package.

Other key features include the following:

- IEEE 802.3u compliant: 100BASE-FX, 100BASE-TX, and 10BASE-Te MII, RMII, RGMII MAC interfaces, respectively
- Low-power single-supply options: 1.8-V AVD
- ±16-kV HBM ESD protection, ±8-kV IEC 61000-4-2 ESD protection
- Operating temperature: –40°C to 125°C
- I/O voltages: 3.3 V, 2.5 V, and 1.8 V

2.2.1.2 Hardware Bootstrap Configurations

Bootstrap configuration is a convenient way to configure the DP83822I device into specific modes of operation. Some of the functional pins are used as configuration inputs. The logic states of these pins are sampled during reset and are used to configure the DP83822I device into specific modes of operation. 表 5 describes bootstrap configuration. A 2.2-kΩ resistor is used for pulldown or pullup to change the default configuration. If the default option is desired, there is no need for external pullup or pulldown resistors. Because these terminals may have alternate functions after reset is deasserted, these terminals must not be connected directly to VCC or GND.

Note:

- Because bootstrap pins may have alternate functions after reset is deasserted, they should not be connected directly to VCC or GND. Pullup and pulldown resistors are required for proper operation.
- Pins COL, LED_0, CRS and RX_ER have internal pullup resistors. All other pins with bootstraps have internal pulldown resistors. To account for the difference between the internal pullup and pulldown, see Table 8 and Table 9 of the DP83822I datasheet for proper implementation.
- LED_0 and LED_1 require parallel pullup or pulldown resistors when using the pin in conjunction with an LED and current limiting resistor.

表 5. Bootstrap Configuration

FUNCTION	COMPONENTS ON BOARD	DESCRIPTION
PHYAD0 (COL) PHYAD1 (RXD_0) PHYAD2 (RXD_1) PHYAD3 (RXD_2) PHYAD4 (RXD_3)	R52, R53 R64, R65, R66, R67	PHY address [4:0]: The DP83822I provides five PHY address terminals, the states of which are latched into an internal register at system hardware reset. The DP83822I supports PHY Address values 0 (<00000>) through 31 (<11111>). PHYAD [4:1] terminals have weak internal pulldown resistors, and PHYAD [0] has a weak internal pullup resistor, setting the default PHYAD if no external resistors are connected.
AN_0 (LED_LINK)	R46, R51	AN_0: FD-HD config. FD = pullup. The default wake-up is auto negotiation enable 100BT. Force Mode AN_0=0, 10Base-T, Half-duplex, 100Base-TX, Half-duplex AN_0=1, 10Base-T, Half- or full-duplex 100Base-TX, Half- or full-duplex
LED_CFG (CRS)	R69	LED configuration: This option selects the operation mode of the LED_LINK terminal (the default mode is Mode 1). All modes are also configurable via register access. See PHY Control Register (PHYCR), Address 0x0019.
AMDIX_EN (RX_ER)	R70	Auto-MDIX enable: This option sets the Auto-MDIX mode. By default, it enables Auto-MDIX. An external pulldown resistor disables Auto-MDIX mode.

表 5. Bootstrap Configuration (continued)

FUNCTION	COMPONENTS ON BOARD	DESCRIPTION
MII_MODE (RX_DV)	R63	MII mode select: This option selects the operating mode of the MAC data interface. This terminal has a weak internal pulldown, and it defaults to normal MII operation mode. An external pullup causes the device to operate in RMII mode.

図 4 provides details of the hardware pin strapping that has been done for this TI Design.

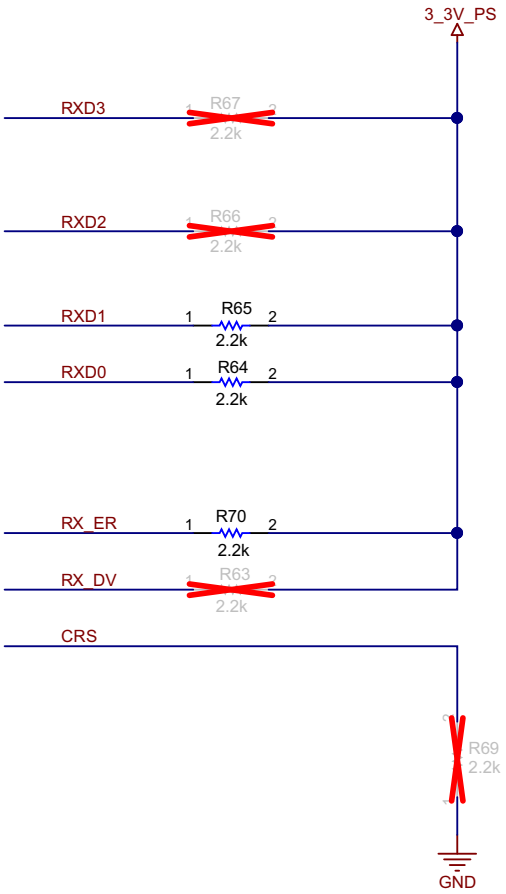


図 4. DP83822I Pin Strap Options

2.2.1.3 LED Configuration

The DP83822I devices support the use of two LEDs. The LEDs can be configured for pullup or pulldown using the resistors as shown in 図 5.

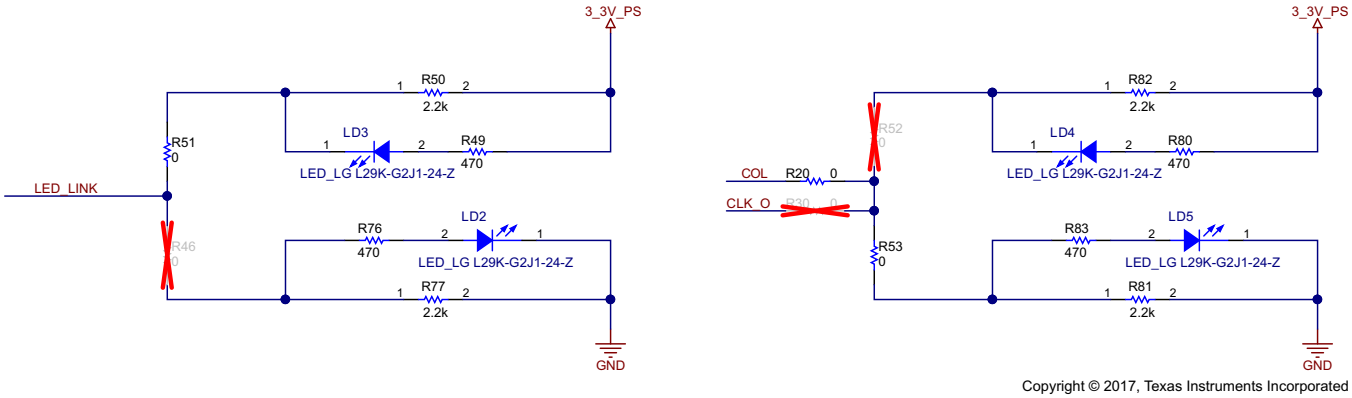


図 5. DP83822I LED_LINK and LED_SPEED Pin Configurations

2.2.2 ISOW7841 Power Supply and Filtering

2.2.2.1 Analog Power Supply for TP or FO Interface

Adjustable LDOs are used to set the analog and the I/O power supply. R22 is the resistor that has to be changed to adjust the output voltage to the following: 4.22K for 3.3 V, 2.56K for 2.5 V, 1.2K for 1.8 V.

When 3.3 V is used for analog supply and the I/O supply, one LDO can be used. When one LDO is used, R47 can be depopulated. When analog supply levels are different compared to I/O levels, populate R47 and depopulate R38.

図 6 provides the analog power configuration using adjustable LDOs including overvoltage protection.

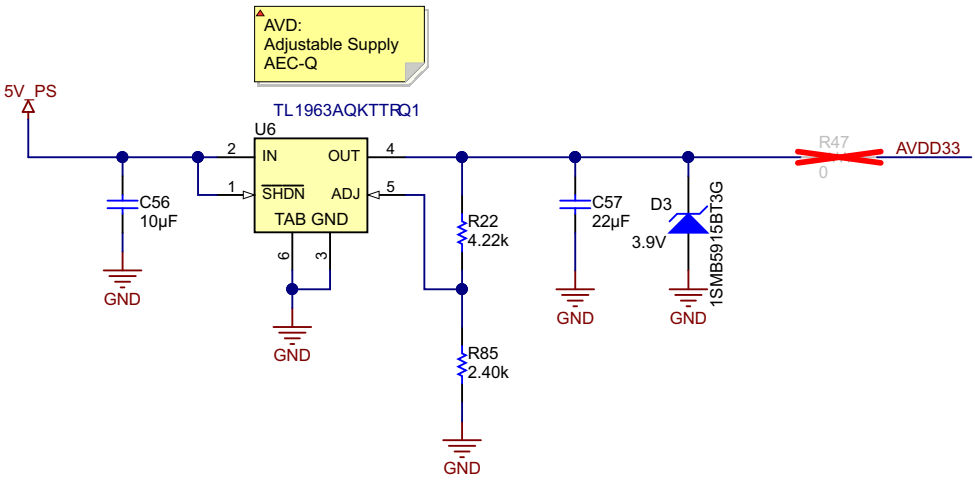


図 6. Analog Supply for TP or FO Interface

2.2.2.2 I/O Supply for TP

図 7 provides the I/O power configuration using adjustable LDOs including overvoltage protection.

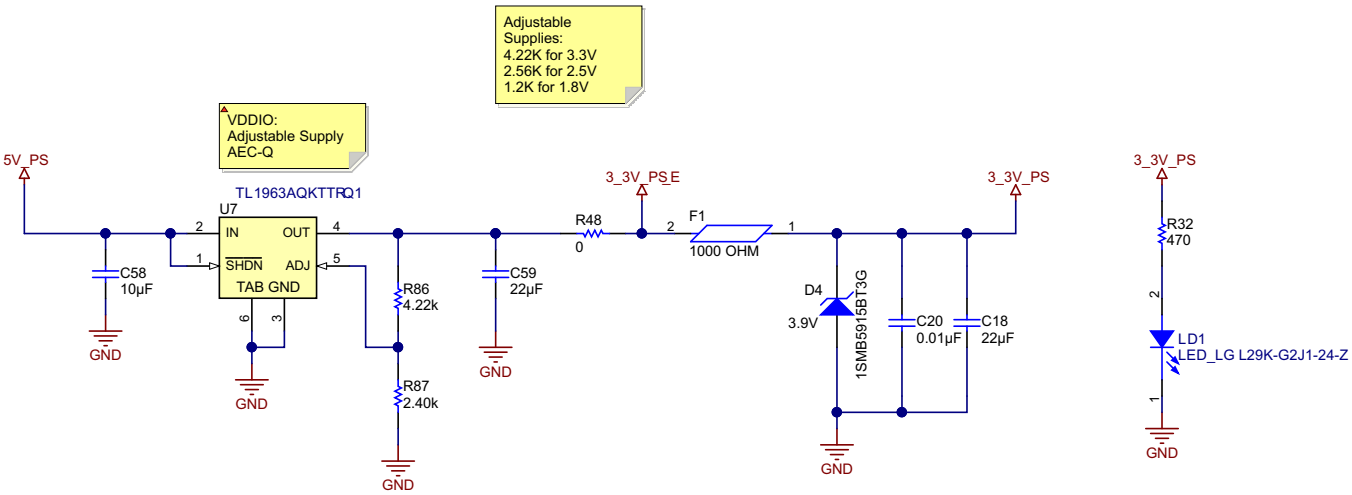


図 7. I/O Supply for TP Interface

注: For the TP interface, the analog and the I/O supply have been configured to 3.3 V.

2.2.2.2.1 TL1963A

The TL1963A device is a low-dropout (LDO) regulator optimized for fast transient response. The device can supply 1.5 A of output current with a dropout voltage of 340 mV. Operating quiescent current is 1 mA, dropping to less than 1 µA in shutdown. Quiescent current is well controlled; it does not rise in dropout as with many other regulators. Output voltage range is from 1.21 to 20 V. The TL1963A-xx regulators are stable with output capacitance as low as 10 µF. Small ceramic capacitors can be used without the necessary addition of ESR as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection.

Other key features include the following:

- Optimized for fast transient response
- Output current: 1.5 A, dropout voltage: 340 mV
- Low noise: 40 μV_{RMS} (10 Hz to 100 kHz) and 1-mA quiescent current
- No protection diodes needed and controlled quiescent current in dropout
- Adjustable output from 1.21 to 20 V
- Less than 1-µA quiescent current in shutdown
- Stable with 10-µF ceramic output capacitor

For more information, see the TL1963A product page.

2.2.2.3 Analog Supply and I/O Supply for FO Interface

When fiber interface is used the I/O supply has to supply the power for the FO transceiver. A 2-A regulator is used to provide the required power supply to the transceiver. The fixed options for 3.3 V, 2.5 V, or 1.8 V is available and can be chosen based on the required power supply level. 図 8 shows the LDO used to provide the I/O supply for LDO. The current requirement is provided by a 2-A LDO.

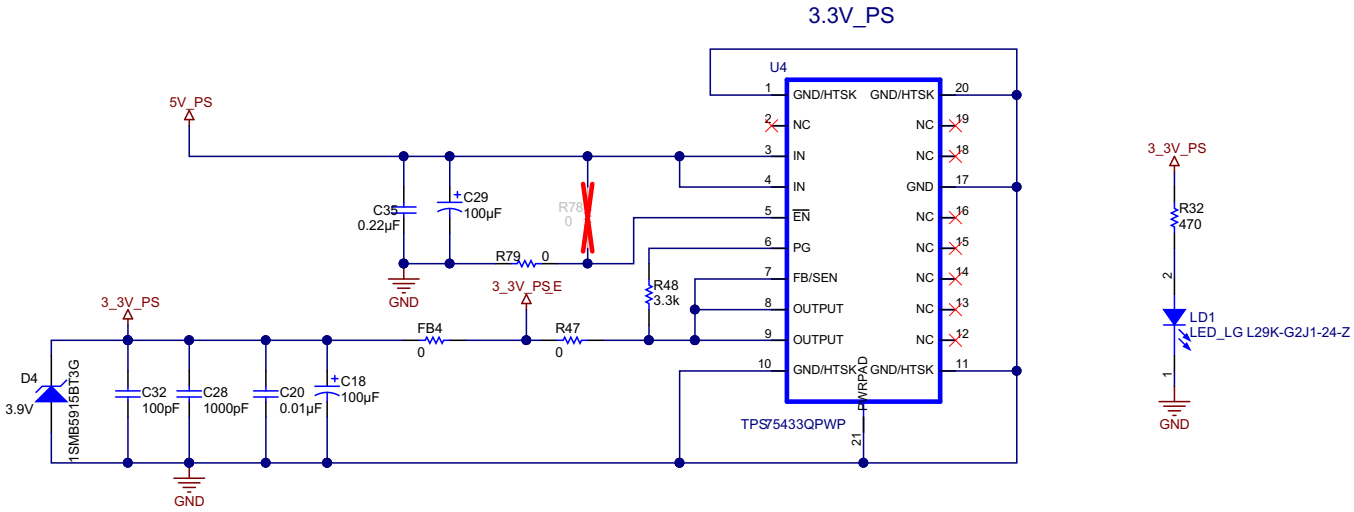


図 8. I/O Supply for FO Interface

注: For the FO interface, the analog and the I/O supply have been configured to 3.3 V.

2.2.2.3.1 TPS75433

The TPS754xx devices are LDO regulators with integrated power-on reset and power-good (PG) functions respectively. These devices are capable of supplying 2 A of output current with a dropout of 210 mV. Quiescent current is 75 µA at full load and drops down to 1 µA when the device is disabled. These devices are designed to have fast transient response for larger load current changes. The TPS754xxQ has a power good terminal (PG) as an active high, open drain output for use with a power-on reset or a low-battery indicator. The TPS754xxQ are offered in 1.5 V, 1.8 V, 2.5 V and 3.3 V fixed-voltage versions Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS754xxQ families are available in a 20-pin TSSOP (PWP) package.

Features

- 2-A LDO voltage regulator
- Available in 1.8- and 3.3-V fixed output
- Ultra-low 75-µA typical quiescent current and fast transient response
- 2% tolerance over specified conditions for fixed-output versions
- 20-pin TSSOP PowerPAD™ (PWP) package

For more information, see the TPS754 product page.

2.2.2.4 Power Consumption for TP Interface

表 6 provides information on the power consumption of the Ethernet transceiver with different voltage configurations

表 6. Ethernet Transceiver Power

POWER SUPPLY CONFIGURATION	TOTAL POWER (mW)
3.3-V AVD/CT and 3.3-V VDDIO	261
1.8-V AVD/CT and 3.3-V VDDIO	174

2.2.2.5 Power Consumption for FO Transceiver (AFBR-5803Z/5803TZ)

表 7 provides information on the power consumption of the FO, fast-Ethernet transceiver including the transmitter and receiver.

表 7. FO Fast Ethernet Transceivers

FUNCTION	TOTAL POWER (mW)
Transmitter electrical characteristics at VCC = 3.3 V	600
Receiver electrical characteristics at VCC = 3.3 V	250

2.2.3 TP Interface (Copper) With ESD Protection Using TPD4E05U06

The TP interface has three functional blocks: the RJ45 connector, ESD protection diodes, and isolation transformer. The isolation transformer and ESD protection diodes is selected based on the requirements to meet EMI and EMC tests. The design requirements for the DP83822I in TPI operation (100BASE-TX or 10BASE-Te) are as follows:

- AVD supply = 3.3 V or 1.8 V
- Center tap supply = AVD supply
- VDDIO supply = 3.3 V, 2.5 V, or 1.8 V
- Reference clock input = 25- or 50-MHz (RMII slave)

For more details, see Section 9.2.1: TPI Network Circuit of the DP83822i datasheet.

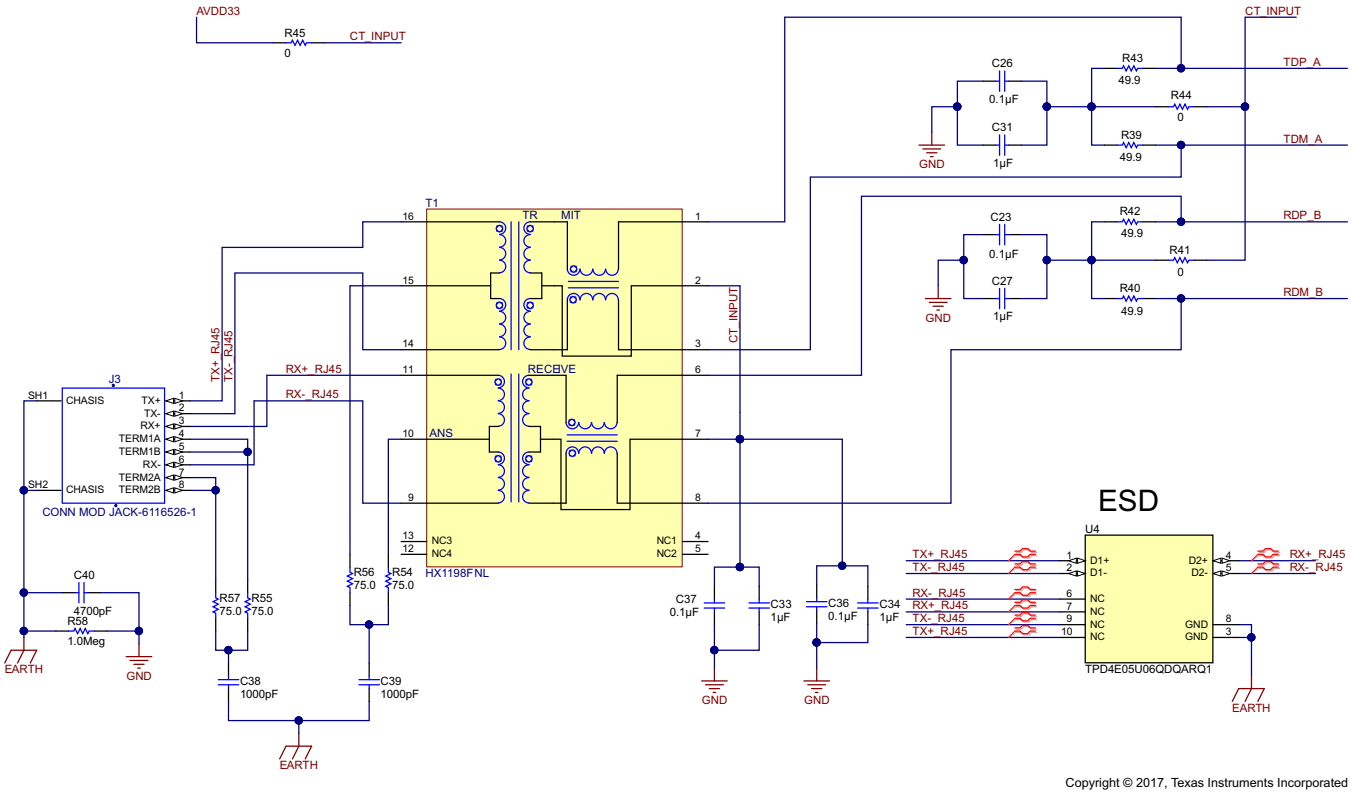


図 9. TP Interface and ESD Protection Schematic

The center tap of the transformer must be connected to the analog supply rail (AVD) with decoupling capacitors close to the transformer. All resistors and capacitors must be placed as close to the device as possible.

2.2.3.1 TP ESD Protection

This reference design uses a shielded RJ-45 connector without an internal isolation transformer. RJ45 is the standard cable used for all the Ethernet and LAN applications. An external isolation transformer is interfaced. The TIDA-00928 design uses the HX1198FNL from Pulse Electronics. The device is a 1:1 transformer with an isolation of 1.5 kV_{RMS} (for 60 seconds). Based on the application, it may be necessary to connect a common-mode choke along with the isolation transformer. The HX1198FNL already has a common-mode transformer integrated into. The network or Medium Dependent Interface (MDI) connection is through the transmit (TX+ and TX–) and receive (RX+ and RX–) differential pair terminals. The transmit and receive terminals connect to a termination network, then to a 1:1 magnetic transformer, then to ESD protection devices and an RJ-45 connector. This TI Design uses the TPD4E05U06 as ESD protection diodes in between the RJ-45 connector and the isolation transformer. The TPD4E05U06 is a quad-channel ultra-low cap ESD protection device. This device offers a ±15-kV IEC air-gap and ±8-kV contact ESD protection compliant to IEC 61000-4-2.

2.2.3.2 TPD4E05U06

The TPDxE05U06 is a family of unidirectional transient voltage suppressor (TVS) based electrostatic discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard.

Other key features include the following:

- IEC 61000-4-2 Level 4 ESD protection , ±12-kV contact discharge , ±15-kV air gap discharge
- IEC 61000-4-4 EFT protection , 80 A (5/50 ns)
- IEC 61000-4-5 surge protection, 2.5 A (8/20 µs)
- Industrial temperature range: –40°C to 125°C

For more information, see the TPD4E05U06 product page.

2.2.3.3 RJ45 Connector

表 8 describes the part numbers used for the Ethernet copper interface.

表 8. Ethernet RJ45 Interface Connector Part Numbers

PART NUMBER	DESCRIPTION	DETAILS
6116526-1	CONN MOD JACK 8P8C R/A SHIELDED	8p8c (RJ45, Ethernet)
HX1198FNL or HX1188FNL	MODULE XFRMR SGL ETHR LAN 16SOIC	Isolation transformer

2.2.4 Ethernet—Fiber Transceiver—100BASE-FX

The FO interface provides option for SC and ST type of interface using the AFBR-5803Z and AFBR-5803TZ transceivers. The fiber design schematics shows the AFBR-5803Z. The AFBR-5803TZ is pin compatible and can be used in the brick with the change of only transceiver and interface cable. All resistors and capacitors must be placed as close to the fiber transceiver as possible.

For more details. see Section 9.2.2: Fiber Network Circuit of the DP83822I datasheet.

2.2.5 MII to Host MCU

The MII connector provides interface between the Ethernet transceiver and the host MCU. The power supply from the MCU is also provided through this connector. The MII, RMII, or RGMII connects the DP83822I to the media access controller (MAC). The MAC may in-fact be a discrete device or integrated into a microprocessor, CPU, FPGA, or ASIC. To meet the EN55011 or EN55022 Radiated Emission requirements, provision for adding the following components are as follows:

- Series resistors: Series termination resistor provision is provided on all the signals. The value can be optimized based on testing.
- Parallel capacitor: Provision for capacitor has been provided on the transmit and receive clocks and also for the four receive data signals.

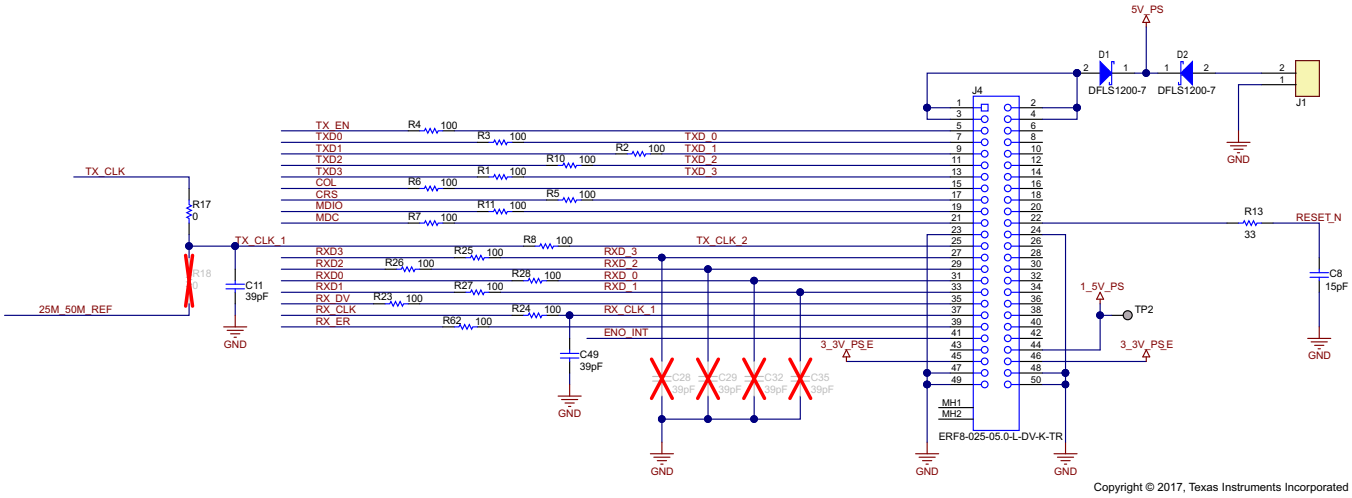


図 10. MII Connector for Host MCU Interface

2.2.6 Board Design Guideline

This section provides approaches for optimal board design. Also see Section 11.1: Layout Guidelines of the device data sheet. Note that the overall size of the Ethernet brick board can be reduced by optimizing the design further based on the application.

2.2.6.1 MII Layout Guidelines

For the series resistors on the MII lines, capacitor on clock lines, and RXD lines:

- MII signals are single-ended signals
- Route traces with a 50-Ω impedance to ground
- Keep trace lengths as short as possible; less than two inches is recommended and less than six inches maximum

2.2.6.2 Isolation Transformer Layout for TP Interface

There should be no metal layer running beneath the transformer. Transformers can inject noise into metal beneath them, which can affect the performance of the system. Because the DP83822 is a current-mode line driver design, the center tap pin on the device side of the transformer must be tied to the analog supply rail (AVD). Decoupling capacitors should be placed near the center tap pin of the transformer.

2.2.7 Software Description

表 9 describes the registers used for configuring the Ethernet PHY including performing hardware rest and MII configuration.

表 9. Software Configuration for EPHY

FUNCTIONALITY	CONFIGURATION DESCRIPTION
Hardware reset	A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to /RESET. This pulse resets the device so that all registers are reinitialized to default values, and the hardware configuration values are re-latched into the device (similar to the power-up and reset operation). The time from the point when the reset pin is deasserted to the point when the reset has concluded internally is approximately 200 µs.
External MII PHY initialization	Set the external PHY address (as per the boot strap configuration). All the read and write requests to the PHY use the configured external PHY address. To reset the PHY: 1. MII reset: Set the BMCR (0x00) register bit 15 to one. 2. Software or digital reset: Set PHYRCR (0x1F) data register bit 15 and bit 14 to one.
	Issue a delay of 500 µs.
	Set the BMCR (0x00) register auto negotiation enable and auto negotiation restart by setting bit 12 and bit 8 to one.
	Poll the BMSR (0x01) register bit 5 to check if auto-negotiation is complete.
MII_MODE	The MII_MODE is selected by pin 26 (RX_DV). This pin has internal weak pulldown and defaults to MII mode. (External pullup makes the PHY to operate in RMII mode.)
PHY ID	PHY ID is decided by the pullup registers (see the Bootstrap section of the DP83822 datasheet). Take care that the appropriate PHY ID is used for appropriate hardware bootstrap configuration (per pullup registers). This values of pins 29, 30, 31, 32, and 1 (PHYAD0/COL, PHYAD1/ RXD0, PHYAD2/ RXD1, PHYAD3/RXD2, and PHYAD4/ RXD3, respectively) are latched into an internal register at hardware reset.
LED configuration	Pin 17 and pin 29 can be used for LED configuration either as pullup or pulldown. Pin 17 indicates link status (fully lit) by default; activity is indicated by blinking the same LED. If the designer needs to use pin 29 for indicating LED status, MLEDCR has to be configured. Configuring MLEDCR provides an option to route the activity signal to pin 29 instead of pin 17. In order to route the activity signal to pin 29 instead of pin 17, the COL signal has to be disabled. For further details, see the LED Interface section of the DP83822I datasheet.
Testing DP83822I or DP83822IF	This TI Design has been created with the assumption that the hardware is connected to one end of the Ethernet cable, and the other end of the Ethernet cable is connected to the PC. TX clock and RX clock can be probed or measured (after the PHY is powered up and not in reset state). Initiate a ping request with an IP address that is within the subnet of the PC. For example, 192.16.0.100 is the PC IP address and 255.255.255.0 is the subnet mask. Initiate a ping command, for example, ping 192.16.0.1 –t TX[0:3] and RX[0:3]. The ping result will show some data patterns. Ping will create traffic at every plug-in of the Ethernet cable. After some time, when a destination host unreachable message is seen, there may not be a further Ethernet message on the wire.

2.2.7.1 FO Interface Register Configuration for DP83822IF

表 10 provides information on configuring the transceiver for fiber mode.

表 10. Fiber Mode Control Register

BIT	NAME	DEFAULT	FUNCTION
15	FX FEF faulting status	RO, LH	Asserted when the FEF (far-end fault) detection mechanism detects FEF signaling from the far-end peer.
14	FX PECL signaling status	RO ,LH	Asserted if the FX receiver detects violation of the PECL signaling from the optic transceiver (such as glitches or invalid pulse width).
13	FX SD status	RO, LL	Indicates the status of SD_IN signal in the fiber RX path. If SD_IN is deasserted, SD_IN will be latched low. Upon read, the value of the bit will be updated with the current value.
12:10	RESERVED	011, RO	—
9	Enable auto SD indication	0, RW	When asserted, this bit enables auto detection of the SD_IN signal based on SD indication the optic transceiver output. This mode assumes that when SD_IN is low, the optic transceiver does not transmit valid PECL signaling. The auto SD_IN feature can detect Valid PECL signaling, and once detected, auto SD_IN assumes the SD_IN is asserted and establishes the FX link.
8:0	RESERVED	1 0110 0100, RO	—

表 11 provides information on controlling the transceiver for fiber mode.

表 11. Fiber Mode Control Register, Address 0x0102

BIT	NAME	DEFAULT	FUNCTION
15	Enable manual SD_IN Config	0, RW	Allows manual configuration of the SD_IN signal. Manual configuration of the SD_IN signal allows the MAC to control the start of an FX link, assuming the MAC is in "PHY link partners connected" status. The actual control on the SD_IN is done using bit [14] in this register.
14	SD_IN manual config	0, RW	SD_IN manual control: '1' notifies the PHY SD_IN is on, and '0' notifies the PHY the SD_IN is off. Manual configuration overrides all other SD_IN mechanisms.
13:0	RESERVED	00 0010 0000 0000	Writes ignored, read as 0x200h.

2.2.8 Design Enhancements

Many end equipment with an increase in connected systems require power over Ethernet (POE) to be added to the Ethernet interface. For example, the Connected LED Lighting With IEEE802.3bt Power Over Ethernet (PoE) Reference Design supplies power and data over a single Ethernet cable to a connected LED lighting ballast. This reference design uses TI's TPS2372-4 PoE powered device (PD) interface, LM3409 buck controller, LM5165 buck converter, TPS62740 buck converter, TM4C1292NCPDT microcontroller (MCU), TPD4E05U06-Q1 ESD protection device, and DP83822I Ethernet PHY to provide power to the LED light remotely controlling the brightness and dimming parameters of the LED light while connected to the network. For more details, see *IEEE802.3bt Power Over Ethernet (PoE) Connected LED Lighting Reference Design*.

3 Getting Started Hardware

This section provides information on connecting the Ethernet brick for testing.

3.1 TP Interface

The setup shown in 図 11 is used to test the communication interface with the Ethernet brick configured for a TP (RJ45) interface.

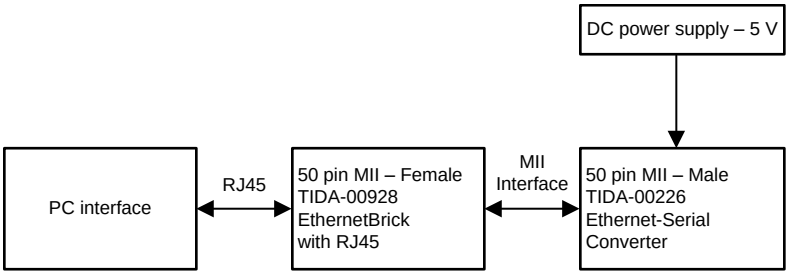


図 11. Ethernet Brick Interface With TP (RJ45) Interface

3.2 FO Interface

This section provides test setup information for different fiber interface types.

3.2.1 Ethernet Brick With ST Interface

The setup shown in 図 12 is used to test the communication interface with the Ethernet brick configured for an FO interface with a ST interface.

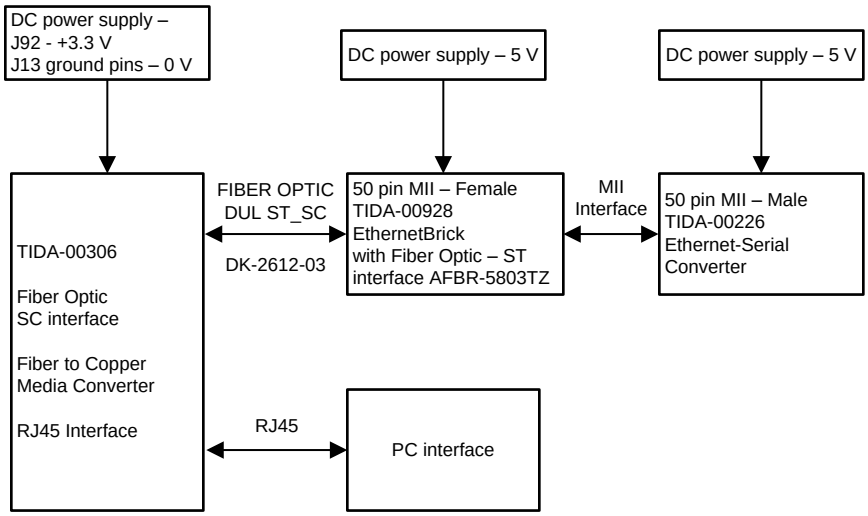


図 12. Ethernet Brick Interface With ST Interface

3.2.2 Ethernet Brick With SC Interface

The setup shown in 図 13 is used to test the communication interface with the Ethernet brick configured for an FO interface with a SC interface.

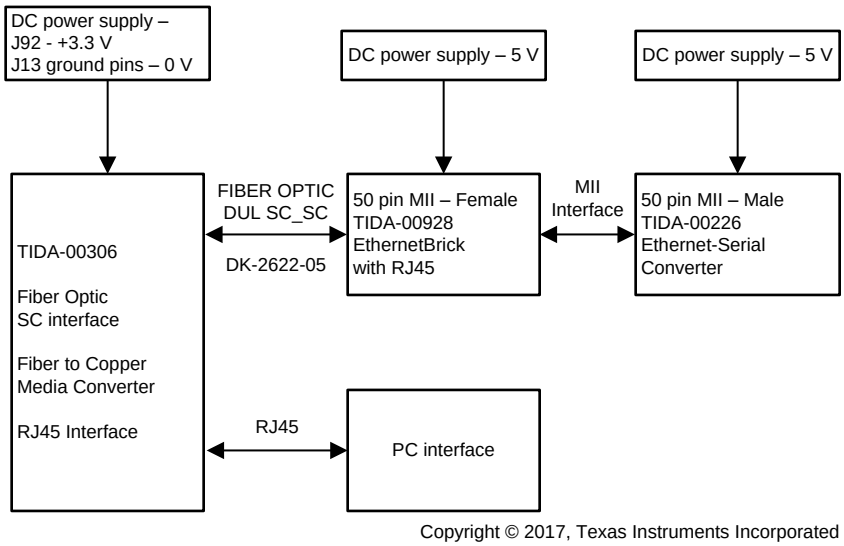


図 13. Ethernet Brick Interface With SC Interface

3.2.3 Cable and Transceiver Options

表 12 provides information on the different transceivers and interface cables used for FO communication.

表 12. FO Interface Components

INTERFACE TYPE	FO TRANSCEIVER	CABLE
ST	AFBR-5803TZ	DK-2612-03
SC	AFBR5803Z	DK-2622-05
LC, SFF	HFBR-5961L	DK-2632-02
SFP	SFP modules: SFP-1M31-2-CO (GLC-FE-100FX), HFBR 57E5APZ, FTLF1217P2BTL SFP connector: 1367073-1, CONN SFP SGL CAGE : U77-A1118-200T	DK-2632-02

3.2.4 SC and ST Interface Cable Configuration

表 13 provides interconnect information between the SC and ST connector-based communication interface.

表 13. Connection for Communication Testing Between SC and ST Type Fiber Interface

CONNECTOR TYPE	TX	RX
SC	B2	B1
ST	A1	A2

3.3 Media Converter for FO Interface Test Setup

See "Section 5.1 Communication Interface Testing (Computer to Device)" and "Section 5.2 Media Converter Implementation" of the TIDA-00306 design guide (TIDU510) for how to interface the media converter to the Ethernet brick with an FO interface.

3.4 Network Connection

Network connection settings for ping test are as follows:

- Go to "Network Connections."
- Go to "Local Area Connection."
- Right-click for "Properties."
- Select "Internet Protocol Version 4 (TCP/IPv4)."
- Go to "Properties."
- Select "Use the following IP Address."
- Enter the IP Address = 192.16.0.100, and click on "Subnet Mask," which should show 255.255.255.0.
- Click "OK."
- Click "Close."

4 Testing and Results

This section provides details of the different functional, performance, and EMC tests performed.

4.1 Functional Testing

The functional tests include the power supply, clock functionality, and Ethernet MII.

表 14. Board Functional Test Observations

PARAMETERS	OBSERVATION
Clock	25 MHz
AVD (3.15 to 3.45 V)	3.31-V DC
AVD (1.71 1.89 V)	1.795-V DC
VDDIO (3 to 3.6 V)	3.31-V DC
MII interface	OK
Link and activity LED	OK
Copper interface	OK
Fiber interface	OK

4.2 Communication Interface Testing

The communication interface test is done with different configurations for the Ethernet brick, as detailed in 表 15.

表 15. Summary of Communication Tests With DP83822I or DP83822IF Ethernet Brick

SERIAL NUMBER	TEST	OBSERVATION
1	Communication test with TP interface	The communication was tested for 1000 packet transfers without a communication failure at any time
2	Communication test with FO transceiver: ST interface	The communication was tested for 1000 packet transfers without a communication failure at any time
3	Communication test with FO transceiver: SC interface	The communication was tested for 1000 packet transfers without a communication failure at any time

4.2.1 Ping Test Observations

Go to Start → Run → Type "cmd" → Type "ping 192.16.0.1" and click "ENTER." It will show the following window and show four replies (see 図 14).

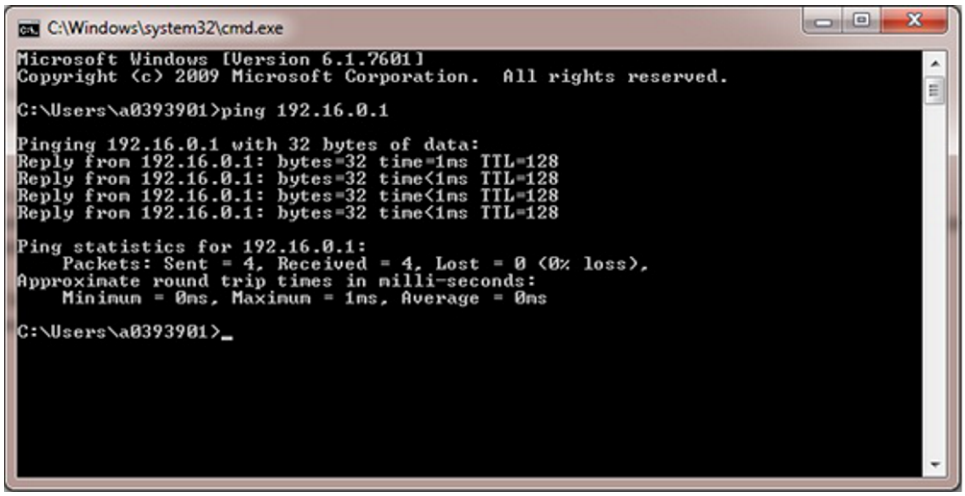


図 14. Ping Test Reply

4.2.2 Continuos Replies

For continued replies, type "ping 192.16.0.1 –t" and click "ENTER." It will show the following window and show continuous replies for the ping (see 図 15).

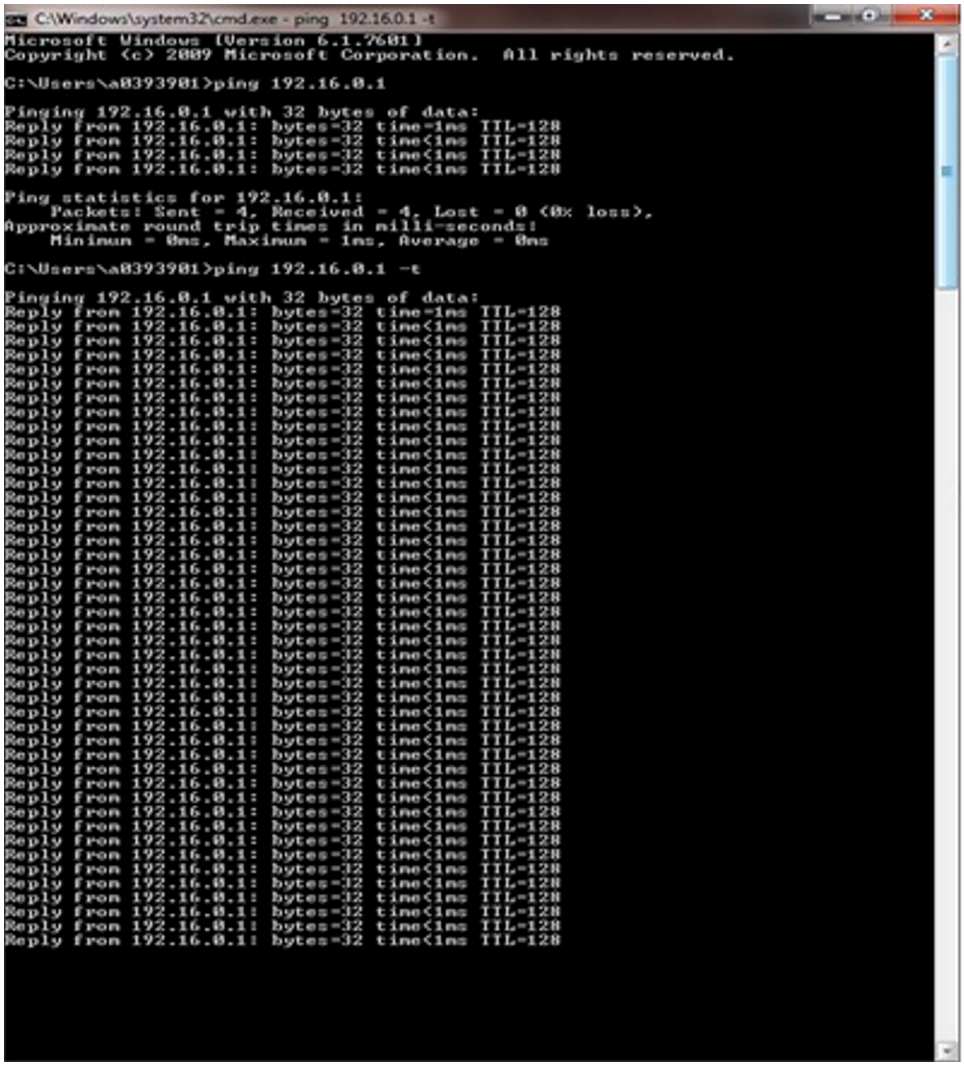


図 15. Continuos Ping Test Reply

4.2.3 Stop Communication

To stop the replies, press the shortcut "CTRL+C " or close the command prompt window. It will show the following window and the replies are stopped (see 図 16).

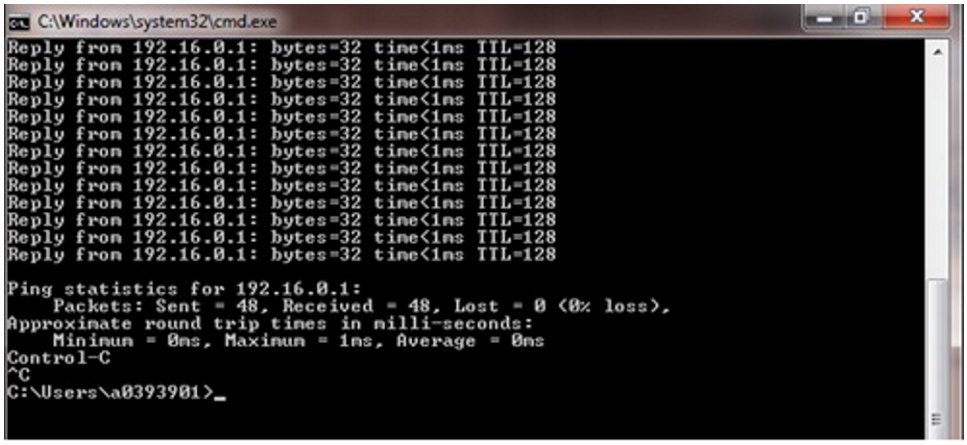


図 16. Ping Test Stopped

4.3 EMC IEC Pre-Compliance Testing

The following tests are performed as shown in 表 16.

表 16. EMC Tests

TESTS	STANDARDS	TEST REQUIREMENTS	TEST CRITERIA
Electrostatic discharge	IEC 61000-4-2	Contact ±8 kV	Criteria B
Radiated immunity	IEC 61000-4-3	10 V/M, 80 to 1000 MHz 3 V/M , 990 to 3000 MHz	Criteria A
EFT	IEC 61000-4-4	±2 kV with capacitive clamp, 5 kHz	Criteria B
EFT	IEC 61000-4-4	±1 kV with capacitive clamp, 5 kHz, 100 kHz, 1000 kHz	Criteria A
Surge	IEC 61000-4-5	±1 kV, communication cable, injected on shield	Criteria A
Conducted immunity	IEC 61000-4-6	0.15 to 80 MHz, CDN or EM clamp or injected to shield	Criteria A

表 17 provides information on the different criteria use to indicate the performance of the device under test.

表 17. Performance Criteria

CRITERIA	PERFORMANCE (PASS) CRITERIA
A	The Ethernet brick must continue to operate as intended. No loss of function or performance even during the test.
B	Temporary degradation of performance is accepted. After the test, Ethernet brick must continue to operate as intended without manual intervention.
C	During the test, a loss of functions accepted, but no destruction of hardware or software. After the test, Ethernet brick must continue to operate as intended automatically, after manual restart, power-off, or power-on.

4.3.1 IEC 61000-4-2 ESD Test

The IEC 610004-2 ESD test simulates an electrostatic discharge of an operator directly onto an adjacent electronic component. An electrostatic charge usually develops in low relative humidity and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the Ethernet brick, which can happen through direct contact with the Ethernet brick (contact discharge), or through an air-gap (air-discharge). This is applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the cable and the RJ45 connector during the test (contact discharge). After the test, the Ethernet brick is verified for functionality. The test results show the Ethernet brick can withstand the required discharge (see 表 19). The Ethernet brick was not permanently damaged.

表 18. ESD Test Steps

TEST NO	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 6 kV	Pass
6	Contact –6 kV	Pass
7	Contact 8 kV	Pass
8	Contact –8 kV	Pass

表 19. ESD Test Summary

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	RJ45	±8 kV	After the test, the Ethernet brick continued to operate as intended.

4.3.2 IEC 61000-4-3 Radiated Immunity

Testing to IEC 61000-4-3 ensures that the end equipment is immune to commonly occurring radiated RF fields. Some commonly occurring unintentional RF emitting devices in an industrial application are electric motors and welders. In the IEC 61000-4-3 test, a radiated RF field is generated by an antenna in a shielded anechoic chamber using a pre-calibrated field, swept from 80 MHz to 2.7 GHz. The RF voltage is amplitude modulated 80% at 1 kHz. The EUT is subjected to vertical and horizontal polarizations with different angles of placement. The reference design board has been tested to IEC 61000-4-3 radiated RF immunity testing Level 3 (10 V/m).

4.3.2.1 Setup for Testing Radiated Immunity

図 17 and 図 18 show the test setup for the reference design board.

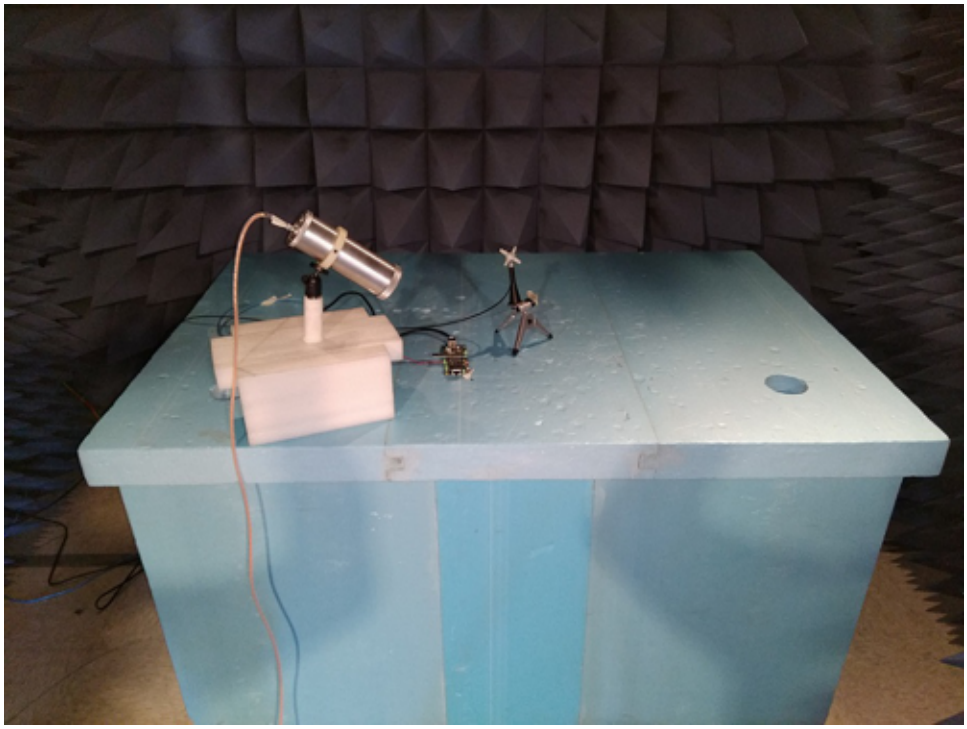


図 17. TIDA-00928 Board Placed Inside Shielded Anechoic Chamber

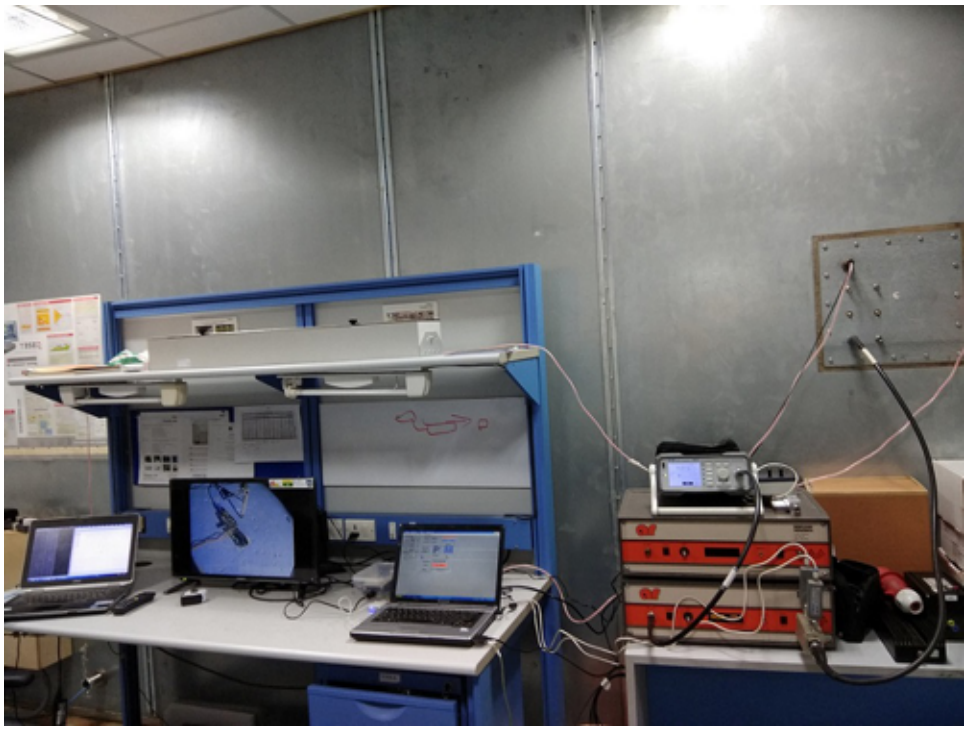


図 18. IEC 61000-4-3 Test Setup and Monitoring of TIDA-00928 Inside Shielded Anechoic Chamber

4.3.2.2 Test Results Summary

The reference design board is tested for different fields: strengths, frequencies, and antenna configuration. 表 20 provides the summary of the tests and observations.

表 20. Summary of TIDA-00928 Test Conditions and Observations

TEST	CONDITIONS	OBSERVATIONS
TEST CONDITION 1: 80 to 1000 MHz		
Radiated susceptibility as per IEC 61000-4-3	• 3 V/M, horizontal antenna polarization • 80 to 1000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 1162 • Packets received: 1162 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.
Radiated susceptibility as per IEC 61000-4-3	• 10 V/M, horizontal antenna polarization • 80 to 1000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 1455 • Packets received: 1455 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.
Radiated susceptibility as per IEC 61000-4-3	• 3 V/M, vertical antenna polarization • 80 to 1000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 987 • Packets received: 987 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.
Radiated susceptibility as per IEC 61000-4-3	• 10 V/M, vertical antenna polarization • 80 to 1000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 1450 • Packets received: 1450 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.

表 **20. Summary of TIDA-00928 Test Conditions and Observations (continued)**

TEST	CONDITIONS	OBSERVATIONS
TEST CONDITION 2: 990 to 3000 MHz		
Radiated susceptibility as per IEC 61000-4-3	• 3 V/M, horizontal antenna polarization • 990 to 3000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 470 • Packets received: 470 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.
Radiated susceptibility as per IEC 61000-4-3	• 3 V/M, Vertical antenna polarization • 990 to 3000 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms • DUT angle: 0 degrees	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 457 • Packets received: 457 • Packets lost: 0
		Camera pictures from inside the anechoic chamber observed continuously for LED indication.
		Tests at random frequency with changed dwelling time, DUT angles are performed, and no packet loss observed.

4.3.2.3 Continuous Ping Testing Results

Ping testing as shown in 4.2 is performed during the testing, 図 19 shows the and the results.

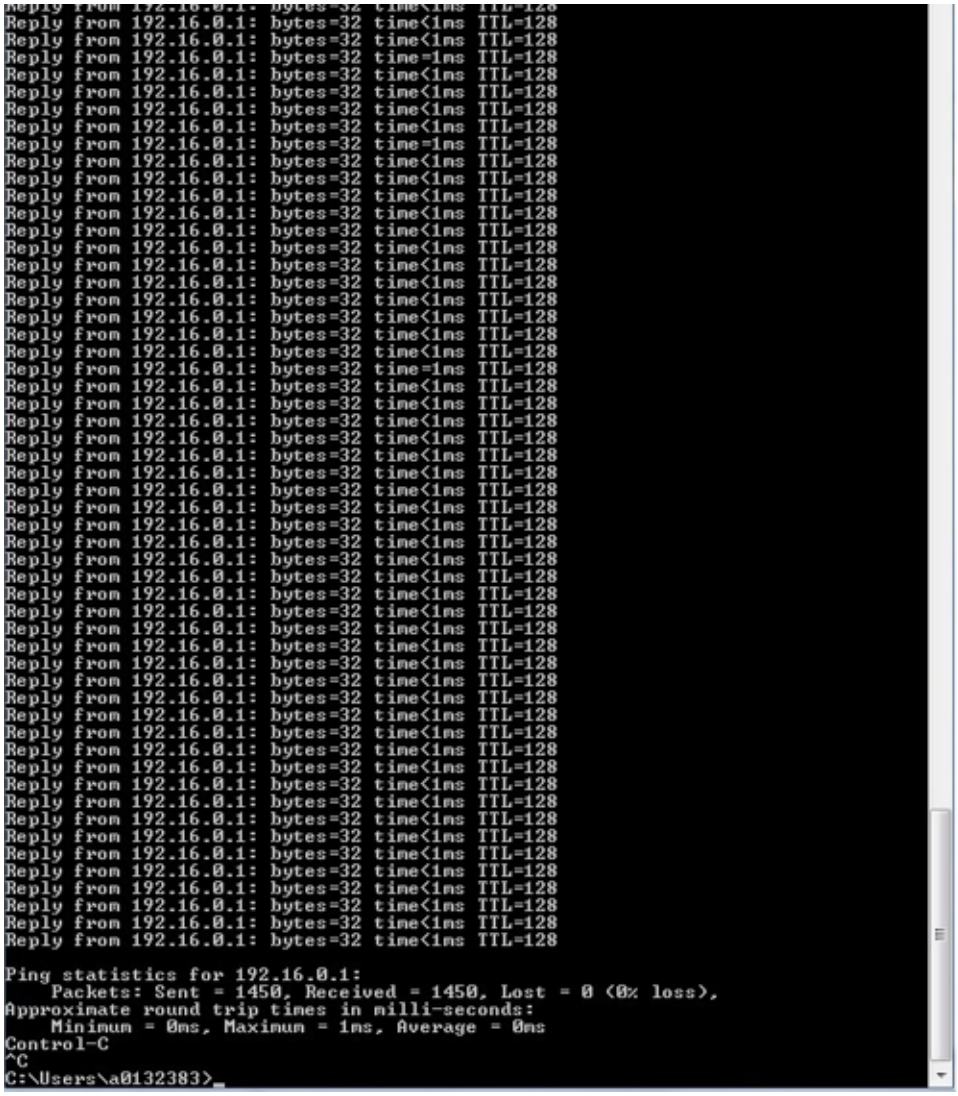


図 19. Ping Test Results During Radiated Immunity Testing

4.3.3 IEC 61000-4-4 EFT Test

The EFT burst was applied at I/O connectors with a clamp, and the performance criteria expected are as follows:

表 21. EFT Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
EFT	IEC 61000-4-4, ±2 kV with capacitive clamp	Communication cable	± 2 kV	Pass, Criteria B
				After the test, the Ethernet brick continued to operate as intended.

表 22 details the tests performed and observations.

表 22. Test Results Steps and Observations for EFT Testing

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV, 5 kHz	Pass, Criteria B
2	–0.5 kV, 5 kHz	Pass, Criteria B
3	1 kV, 5 kHz	Pass, Criteria B
4	–1 kV, 5 kHz	Pass, Criteria B
5	2 kV, 5 kHz	Pass, Criteria B
6	–2 kV, 5 kHz	Pass, Criteria B
7	0.5 kV, 100 kHz	Pass, Criteria B
8	–0.5 kV, 100 kHz	Pass, Criteria B
9	1 kV, 100 kHz	Pass, Criteria B
10	–1 kV, 100 kHz	Pass, Criteria B
11	2 kV, 100 kHz	Pass, Criteria B
12	–2 kV, 100 kHz	Pass, Criteria B

4.3.3.1 Setup

The burst signal is injected on the voltage inputs. The test is carried out with the Ethernet brick placed 10 cm above the reference plate. After the test, the Ethernet brick is verified for functionality. The test results show the Ethernet brick can withstand up to ±2 kV. The Ethernet brick performed normally after each test. Because functionality could not be verified during the test, the result is noted as passing Class B.

4.3.4 IEC 61000-4-4 EFT Test With Data Communication

The EFT burst is applied at I/O connectors with a clamp, and the performance criteria expected are as follows:

表 23. EFT Test With Data Communication Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
EFT	IEC 61000-4-4, ±1 kV with capacitive clamp and 5 kHz, 100 kHz, or 1000 kHz	Communication cable	± 1 kV	Pass, Criteria A
				Data error during the test is less than 5%

図 20 shows the test setup for the reference design board. The testing is done with a 45-meter Ethernet cable connected and a data packet continuously being pinged.

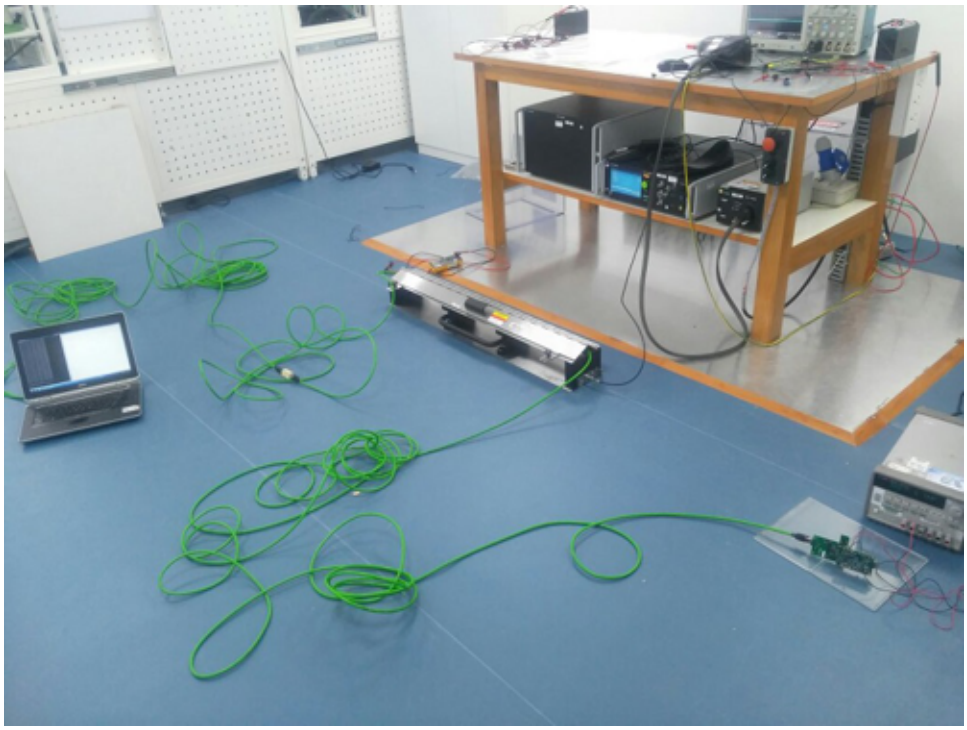


図 20. Test Setup for TIDA-00928 Board With Continuous Communication

表 24. Test Results Steps and Observations for EFT Testing With Data Communication

TEST NO	TEST MODE	OBSERVATION
1	± 0.5 kV , 5 kHz, data communication	Pass, Criteria A
2	± 0.5 kV , 100 kHz, data communication	Pass, Criteria A
3	± 0.5 kV , 1000 kHz, data communication	Pass, Criteria A
4	± 1 kV , 5 kHz, data communication	Pass, Criteria A
5	± 1 kV , 100 kHz, data communication	Pass, Criteria A
6	± 1 kV , 1000 kHz, data communication	Pass, Criteria A

4.3.4.1 Continuous Ping Testing Results Display

Ping testing as per 4.2 is performed during the testing, and 図 21 shows the results.

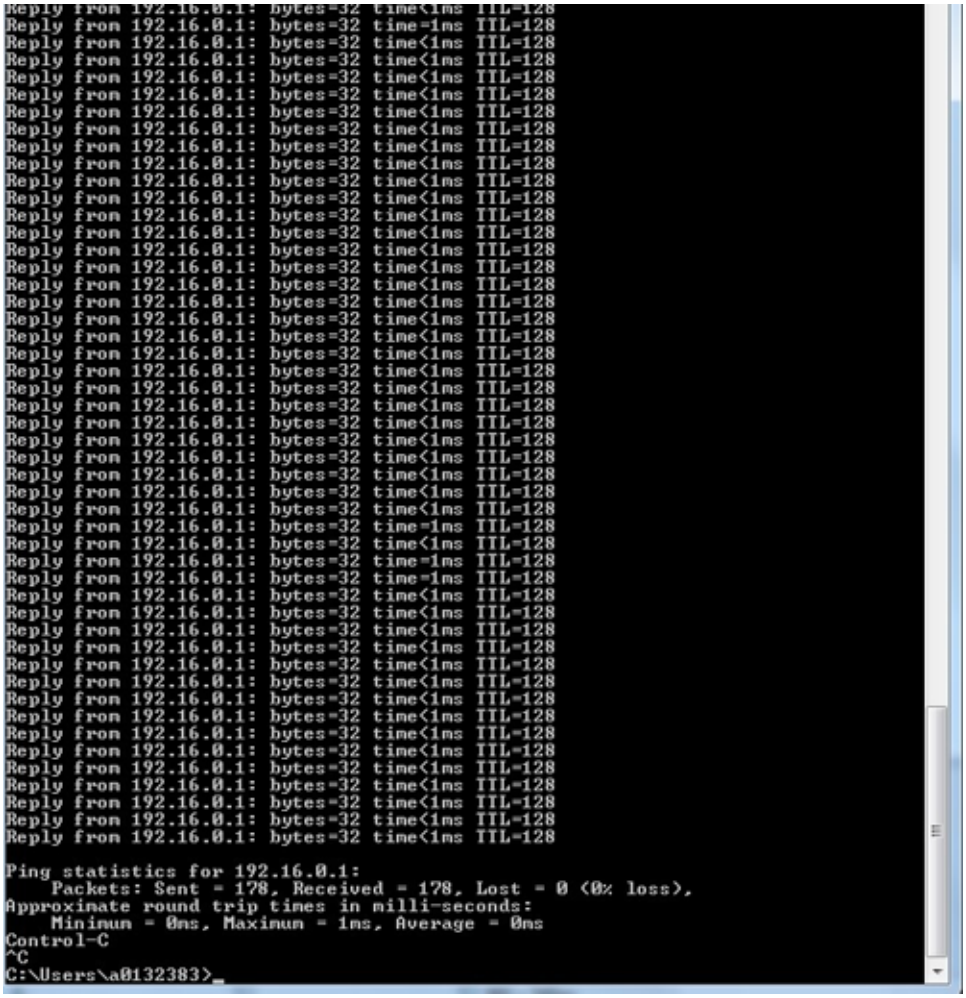


図 21. Summary of Data Packet Transmit and Receive With 100-kHz EFT Applied

4.3.4.2 TIDA-00928 Board EFT Test Result Summary

The Below table provides the summary of the test results for Ethernet Brick with different voltage EFT voltage levels

表 25. TIDA-00928 EFT Testing With Continuous Data Communication and 45-Meter Cable

TEST LEVEL	TEST CONDITION	OBSERVATION
± 500 V	5 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 192 Packets received: 192 Packets lost: 0 No change in performance after the test. Observed for 5 minutes
± 500 V	100 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 233 Packets received: 232 Packets lost: 1 Error type: Request timeout No change in performance after the test. Observed for 5 minutes
± 500 V	1000 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 220 Packets received: 219 Packets lost: 1 Error type: Request timeout No change in performance after the test. Observed for 5 minutes
± 1000 V	5 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 160 Packets received: 158 Packets lost: 2 Error type: Request timeout No change in performance after the test. Observed for 5 minutes
± 1000 V	100 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 180 Packets received: 180 Packets lost: 0 No change in performance after the test. Observed for 5 minutes
± 1000 V	1000 kHz, 1 minute	Meets Criteria A Packet size: 32 bytes Packets sent: 175 Packets received: 175 Packets lost: 0 Error type: Request timeout No change in performance after the test. Observed for 5 minutes

4.3.5 IEC 61000-4-5 Surge Immunity

Surge is applied on the shielded cable, and the performance criteria expected are as follows:

表 26. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
Surge	± 1 kV	Communication cable	± 1 kV	Pass, Criteria A

表 27. Test Results Steps and Observations For Surge Testing

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV	Pass
2	–0.5 kV	Pass
3	1 kV	Pass
4	–1 kV	Pass
7	2 kV	Pass
8	–2 kV	Pass

4.3.5.1 Setup

Because the shielded cable is less than 20 m and has direct coupling to the shield (2 Ω/500 A, 20 s between surges), the system continued to communicate after test without any additional errors, which was validated for at least 5 minutes after the test. This test is performed with the TIDA-00299 reference design board.

4.3.6 IEC 61000-4-6 Conducted Immunity

The IEC 61000-4-6 conducted immunity test is applicable to end equipments that operate in environments where radio frequency fields are present and connected to main supplies or other networks (signal or control lines). The source of conducted disturbances is electromagnetic fields, emanating from RF transmitters that can act on the whole length of cables connected to the installed equipment. In the IEC 61000-4-6 test, an RF voltage is stepped from 150 kHz to 80 MHz. The RF voltage is 80% amplitude modulated (AM) by a 1-kHz sinusoidal wave. The reference design board is tested to Level 3, 10 V. For IEC 61000-4-6 testing, the stress signal is applied by using the EM clamp (for unshielded twisted pair [UTP] or shielded twisted pair [STP]), CDN (power supply lines), or direct injection to shielded, placed on the RJ45 communication cable or the power supply lines.

4.3.6.1 Setup for Testing Conducted Immunity

図 22 and 図 23 show the test setup for the reference design board.

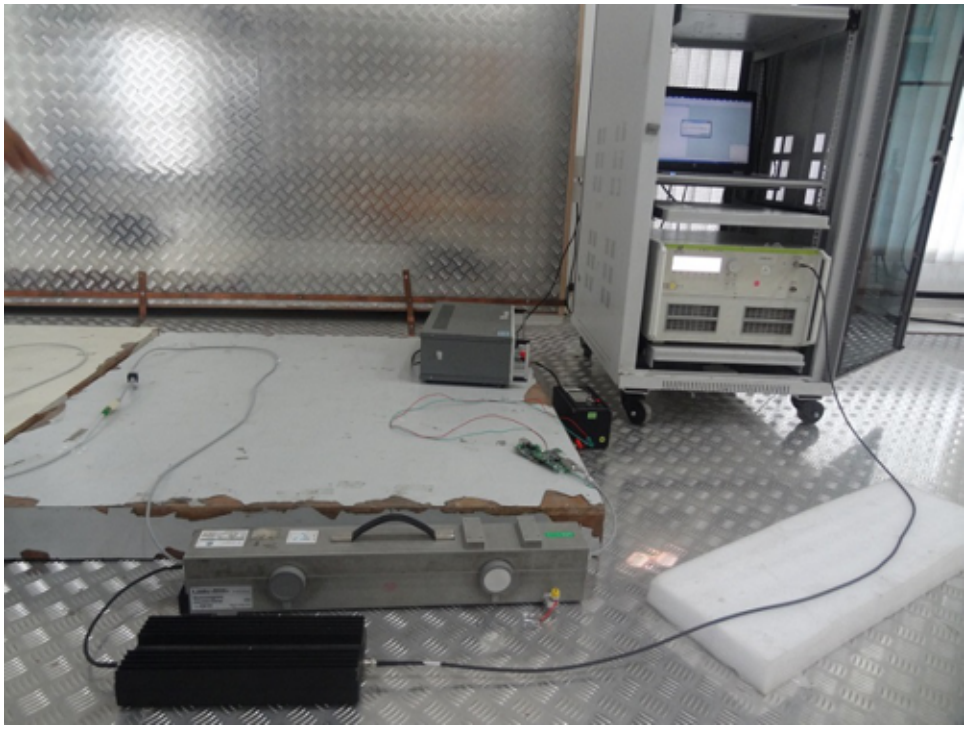


図 22. TIDA-00928 Board Testing on Communication Cable With EM Clamp

図 23. TIDA-00928 Board Testing on Communication Cable With CDN

4.3.6.2 Test Results Summary

The reference design board is tested for different voltage level and frequency configurations. 表 28 provides the summary of the tests and observations.

表 28. Summary of TIDA-00928 Board Test Conditions and Observations as per IEC 61000-4-6

TEST	CONDITIONS	OBSERVATIONS
TEST CONDITION 1: 150 kHz up to 80 MHz, TEST ON COMMUNICATION PORT		
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 3 V_{RMS}, Level 2 • Unshielded Ethernet cable • EM clamp • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 900 • Packets received: 900 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with changed dwelling time are performed, and no packet loss observed.
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 10 V_{RMS}, Level 3 • Unshielded Ethernet cable • EM clamp • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 882 • Packets received: 882 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with changed dwelling time are performed, and no packet loss observed.
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 3 V_{RMS}, Level 2 • Shielded Ethernet cable • EM clamp • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 913 • Packets received: 913 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with changed dwelling time are performed, and no packet loss observed.
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 10 V_{RMS}, Level 3 • Shielded Ethernet cable • EM clamp • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 1049 • Packets received: 1049 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with changed dwelling time are performed, and no packet loss observed.

表 28. Summary of TIDA-00928 Board Test Conditions and Observations as per IEC 61000-4-6 (continued)

TEST	CONDITIONS	OBSERVATIONS
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 10 V_{RMS}, Level 3 • Shielded Ethernet cable • Direct injection • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 866 • Packets received: 866 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with changed dwelling time are performed, and no packet loss observed.
TEST CONDITION 2: 150 kHz up to 80 MHz, DC POWER SUPPLY		
Conducted immunity (susceptibility) as per IEC 61000-4-6 4-6	• 3 V_{RMS}, Level 2 • Unshielded cable • Power supply line (CDN) • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 835 • Packets received: 835 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with a changed dwelling time are performed, and no packet loss observed.
Conducted immunity (susceptibility) as per IEC 61000-4-6	• 10 V_{RMS}, Level 3 • Unshielded cable • Power supply line (CDN) • Test frequency range of 150 kHz up to 80 MHz • 80% modulation • Frequency steps 1% of last step frequency • Dwell time: 1000 ms	There is no change compared with the initial operation during the test. • Meets Criteria A • Packet size: 32 bytes • Packets sent: 869 • Packets received: 869 • Packets lost: 0
		DUT functionality is observed continuously for LED indication.
		Tests at random frequency with a changed dwelling time are performed, and no packet loss observed.

4.3.6.3 Continuous Ping Testing Results

Ping testing as per 4.2 is performed during the testing, and 図 24 shows the results.

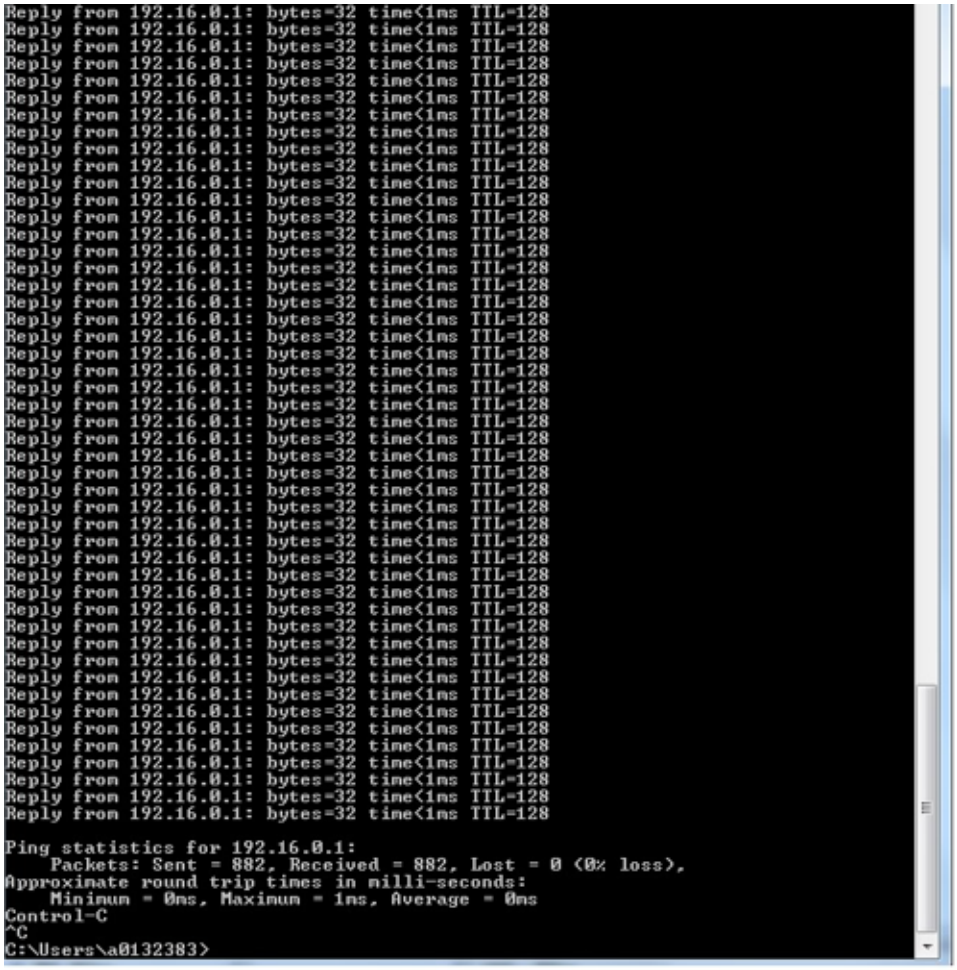


図 24. Ping Test Results During Conducted Immunity Testing

4.4 Radiated Emission (EMI)

MII signals are critical to pass the radiated emission test. Therefore, proper routing is crucial for signals with defined characteristic impedance with less vias. Series termination resistors need to be placed close to the source. It is recommended to have a capacitor connected from the termination resistor to ground to act as an RC filter to round off sharp edges from the MII signals. TX_CLK and RX_CLK are continuous signals that make their peak and quasi-peak amplitudes almost equal in emissions. For this reason, those signals play a critical role in passing the radiated emission test. The values of the termination resistor and capacitor need to be adjusted based on the test results.

4.4.1 Test Setup

図 25 shows the Ethernet brick setup for radiated emission testing.

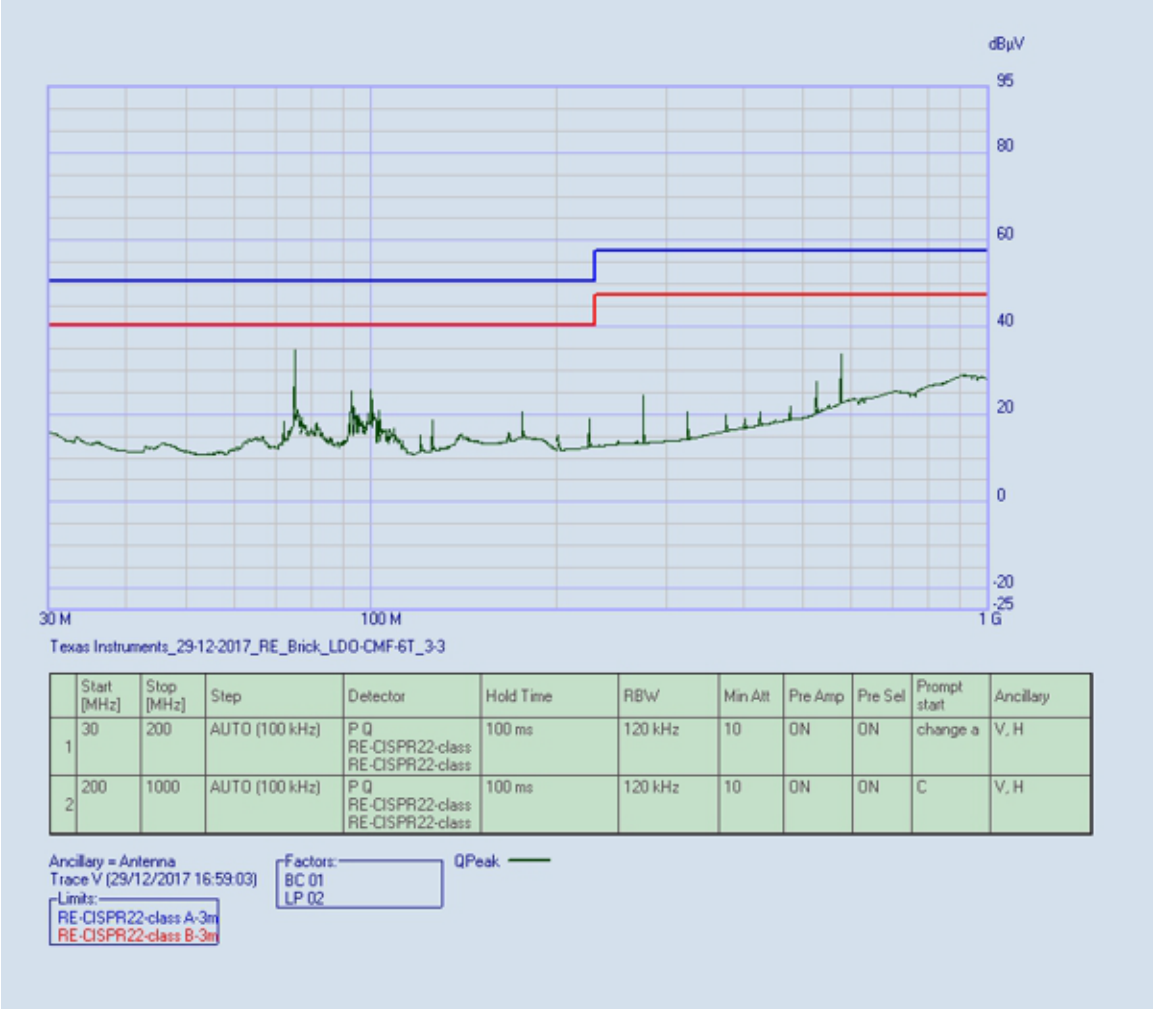
図 25. Ethernet PHY + Controller During Radiated Emission Test

The Ethernet brick has the following connections:

- Powered from a 6-V battery
- Battery inputs are connected through a common-mode inductor (constructed using a B64290A0719X049 inductor with an AL value of 1.13 µH and six turns of winding)
- Ethernet brick interfaced to computer with continuously communication and checking for packet error
- DC/DC converter TPS62177 on the TIDA-00226 reference design is replaced with the TL1963A-33DCYR LDO to power both TIDA-00226 and TIDA-00928 reference designs

4.4.2 Test Scan With VDD Supply Configured to 3.3 V and I/O Supply Configured to 3.3 V

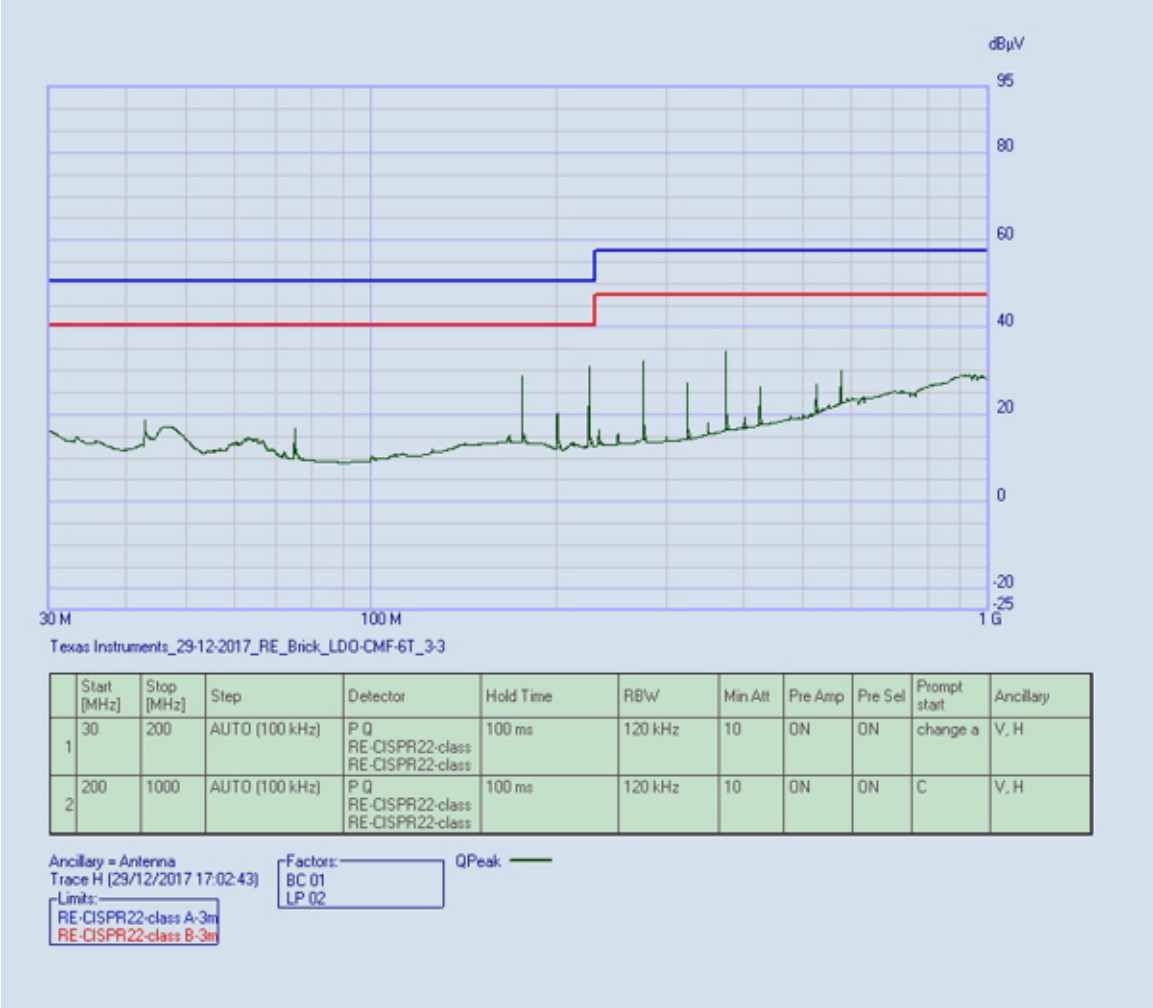
The radiated emission testing is done with the Ethernet brick communicating continuously with the computer. Disturbance field strength limits (quasi-peak) according to CISPR 11 / EN 55011 and CISPR 22 / EN 55022, normalized to a distance of 3 m. 図 26 shows the radiated emission plot with vertical polarization.



	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	30	200	AUTO (100 kHz)	P Q RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	change a	V, H
2	200	1000	AUTO (100 kHz)	P Q RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	C	V, H

図 26. Quasi-Peak Measurements in Vertical Polarization

図 27 shows the radiated emission plot with horizontal polarization.



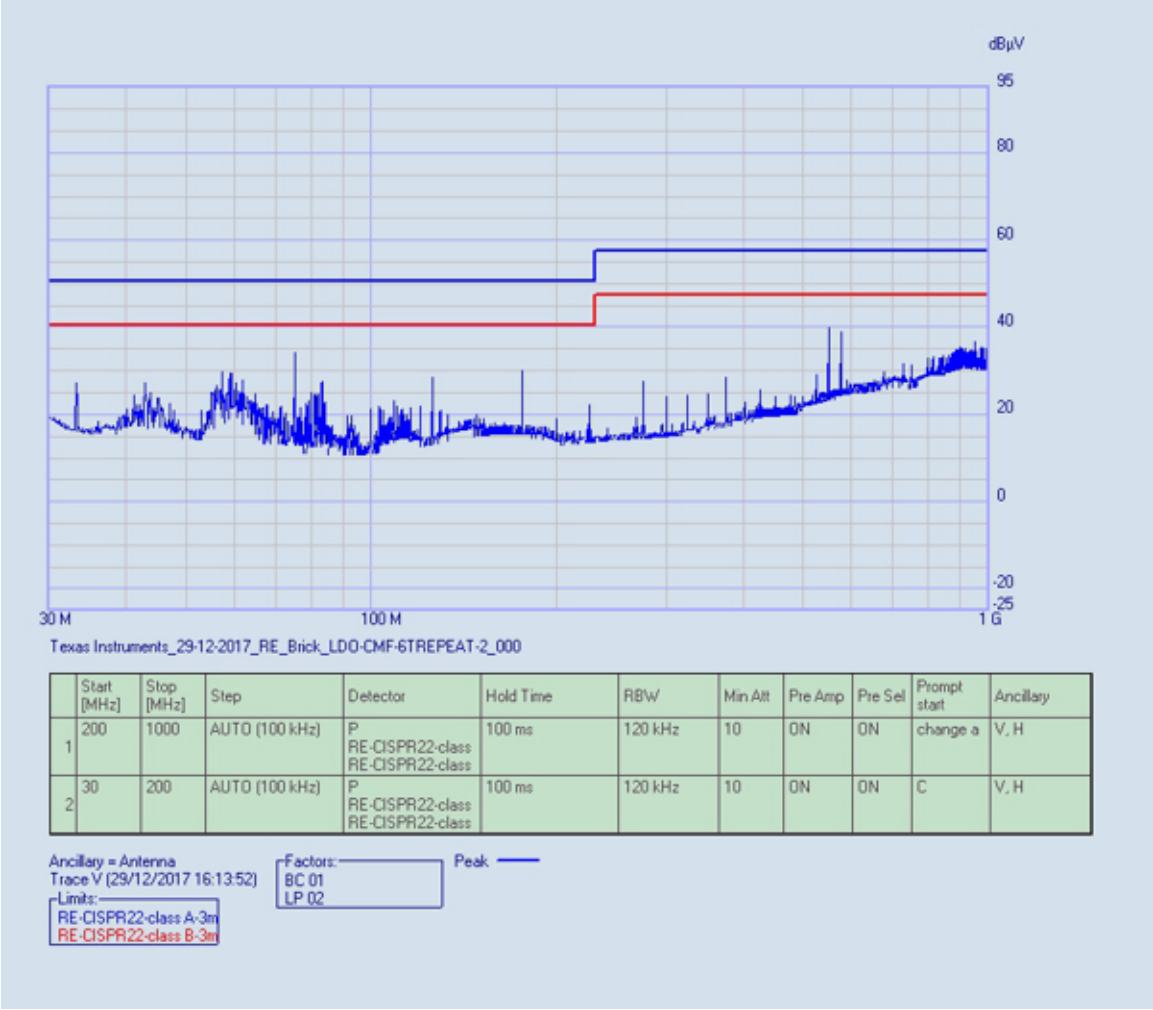
	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	30	200	AUTO (100 kHz)	P Q RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	change a	V, H
2	200	1000	AUTO (100 kHz)	P Q RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	C	V, H

図 27. Quasi-Peak Measurements in Horizontal Polarization

注: The Ethernet PHY brick has passed Class A limits with around a 8-dB margin.

4.4.3 Test Scan With VDD Supply Configured to 1.8 V and IO Supply Configured to 3.3 V

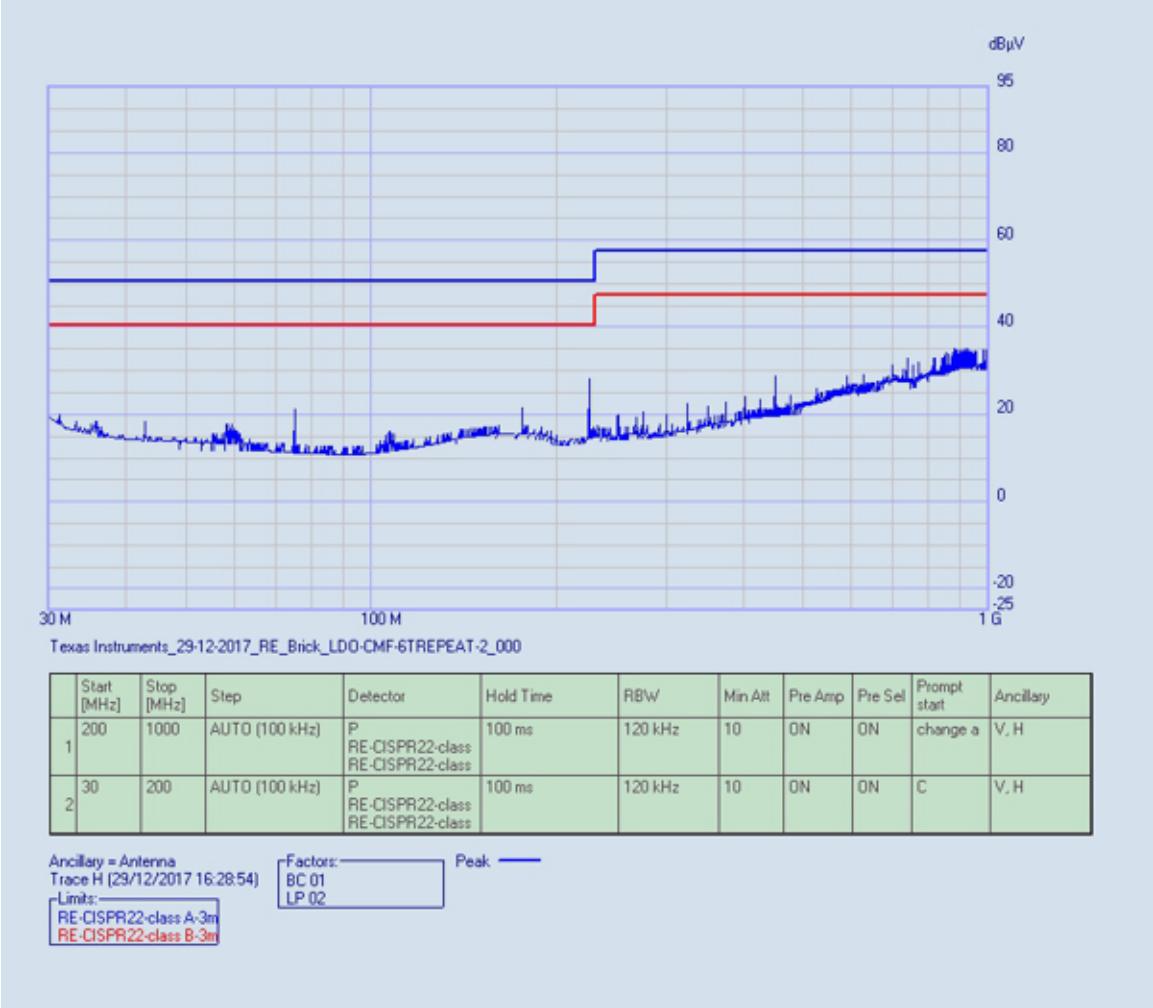
The radiated emission testing is done with the Ethernet brick communicating continuously with the computer. Disturbance field strength limits (quasi-peak) according to CISPR 11 / EN 55011 and CISPR 22 / EN 55022, normalized to a distance of 3 m. 図 28 shows the radiated emission plot with vertical polarization and peak measurement.



	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	200	1000	AUTO (100 kHz)	P RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	change a	V, H
2	30	200	AUTO (100 kHz)	P RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	C	V, H

図 28. Peak Measurements in Vertical Polarization

図 29 shows the radiated emission plot with horizontal polarization and peak measurement.



	Start [MHz]	Stop [MHz]	Step	Detector	Hold Time	RBW	Min Att	Pre Amp	Pre Sel	Prompt start	Ancillary
1	200	1000	AUTO (100 kHz)	P RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	change a	V, H
2	30	200	AUTO (100 kHz)	P RE-CISPR22-class RE-CISPR22-class	100 ms	120 kHz	10	ON	ON	C	V, H

図 29. Peak Measurements in Horizontal Polarization

4.5 Summary

表 29 summarizes the tests done and the observations gathered.

表 29. Test Results Summary for DP83822I or DP83822IF Ethernet Brick

SERIAL NUMBER	PARAMETERS	OBSERVATIONS
1	AVD analog power supply	OK
2	VDDIO I/O supply	OK
3	Communication testing with 1.8-V and 3.3-V AVD	OK
4	Clock	OK
5	MII to MCU	OK
6	Communication testing with TP (RJ45 copper)	OK
7	Communication testing with FO (SC interface)	OK
8	Communication testing with FO (ST interface)	OK
9	Radiated Emission Class A	OK
10	ESD	OK
11	EFT with continuous communication	OK
12	Surge	OK
13	Conducted susceptibility	OK
14	Radiated susceptibility	OK

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00928.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00928.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00928.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00928.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00928.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00928.

6 Related Documentation

1. Texas Instruments, *DP83848K PHYTER Mini LS Industrial Temperature Single Port 10/100 Ethernet Transceiver Data Sheet*
2. Texas Instruments, *Tiva™ C Series TM4C1294 Connected LaunchPad Evaluation Kit User's Guide*
3. Texas Instruments, *AN-1540 Power Measurement of Ethernet Physical Layer Products Application Report*
4. Texas Instruments, *How to Configure DP83867 SFDs Application Report*
5. Texas Instruments, *Ethernet Copper-to-Fiber Media Converter Reference Design for Substation and Distribution Automation Design Guide*
6. Texas Instruments, *TIDA-00496 10/100-Mbps Industrial Ethernet Brick With IEEE 1588 PTP Transceiver (Twisted Pair/Fiber) for Grid Infrastructure Applications Design Guide*
7. Texas Instruments, *EN55011-Compliant, Industrial Temperature 10/100-Mbps Ethernet PHY Brick Design Guide*
8. Texas Instruments, *32-Bit Arm® Cortex®-M4F MCU-Based Small Form Factor Serial-to-Ethernet Converter Design Guide*
9. Texas Instruments, *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver Data Sheet*
10. Texas Instruments, *EtherCAT® Slave and Multi-Protocol Industrial Ethernet Reference Design Guide*
11. Texas Instruments, *DP83822 10/100 Mbps Ethernet PHY Evaluation Module User's Guide*
12. Texas Instruments, *IEEE802.3bt Power Over Ethernet (PoE) Connected LED Lighting Reference Design Guide*

6.1 商標

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7 Terminology

SFF— Small form factor

FO— Fiber optic

TP— Twisted pair

8 About the Authors

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (September 2017) から **Revision C** に変更 **Page**

- 現行のデザイン・ガイド・テンプレートに合わせてレイアウトを更新 1
- 「特長」に事前認証テストの一覧を 追加 1
- Removed "ESD level" row from Table 1: *Ethernet Brick Design Features* 6
- "EMC" row to Table 1: *Ethernet Brick Design Features* 追加 6
- "Radiated emission" description from "EN55011, Class A" to "EN55011, Class B" in Table 1: *Ethernet Brick Design Features* 変更 6
- Section 4.3 from *EMC Pre-Compliance Testing* to *EMC IEC Pre-Compliance Testing* 変更 31
- more tests to Table 16: *EMC Tests* 追加 31
- Section 4.3.2: *IEC 61000-4-3 Radiated Immunity* 追加 32
- Moved Table 21: *EFT Test Observations* to the beginning of Section 4.3.3: *IEC 61000-4-4 EFT Test* 37
- tests 7 through 12 to Table 22: *Test Results Steps and Observations for EFT Testing* 追加 37
- Section 4.3.3.1: *Setup* 追加 37
- Section 4.3.4: *IEC 61000-4-4 EFT Test With Data Communication* 追加 37
- Table 23: *EFT Test With Data Communication Observations* 追加 37
- Section 4.3.5: *IEC 61000-4-5 Surge Immunity* 追加 41
- Section 4.3.6: *IEC 61000-4-6 Conducted Immunity* 追加 41
- Section 4.4 from *Radiated Emission Testing as per CISPR 22* to *Radiated Emission (EMI)* 変更 46
- Ethernet brick connections in Section 4.4.1: *Test Setup* 追加 46
- VDD supply configuration from 1.8 V to 3.3 V 変更 47
- Updated Figure 26: *Quasi-Peak Measurements in Vertical Polarization* 47
- Updated Figure 27: *Peak Measurements in Horizontal Polarization* 48
- Section 4.4.3: *Test Scan With VDD Supply Configured to 1.8 V and IO Supply Configured to 3.3 V* 追加 49
- Section 4.5 title from *Test Results Summary for DP83822I or DP83822IF Ethernet Brick* to *Summary* 変更 51
- serial numbers 12 through 14 to Table 29: *Test Results Summary for DP83822I or DP83822IF Ethernet Brick* 追加 51
- *Tiva™ C Series TM4C1294 Connected LaunchPad Evaluation Kit User's Guide* to Section 6: *Related Documentation* 追加 52
- *AN-1540 Power Measurement of Ethernet Physical Layer Products Application Report* to Section 6: *Related Documentation* 追加 52
- *Ethernet Copper-to-Fiber Media Converter Reference Design for Substation and Distribution Automation Design Guide* to Section 6: *Related Documentation* 追加 52
- *EN55011-Compliant, Industrial Temperature 10/100-Mbps Ethernet PHY Brick Design Guide* to Section 6: *Related Documentation* 追加 52
- *32-Bit Arm® Cortex®-M4F MCU-Based Small Form Factor Serial-to-Ethernet Converter Design Guide* to Section 6: *Related Documentation* 追加 52
- *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver Data Sheet* to Section 6: *Related Documentation* 追加 52
- *EtherCAT® Slave and Multi-Protocol Industrial Ethernet Reference Design Guide* to Section 6: *Related Documentation* 追加 52
- *IEEE802.3bt Power Over Ethernet (PoE) Connected LED Lighting Reference Design Guide* to Section 6: *Related Documentation* 追加 52

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- Corrected table title from *DP82822 Family Comparison* to *DP83822 Family Comparison* 8

2016年10月発行のものから更新 **Page**

- 現行のデザイン・ガイド・テンプレートに合わせて 変更 1

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