参考資料

TI Designs: TIDA-00976
高速、ハイサイド電流センスのリファレンス・デザイン

概要

TIDA-00976 TI Designは電流から電圧への高速変換回路です。このデザインは、5V～30Vの正の電源レールで高速な電流の測定を行う必要がある、電流センス・アプリケーションに最適化されています。このデザインは同相電圧を30Vから降圧し、2.5Vを中心とする出力電圧を生成して、アナログ/デジタル・コンバータ(ADC)によりサンプリングを行います。出力同相電圧は、さまざまな高精度基準電圧を使用して簡単に変更できます。

リソース

THS4131	プロダクト・フォルダ
TINA-TI™	ツール・フォルダ

TI E2E™ Community

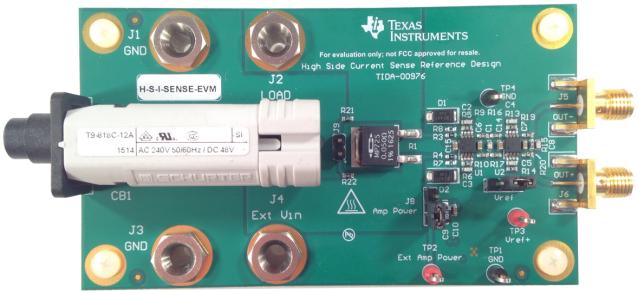
E2Eエキスパートに質問

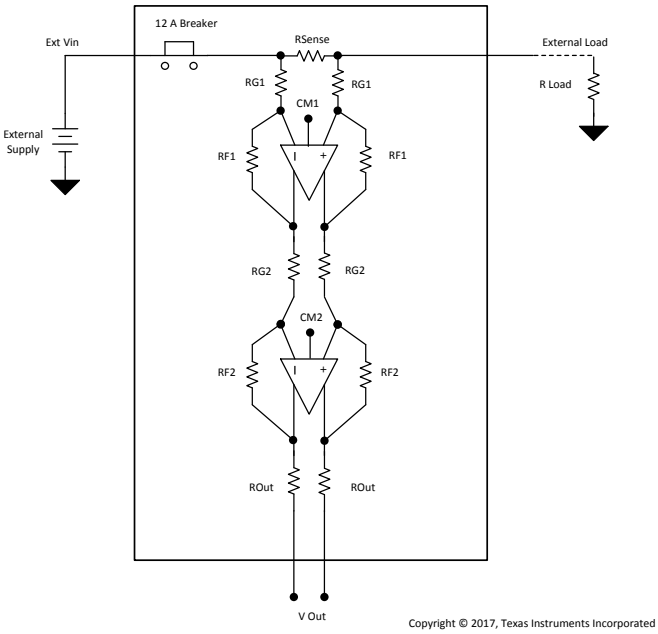
特長

- 帯域幅: 15MHz超
- 電流を電圧に変換
- ハイサイドの電圧範囲: 5～30V
- 柔軟な出力同相電圧

アプリケーション

- 電力品質測定器
- 無線周波数(RF)パワー・アンプ(PA)制御およびエンベロープ・トラッキング
- モータ制御
- 力率補正および測定





1 System Description

The TIDA-00976 TI Design is a fixed-gain, high-bandwidth, and fully-differential, current-to-voltage conversion circuit designed for high-speed applications. With a supply voltage range of 5 to 30 V, this amplifier provides exceptional flexibility in high-side current-sense applications. With an input voltage of 30 V and typical ADC input voltage ranges of 5 V or less, the TIDA-00976 uses a two-stage configuration to reduce the input voltage range to a safe range for a typical ADC. The TIDA-00976 has been optimized for high-input voltage and large currents. The TIDA-00976 uses two THS4131 high-speed, fully-differential amplifiers (FDAs) to convert an input current to output voltage.

Design options for higher supply voltage and additional filtering are provided to cover additional applications.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Supply voltage	5- to 30-V external supply
Current-to-voltage gain	100 to 400 mV_{PP}/ Amp
Differential-output common-mode voltage	2.5 V (adjustable)
Target bandwidth	> 15 MHz
Onboard active load	Vin = 5 to 30 V; Gain = 500 mV/A
Onboard circuit breaker	12 A

2 System Overview

2.1 Block Diagram

A block diagram of the system is shown in 図 1. The main portion of the design is two fully-differential amplifiers (FDAs). A circuit breaker and a precision reference are included on the reference design board. There is also a connector for an external load.

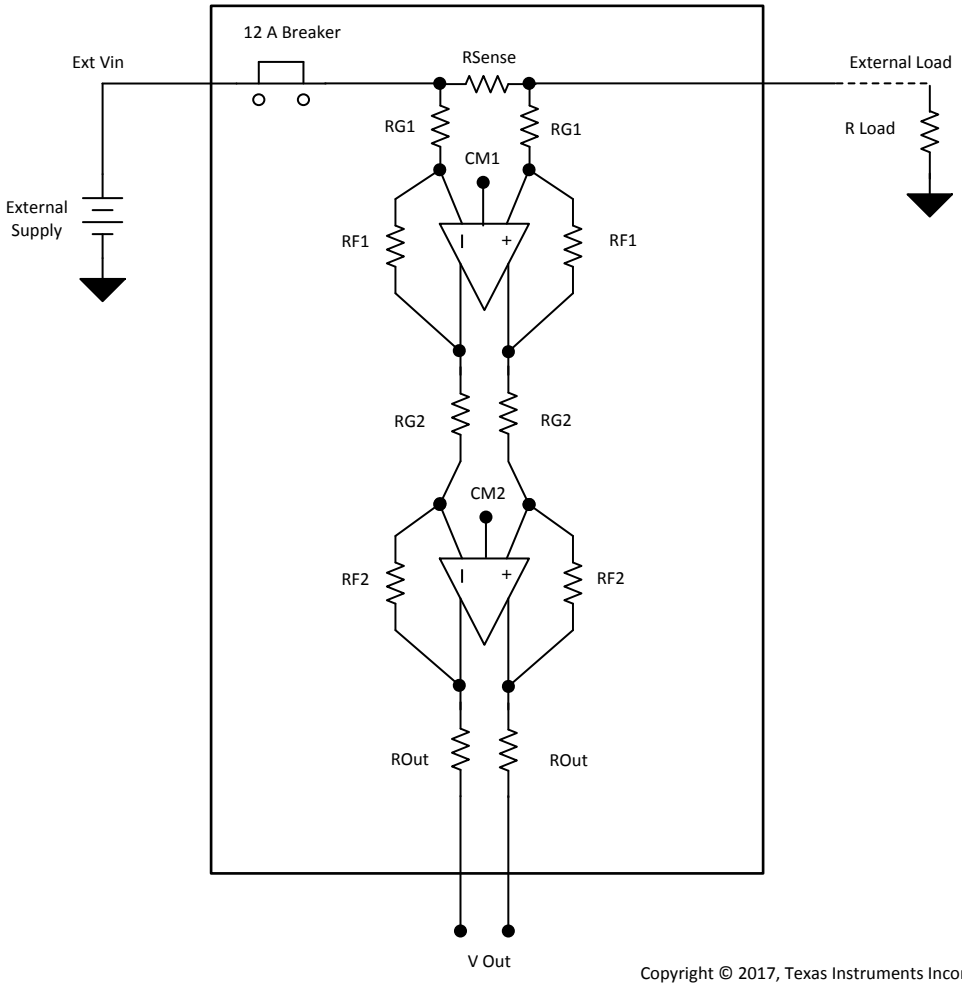


図 1. System Block Diagram

2.2 Design Considerations

Voltage calculations at key points in the signal path are annotated in 図 2.

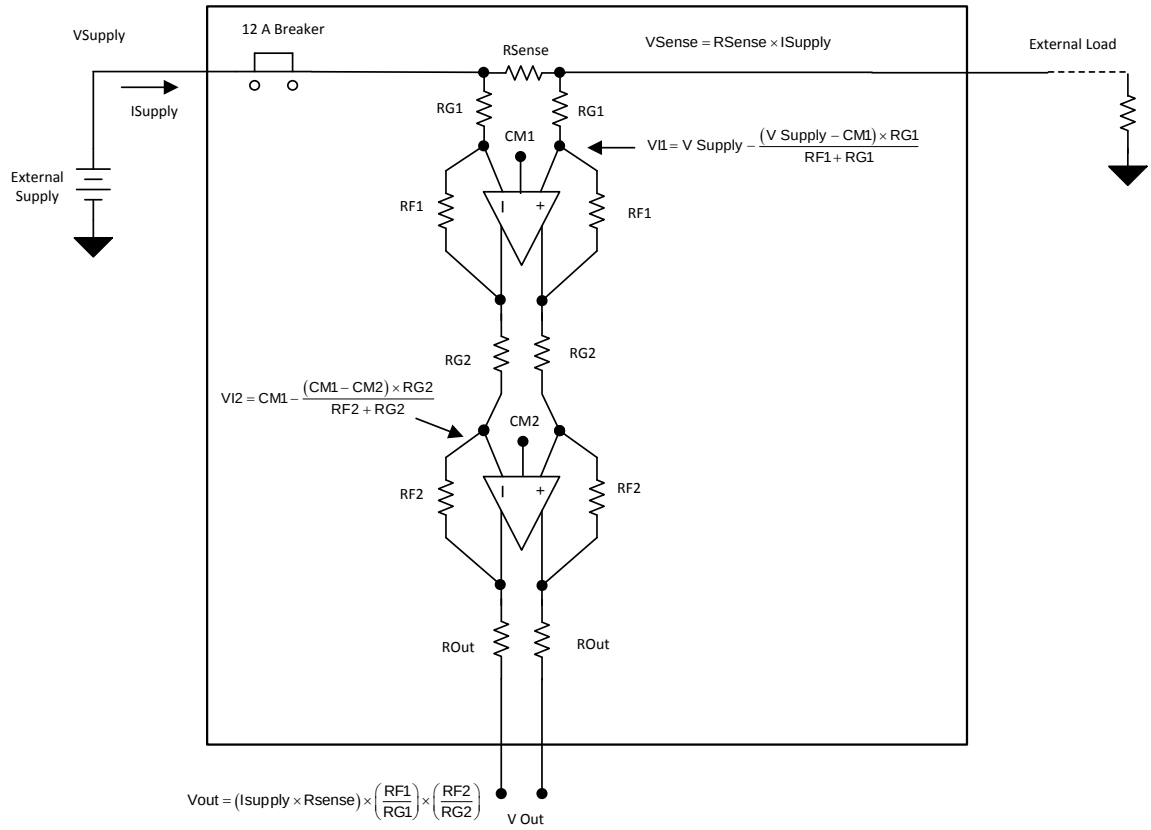


図 2. Detail of Common-Mode Voltages and Design Equations

2.3 Highlighted Products

2.3.1 THS4131

This TI Design features the THS4131 FDA. The THS4131 provides an excellent combination of wide supply range, high speed, and low noise, which makes it ideally suited for high-side, current-sense applications. The THS4131 has externally set gain with four resistors.

In addition to a wide supply-voltage range, the THS4131 also has a very wide input common-mode range. The input common-mode voltage can range from (V- + 1.0 V) to (V+ - 0.5 V). This wide input common-mode range allows flexibility for current sensing from the positive supply rail.

The common-mode rejection ratio (CMRR) provided by the fully-differential signal chain reduces any feed-through from the power supply regulator voltage fluctuations, which increases the power-supply rejection ratio (PSRR) of the current-sense circuit.

2.3.2 REF5025AID

The REF5025 is a 2.5-V, low-noise, precision voltage reference. This reference is used to set the output common-mode voltage. The REF50xx series offers several voltage options if required for different ADC common modes.

2.4 System Design Theory

The design of TIDA-00976 is a high-side, current-sensing circuit. In a high-side, current-sense system the sense resistor is between the power supply and the circuit. The primary advantage of a high-side, current-sense circuit is that the ground path is undisturbed. Many systems use ground connections to suppress noise and power-supply voltage transients, so the high-side, current-sense option is desirable. The primary drawback of high-side, current-sense circuits is that the supply voltage is now the common-mode voltage of the sense voltage generated on the sense resistor. This reference design uses a THS4131 FDA with an input common mode that can support supply voltages up to 30 V.

An FDA with wide bandwidth is the core of the signal path as shown in 図 2. In order to support the full supply range of 30 V while also driving a low-voltage ADC, there is a second FDA on the reference design board. If the external VSupply voltage is less than 7 V, the second amplifier may not be necessary. A detail of the common-mode voltages is shown in 図 2.

In addition to a wide supply-voltage range, the TIDA -00976 also offers a very high frequency response. Without filtering, the core design supports bandwidths up to 15 MHz. This frequency response can be tailored for the specific application with additional components.

2.4.1 Design Options

There are several options built into the TIDA-00976 reference design. These options are shown in 図 3, which help extend the voltage range and ensure stability of the final circuit.

The first option is the addition of pull-down resistors, which are labeled RB1. These resistors will reduce the amplifier input common-mode pin voltages and allow for an input voltage higher than 30 V to be applied to the external supply port.

To protect the amplifier inputs from voltage transients in a high-noise environment, placeholders for Zener diodes are provided as shown in 図 3. The reverse-bias rating on the diodes should be rated for at least the maximum supply voltage or 30 V. The addition of the reverse-biased Zener diode might present significant input capacitance that causes frequency-response peaking or instability. As a result, the capacitors CC1 can be used to reduce peaking of the frequency response. A good starting value for this component is 1 pF to 5 pF. A detailed description of stabilizing an amplifier by the addition of an input capacitance can be found in the *Op amp stability and input capacitance*[2].

In order to reduce sampled noise when using an ADC to measure the system output, the system bandwidth should not be significantly larger than the signal bandwidth. The TIDA-00976 has over 15 MHz of bandwidth. If the sampled signal has lower bandwidth, capacitors CF1 and CF2 can be used to reduce broadband noise.

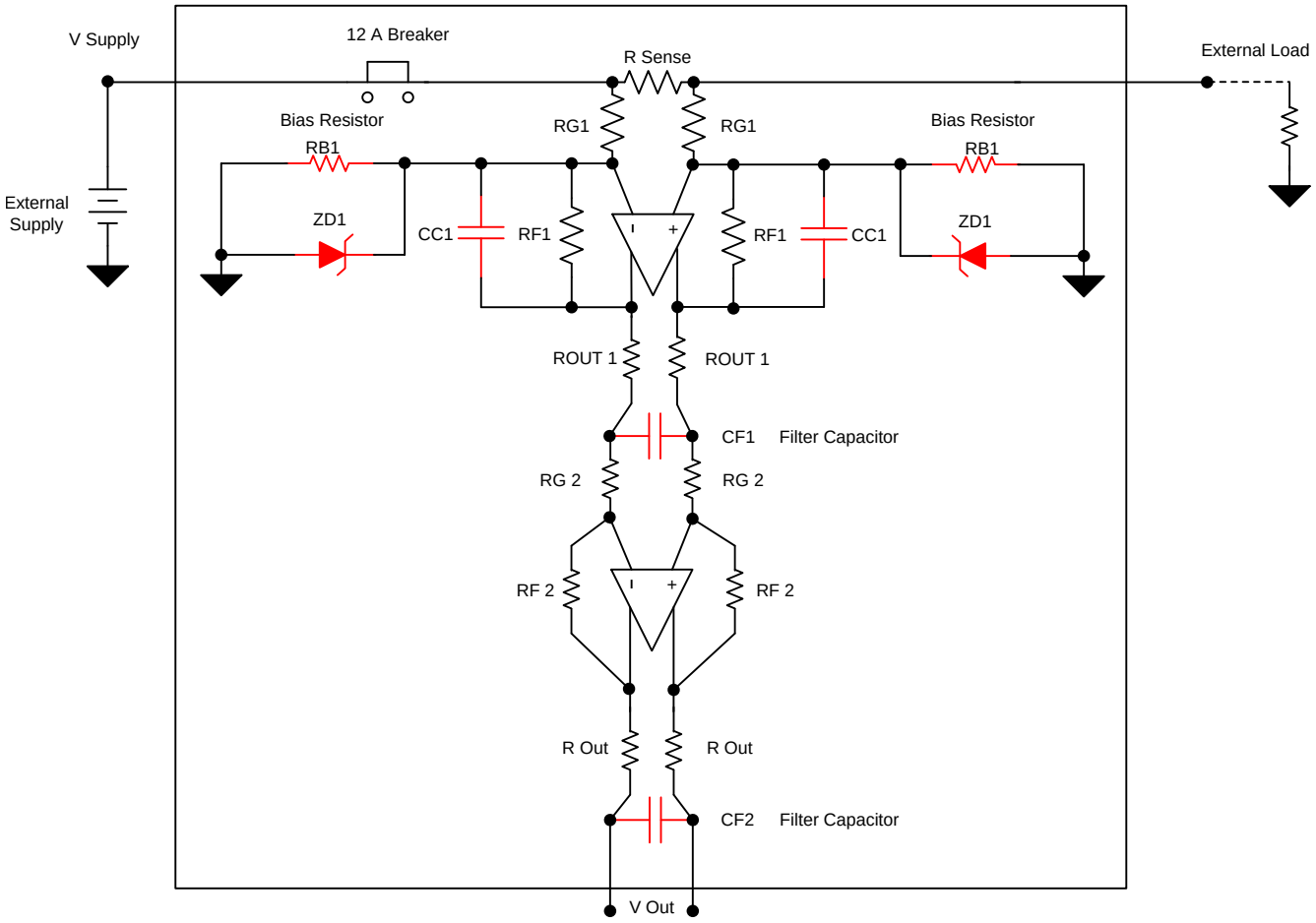


図 3. Design Options Shown in Red

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Hardware

CAUTION

Caution hot surface. The PCB surface can get very hot while passing high currents. Contact may cause burns. Do not touch

The performance of the TIDA-00976 was evaluated by simulation in TINA-TI as well as in the lab using an external load. 図 4 shows the hardware setup diagram for evaluating the reference design for converting a high-side input current to an output voltage.

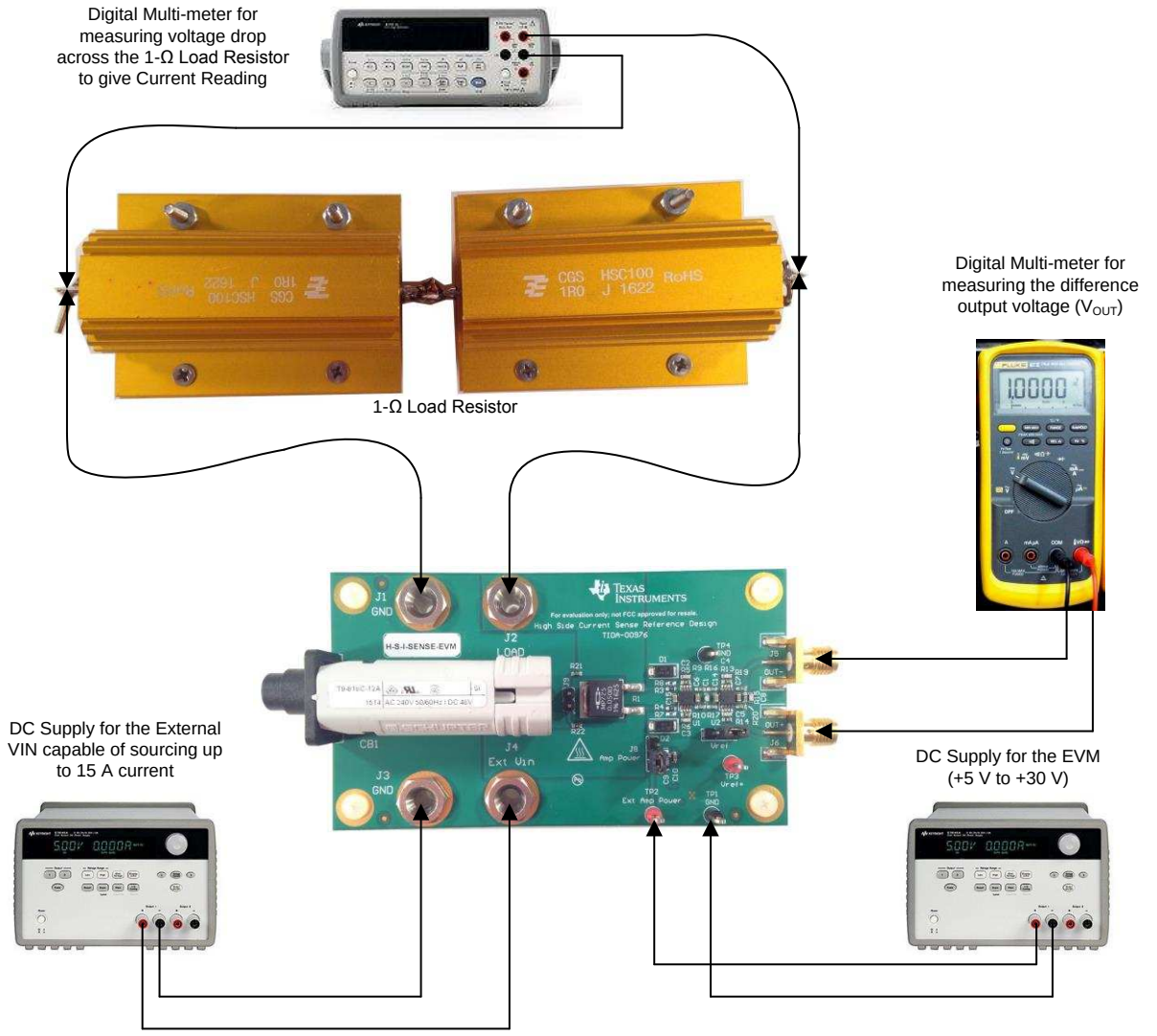


図 4. Hardware Setup Diagram

3.1.1 Applying Power and Basic Setup

The TIDA-00976 has a supply voltage range of 5 to 30 V. The following steps detail the TIDA-00976 setup procedure for high-side input current to output voltage testing, as shown in 図 4.

3.1.1.1 Board Power Supply Setup

The TIDA-00976 reference design supports a supply voltage range of 5 to 30 V.

1. With the supplies disconnected, set the voltage on the DC power supply (capable of souring 1-A current) between 5 to 30V. Also, set the current compliance limit to approximately 100 mA on the DC power supply.
2. Keeping the supplies turned OFF, connect the DC power supply to the EXT amp power connection (TP2) and GND (TP1) as shown in 図 4. Reference the 図 7 for test-point (TP) and jumper connections. Make sure the shorting block on jumper J8 is connected across pins 1 and 2.
3. Turn on the DC power supply connected to the external amp power connector. The supply current recorded on the power supply should be around 27 mA.

3.1.1.2 Connecting the Digital Multimeter to Measure the Output Voltage

1. Connect the digital multimeter voltage port to OUT+ (J6) and COM port to OUT- (J5), as shown in 図 4.
2. Set the dial on the multimeter to DC voltage measurement mode. The multimeter measures the voltage difference across the outputs OUT+ and OUT-.

3.1.1.3 Connecting the External High-Current Load and High-Current Testing

1. Connect a high-current, 1-Ω load resistor bank across the connectors J1 (GND) and J2 (LOAD). Ensure that the connector cable is rated for 15 A (14 gauge or larger). The voltage measurement across the 1-Ω load resistor bank is equivalent to the load current being measured.
2. Connect another digital multimeter voltage port across the 1-Ω load resistor bank to measure the voltage across it, as shown in 図 4.
3. With the supplies turned OFF, connect a high-current bench supply capable of sourcing 15-A current across connectors J4 (external Vin) and J3 (GND). Ensure that the connecting cable is rated for at least 15 A.
4. Turn on the DC power supply connected to the external Vin responsible for providing the input load current. 図 5 gives the relationship between the input load current and the output voltage measured across the outputs OUT+ and OUT-.

3.1.2 Output Common-Mode Voltage Option

In order to support direct interfacing with an ADC, the TIDA-00976 reference design uses a precision reference (REF5025AID) to set the common-mode voltage of U2. This precision reference allows direct DC coupling with ADCs that require a 2.5-V input common-mode voltage. Options ranging from 2 to 10 V are available in the REF50xx family of precision voltage references.

In the event that another common-mode voltage is desired, move the shorting block on jumper J7 across pins 1 and 2. Connect the Vref+ test point to a bench supply and set the voltage to the desired common-mode voltage. The valid common-mode voltages range from 1 V to (Vs+ - 1 V) for the THS4131.

3.2 Testing and Results

3.2.1 High-Side Current Testing

3.1.1 details the setup procedure for high-side current testing. 図 5 shows the linear relationship between the measured input load current and the output voltage across OUT+ and OUT- or V_{OUT} = (OUT+) - (OUT-).

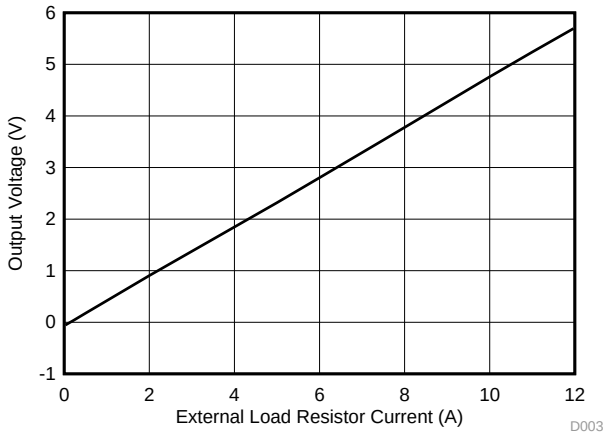


図 5. Output Voltage Versus Load Current

3.2.2 Frequency Response Testing

In order to measure the frequency response without having to source and sink a large current, a differential signal input can be inserted at jumper J9. Replace resistor R1 with a 100-Ω resistor and connect a differential voltage source across J9. The frequency response of the reference design can now be measured with standard 100-Ω differential test equipment. 図 6 shows the frequency responses of the two-stage current-sense circuit.

The filtered frequency response in the below graph includes the diode protection circuit at the input (ZD1) along with CC1 of 5pF (see 図 3). The protection diode used in the circuit is the SMAZ30-13-F with approximately 60 pF of reverse bias capacitance. Also, the CF1 and CF2 are set to 10 pF and 30 pF, respectively. The unfiltered frequency response test is performed by removing all the above mentioned components used for the filtered frequency response.

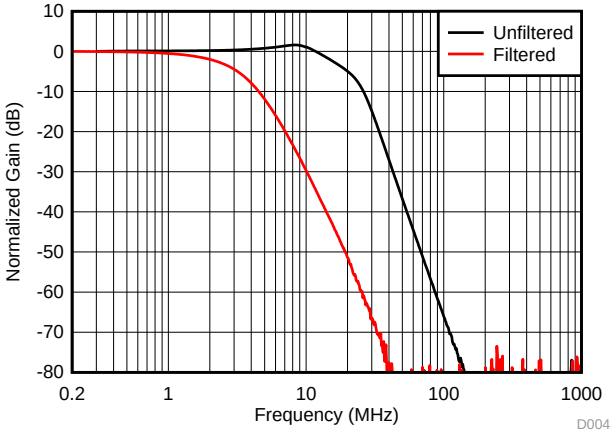


図 6. Measured Frequency Response

3.2.3 Common-Mode Voltage Versus Error Current

Due to the high voltages involved, it is important to calculate the power dissipated in the first stage feedback and gain-set resistors. Power dissipation for typical configurations is shown in 表 2. It is important to note that for a given voltage the resistor power will increase as the resistor value decreases. For this reason, there is a trade-off between selecting low resistor values to reduce noise compared with increased power dissipation. When using surface mount resistors, some typical resistor power ratings are shown in 表 3.

表 2. Common-Mode Voltage Versus Error Current

SUPPLY VOLTAGE (V)	ADC INPUT COMMON MODE (V)	CM1 (V)	CM2 (V)	RG1 (Ω)	iRG1 (mA)	pRG1 (mW) / pRF1 (mW)
5	2.5	2.5	2.5	5k	0.17	0.14 / 0.29
7	2.5	3.5	2.5	5k	0.3	0.45 / 0.9
10	2.5	5	2.5	5k	0.33	0.54 / 1.1
15	2.5	7.5	2.5	5k	0.5	1.25 / 2.5
20	2.5	10	2.5	5k	0.67	2.24 / 4.49
30	2.5	15	2.5	5k	1	5 / 10

表 3. Surface Mount Resistor Power Ratings (1)

PACKAGE SIZE	POWER RATING (mW)
0603	125
0402	63
0201	50

(1) Vishay®

3.2.4 Signal Gain Calculation

The current-to-voltage signal gain calculation as well as the common-mode voltage at various nodes in the circuit are shown in 図 2. The individual stage gain is mainly set by the ratio of feedback resistor (RF) and gain-setting resistor (RG). In actual application, the second FDA output interfaces to a low-voltage ADC. As a result, the maximum input voltage swing of the ADC usually sets the maximum signal current that is measured for a given sense resistor and overall gain configuration. 表 4 shows the maximum signal current that can be measured for 3 V_{PP} maximum input at the ADC for the different sense resistor and gain configurations.

表 4. Signal Gain (V/A)

SENSE RESISTOR (Ω)	STAGE 1 GAIN (V/V)	STAGE 2 GAIN (V/V)	OVERALL GAIN (mV/A)	SUPPLY DROOP (mV/A)	MAX. CURRENT (A) at 3 V_{PP}
0.100	2	2	400	100	7.5
0.050	2	5	500	50	6
0.010	2	5	100	10	30
0.010	4	4	160	10	19

3.2.5 Noise and Offset Errors

The primary offset error and noise terms are shown in 表 5 and 表 6, respectively. While the offset voltage and offset currents are the largest terms, they are also systematic and can be calibrated out from the final measurements. It is the noise terms that cannot be calibrated out due to the randomness associated with the noise. For high-side current-sense applications, the input gain-setting resistor (RG) must be high in order to minimize error currents while applying high-input voltages as discussed in 3.2.3. As a result, the large gain (RG) and feedback resistors (RF) have noise that is significantly more than the amplifier noise. An RG of 5 kΩ has a thermal noise of 9 nV/√Hz, while the amplifier input-noise voltage is 1.3 nV/√Hz. A detailed description of calculating noise in a fully-differential amplifier can be found in the *Analysis of fully differential amplifiers*[3].

表 5. Input Referred Offset Error Terms

PARAMETER	V_{OS}	I_{OS}
Value	0.2 mV	100 nA
Error magnitude with Rg = 5kΩ, A_V = 2 V/V BW = 20MHz	0.4 mV	0.33 mV

表 6. Input Referred Noise Error Terms

PARAMETER	V_N	I_N	RG_Noise (1)
Value	1.3 nV/√Hz	1 pA/√Hz	5 kΩ
Error magnitude with Rg = 5kΩ, A_V = 2 V/V BW = 20MHz	5.8 uV RMS	22 uV RMS	40.5 uV RMS

(1) Thermal Noise = √4kTRG

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00976. 図 7 shows the schematic diagram for the reference design.

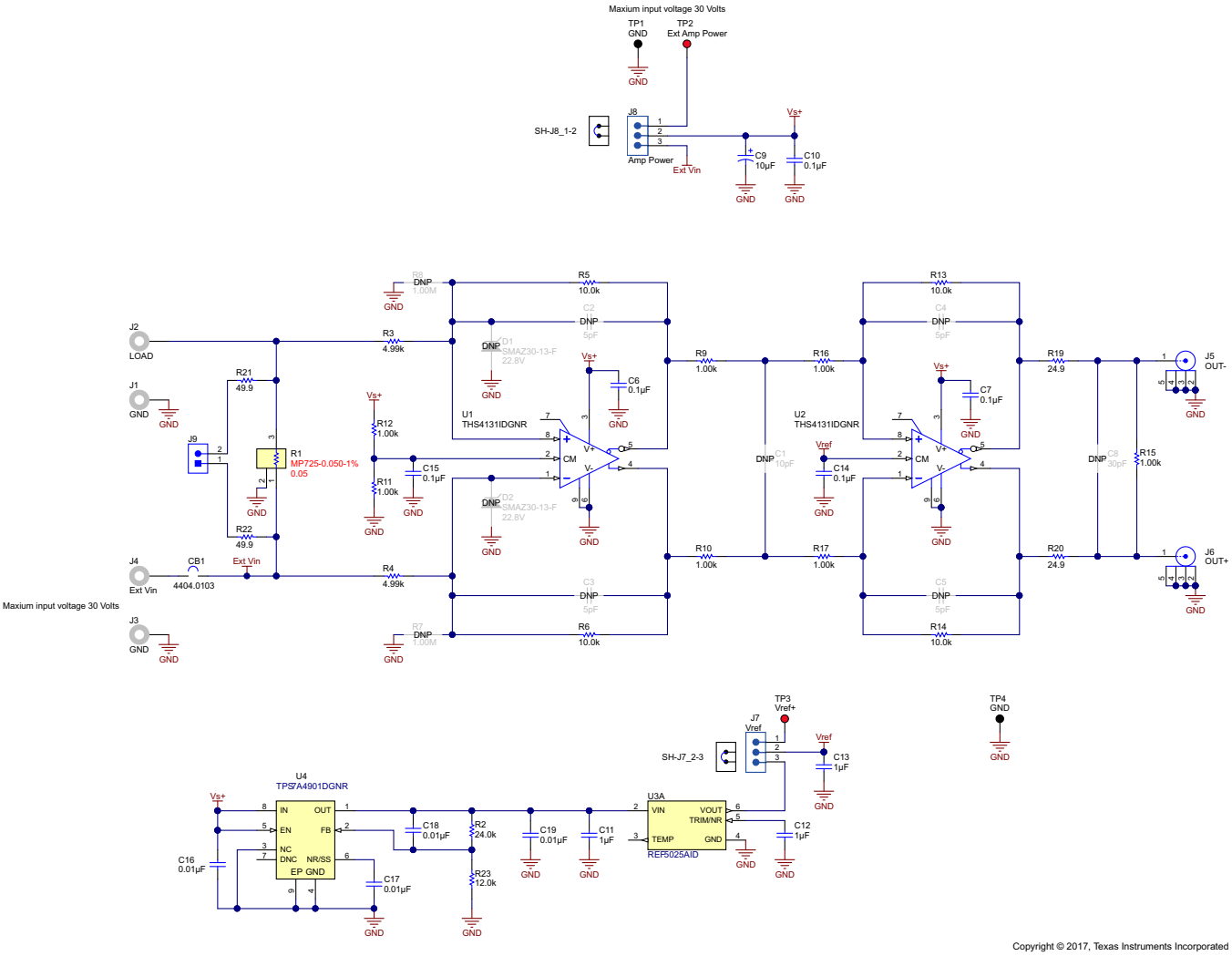


図 7. Schematic Diagram

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00976.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00976.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00976.

4.5 Layout Guidelines

図 8 shows the layout guidelines for this TI Design. The design is built on a four-layer FR-406 dielectric with the layer stackup as shown in 図 9. The sense resistor for measuring load currents is placed symmetrically between the first THS4131 inputs. Traces carrying the load current to be measured have their widths adjusted for maximum current of 20 A on 2-oz copper thickness.

For layout guidelines related to the THS4131, refer the layout section in the *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*[1].

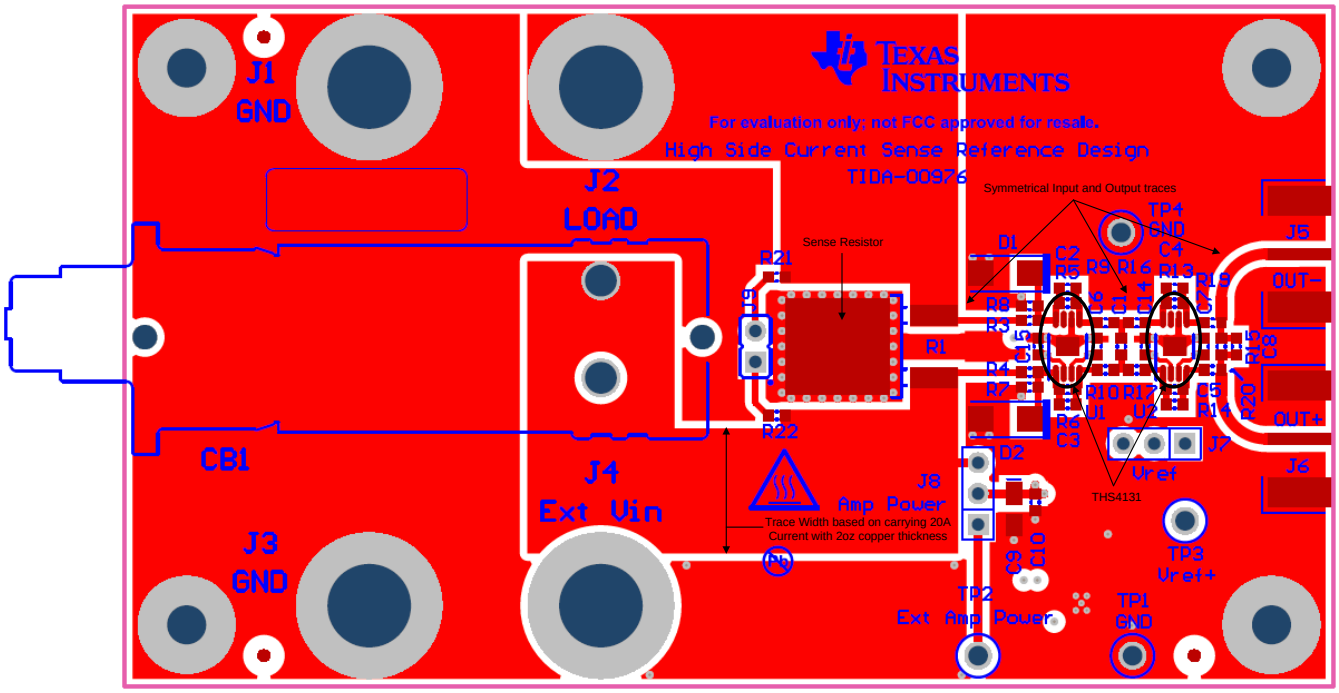


図 8. Example Layout (Top Layer)

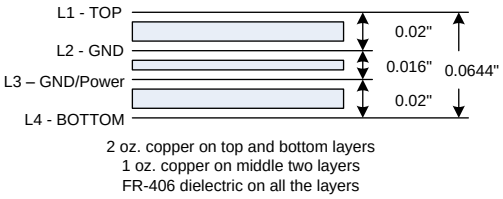


図 9. Layer Stackup

4.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00976.

4.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00976.

5 Related Documentation

1. Texas Instruments, *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*, THS4130 and THS4131 Datasheet (SLOS318)
2. Texas Instruments,*Op amp stability and input capacitance*, Technical Brief (SLYT087)
3. Texas Instruments, *Analysis of fully differential amplifiers*, Technical Brief (SLYT157)
4. Vishay Corporation, Vishay Resistors

5.1 商標

6 About the Author

LOREN SIEBERT is an applications engineer with TI in the High-Speed Amplifier division in Fort Collins, Colorado. He supports applications ranging from 4G and 5G radio base stations to precision, high-accuracy ADC drivers.

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TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

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