参考資料

TI Designs: TIDA-01461
EtherCAT P® (1本のケーブルで電源供給とEtherCAT®通信に対応)のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、EtherCAT P®電源装置の回路における電源結合の物理的実装を示すものです。また、これを使用してEtherCAT Pケーブルから電源を結合することもできます。このリファレンス・デザインは、公式EtherCAT P実装ガイドの要件をすべて満たすように設計されています。逆極性保護、突入電流制限、連続電流制限など、いずれもテキサス・インスツルメンツの半導体をベースにした保護機能を搭載しています。

EtherCAT Pは、EtherCAT®通信と電源供給を1本のケーブルに統合するものです。4線式ケーブルで、独立した2系統の24V/最大3Aの電源を提供し、同じケーブルでEtherCATデバイス間のデータ通信も行えます。これにより、工場におけるEtherCATネットワーク・デバイスの据付・配線コストを削減することができます。

EtherCAT通信に関しては、イーサネット・ケーブルを使用して、AMIC110産業用通信エンジン(ICE)などのEtherCAT対応通信プラットフォームに接続できます。電源供給機能については、EtherCAT Pケーブルを使用して、2つの設計基板を接続できます。EtherCATマスタを一方のリファレンス・デザインに、EtherCATスレーブをもう一方のリファレンス・デザインに接続することで、完全なEtherCAT Pデモンストレーション・システムが実現します。

リソース

TIDA-01461	デザイン・フォルダ
LM5050-1	プロダクト・フォルダ
CSD18540Q5B	プロダクト・フォルダ
LM5069	プロダクト・フォルダ
TPD2E2U06	プロダクト・フォルダ
LMZ35003	プロダクト・フォルダ
TVS3300	プロダクト・フォルダ
AMIC110 ICE	ツール・フォルダ

TI E2E™ Community

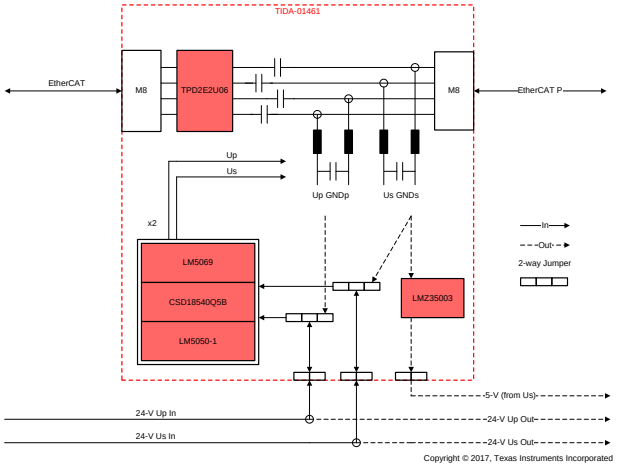
E2E™エキスパートに質問

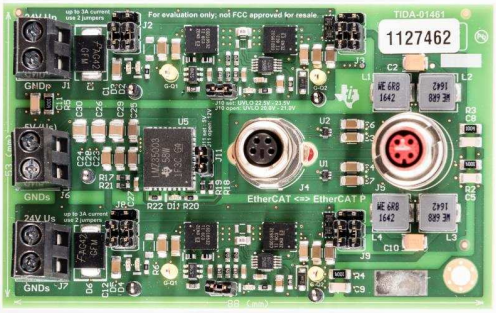
特長

- EtherCAT®通信と電源供給を1本のケーブルに統合
- EtherCAT P®実装ガイドの要件を満たすように設計
- 逆極性保護
- 突入電流制限および連続電流制限
- 可変過電圧/低電圧誤動作防止
- イーサネット・ケーブルを使用してEtherCAT通信プラットフォームに接続可能
- 追加の5V/12V出力により、テキサス・インスツルメンツのAMIC110 ICEを使用した評価が容易

アプリケーション

- リモートIO
- 通信モジュール
- リモート・センサおよびアクチュエータ
- モータ・ドライブ





1 System Description

This reference design implements the power couple in circuitry of an EtherCAT P® power sourcing device (PSD), meaning that the actual EtherCAT® communication controller, PHY, and Ethernet transformer are not part of the design. To connect an EtherCAT communication platform, the board has an Ethernet connector assembled. To connect two design boards, an EtherCAT P connector is assembled.

The reference design is designed to meet the requirements specified in the *EtherCAT and EtherCAT P Slave Implementation Guide* from the EtherCAT technology group.

EtherCAT P combines EtherCAT communication and power transfer on one cable. Four wires provide two isolated power supplies, named Us and Up, each providing 24 V and up to 3 A. The isolation rating between the two power rails must be at least 500 V. The isolation rating of the two power rails against field earth or protected earth is 500 V as well.

The same four wires used for power transfer are used for EtherCAT communication. To couple power in to the data lines, this design uses one second-order LC filter per 24-V supply that act as a low-pass filters. To block the 24 V from the Ethernet transformer, one additional capacitor per data line is put in series between the Ethernet transformer and the power couple in circuitry. This circuitry couples power in as well as couples power out.

Us powers the system of an EtherCAT P device (for example, its EtherCAT communication controller, PHYs, microcontrollers, supervisors, and so on, as well as all internal and external sensors). Up powers all internal and external actors like motors or relays. This separation is useful for systems that need two independent power supplies. Furthermore, it gives for example the ability to shut down the motor of a system while still being able to monitor sensor outputs and transmit data to an EtherCAT master.

An EtherCAT P PSD must fulfill several requirements for Us and Up before those power rails are coupled in to the data lines. 表 1 lists these requirements and they can also be read in the official EtherCAT P implementation guide [1] . This implementation guide also gives detailed information about the EtherCAT P technology itself.

This reference design implements the protection features of a PSD, such as reverse polarity protection, in-rush current limit, current limit, undervoltage lockout (UVLO), and overvoltage lockout (OVLO) with semiconductor components. In this design guide and the schematic, this part is called "power input protection". This block exists for both Us and Up.

For EtherCAT communication, the reference design can be connected to an EtherCAT capable communication platform like the AMIC110 ICE with an Ethernet cable at connector J4. Two reference design boards can be connected with an EtherCAT P cable at connector J5. Connecting an EtherCAT master to the first reference design and an EtherCAT slave to the second reference design results in a complete EtherCAT P demonstration system.

Note that to couple power in, connectors J2, J3 for Up and J8, J9 for Us must be set according to the mode, couple in - couple out, which is used in this reference design. This mode can be set with two jumpers per connector. To couple power in, connect pins 3–5 and 4–6. To couple power out, the two jumpers must connect pins 3-1 and 4-2 of the connectors. With this, it is possible to use the reference design for both couple in and couple out. The input voltage for Up is connected at J1, and the input voltage for Us is connected at J7. The output voltages are available at the same connectors.

To facilitate the usage of the AMIC110 ICE, an additional 5-V buck module is available on the board. Following the implementation guide, this 5-V supply is derived from the Us power rail. In case a 12-V output is needed, remove jumper J11 to change the feedback voltage of the LMZ35003 buck module, which results in an output voltage of 12 V. The LMZ35003 buck module is not part of the actual EtherCAT P implementation.

1.1 Key System Specifications

Unless specified otherwise, all parameters are valid for both 24-V power rails, Us and Up.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input supply voltage	24 V + 20%, – 15%	2.3.2.1
Maximum continuous current	3 A	2.3.2.3
Maximum peak current	7 A	2.3.2.5
Undervoltage lockout (UVLO)	23.0 V to 23.5 V, adjustable to 20.4 V to 20.9 V with jumper J10	2.3.2.1
Overvoltage lockout (OVLO)	28.0 V to 28.8 V	2.3.2.1
Isolation voltage rating (Us-Up)	500 V	1
Isolation voltage rating (Us: PE/FE and Up: PE/FE)	500 V	1
V_{out} of LMZ35003	5 V, adjustable to 12 V with jumper J11	1
I_{out} of LMZ35003	2.5 A	2.2.5

2 System Overview

2.1 Block Diagram

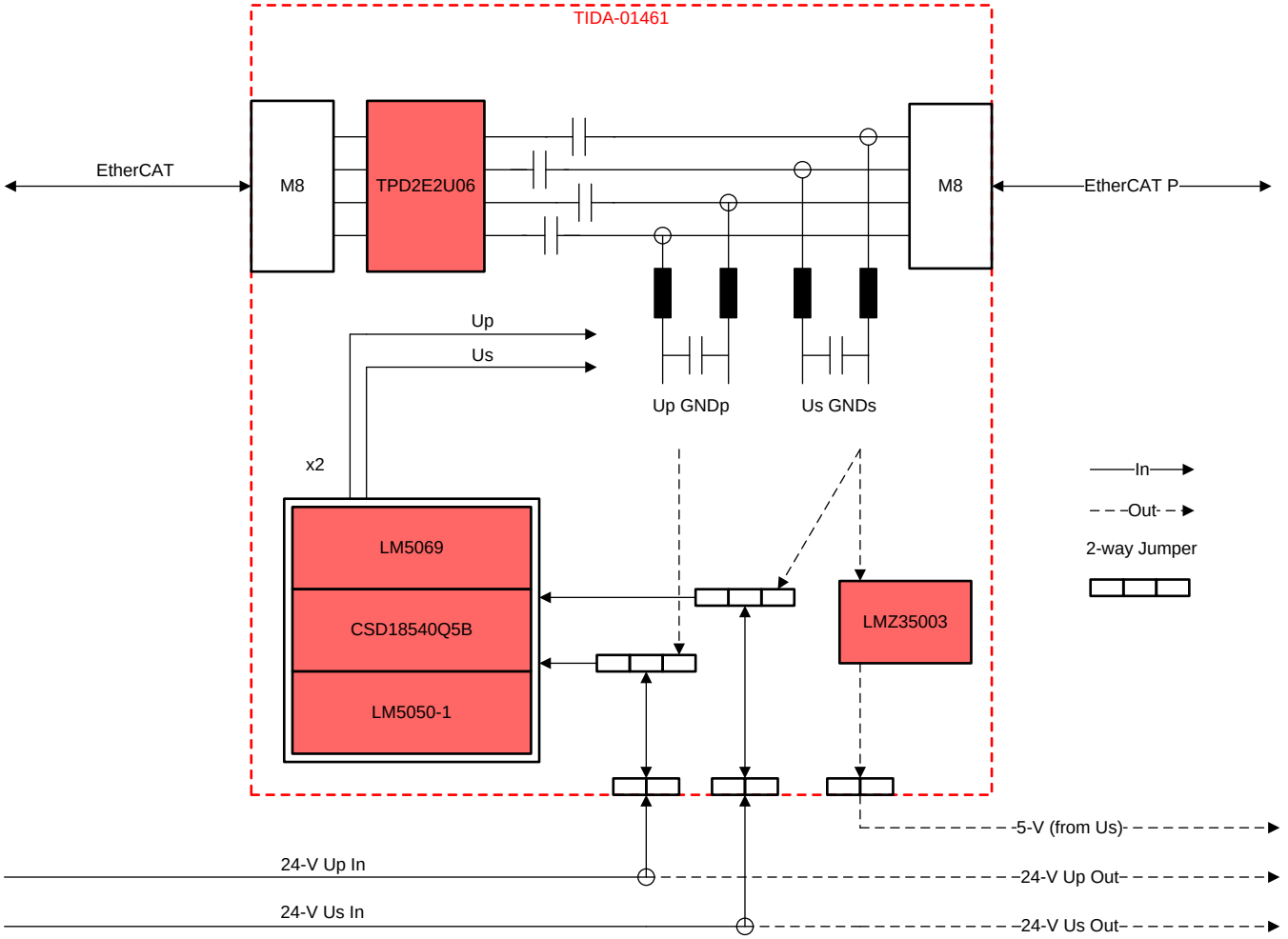


図 1. Block Diagram of TIDA-01461

2.2 Highlighted Products

2.2.1 LM5050-1

The LM5050-1/LM5050-1 High Side OR-ing FET Controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5050-1/LM5050-1 controller provides a MOSFET gate drive with charge pump for an external N-Channel MOSFET and a fast response comparator to turn off the MOSFET when current flows in the reverse direction. The LM5050-1 can connect power supplies ranging from 5 V to 75 V and can withstand transients up to 100 V.

2.2.2 CSD18540Q5B

This 1.8-mΩ, 60-V, NexFET™ power MOSFET minimizes losses in power conversion applications with a SON 5-mm × 6-mm package.

2.2.3 LM5069

The LM5069 positive hot swap controller provides intelligent control of the power supply connections during insertion and removal of circuit cards from a live system backplane or other hot power sources. The LM5069 provides in-rush current control to limit system voltage droop and transients. The current limit and power dissipation in the external series pass N-Channel MOSFET are programmable, ensuring operation within the safe operating area (SOA). The POWER GOOD output indicates when the output voltage is within 1.25 V of the input voltage. The input UVLO and OVLO levels and hysteresis are programmable as well as the initial insertion delay time and fault detection time. The LM5069-1 latches off after a fault detection, while the LM5069-2 automatically restarts at a fixed duty cycle. The LM5069 controller is available in a 10-pin VSSOP package.

2.2.4 TPD2E2U06

The TPD2E2U06 is a dual-channel, low-capacitance TVS diode ESD protection device. The device offers ±25-kV contact and ±30-kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I^2C™.

2.2.5 LMZ35003

The LMZ35003 SIMPLE SWITCHER® power converter is an easy-to-use integrated power solution that combines a 2.5-A DC/DC converter with a shielded inductor and passives into a low-profile, QFN package. This total power solution allows as few as five external components and eliminates the loop compensation and magnetics part selection process.

2.2.6 TVS3300

The TVS3300 is a transient voltage suppressor that provides robust protection for electronic circuits exposed to high transient voltage events. Unlike a traditional TVS diode, the TVS3300 precision clamp triggers at a lower breakdown voltage and regulates to maintain a flat clamping voltage throughout a transient overvoltage event. The lower clamping voltage combined with a low dynamic resistance enables a unique TVS protection solution that can lower the voltage a system is exposed during a surge event by up to 30% in unidirectional configuration and up to 20% in bidirectional configuration when compared to traditional TVS diodes.

2.3 System Design Theory

図 2 shows the system block diagram of this reference design in combination with an EtherCAT communication platform, here the AMIC110 ICE from Texas Instruments.

This reference design is only used to couple power in and couple power out from the EtherCAT data lines. Therefore, two boards must be connected to two EtherCAT devices. In case the EtherCAT slave is supposed to feed power further along a line network, another board can be connected to couple power in again. This application is also tested in 3.2.1.2.

Before Us and Up are coupled in to the data lines, both voltages need to pass the power input protection circuitry. This circuitry makes sure that the voltages are applied correctly, are within the allowed voltage levels, and that the maximum continuous current is not exceeded. These features are explained in more detail in the following subsections.

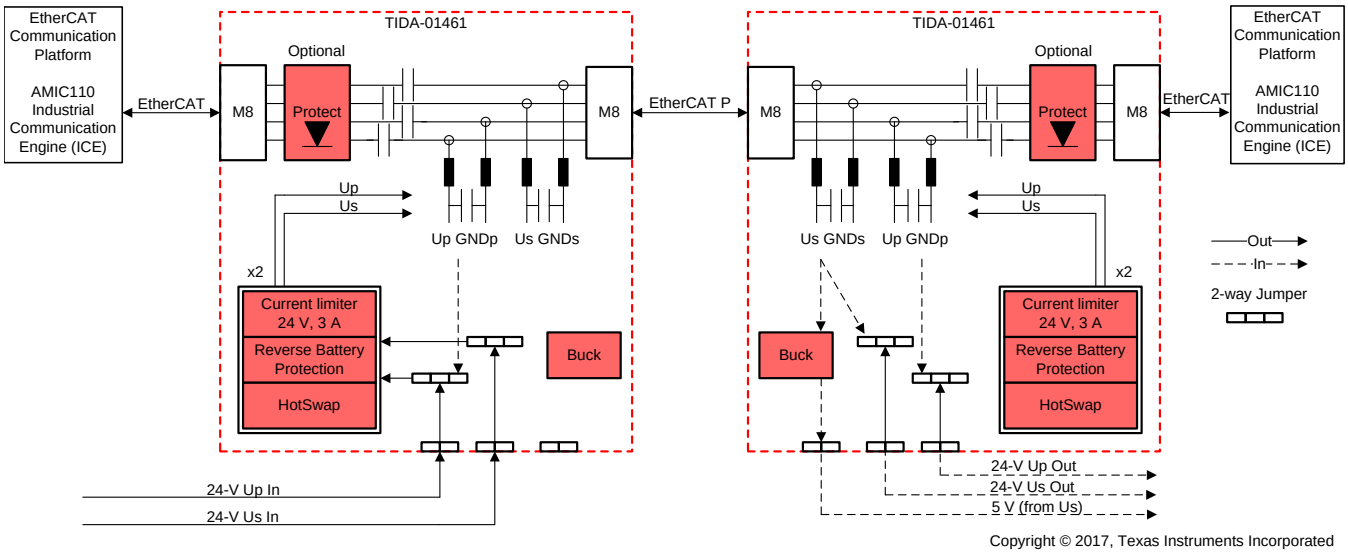


図 2. System Block Diagram With Two AMIC110 ICEs and Two TIDA-01461 Boards

2.3.1 Reverse Polarity Protection

Reverse polarity protection is realized with the LM5050-1 and MOSFET Q1. 図 3 shows the relevant part of the schematic. In case the voltage is applied in a reverse way, Q1 stays in a high-impedance mode. In case the voltage is applied correctly, the LM5050-1 works as follows:

The LM5050-1 regulates the gate-to-source voltage of MOSFET Q1. If the MOSFET current decreases to the point that the voltage across the MOSFET falls below the voltage regulation point of 22 mV (typical), the GATE pin voltage decreases until the voltage across Q1 is regulated at 22 mV. If the source-to-drain voltage is greater than 22 mV, the gate-to-source voltage increases and eventually reaches the Zener clamp level of the 12-V GATE to IN pin.

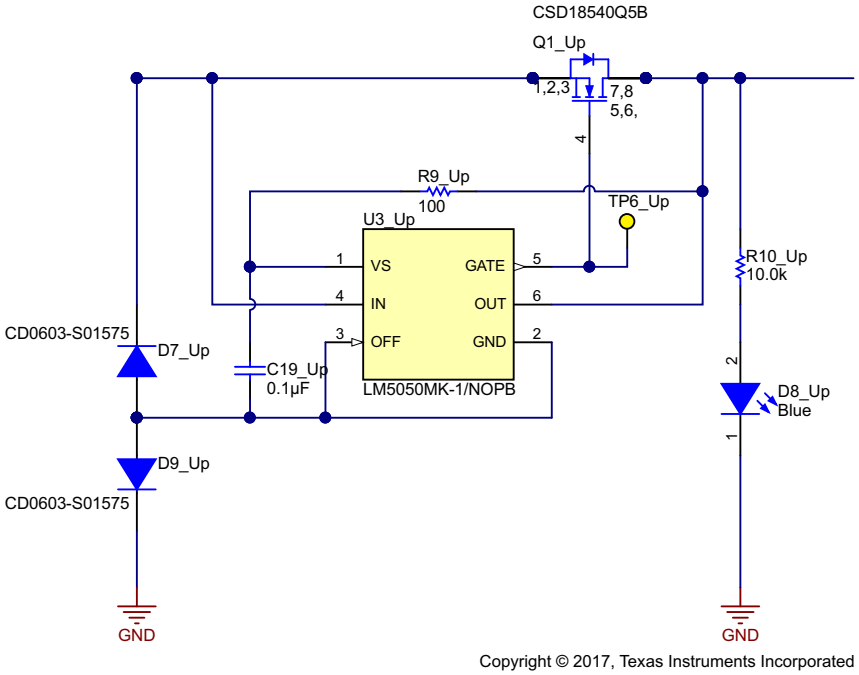


図 3. Schematic of Reverse Polarity Protection With LM5050-1

If the MOSFET current reverses, possibly due to failure of the input supply, such that the voltage across the LM5050-1 IN and OUT pins is more negative than –28 mV (typical), the LM5050-1 quickly discharges the gate of Q1 through a strong GATE to IN pin discharge transistor. If the input supply fails abruptly, as would occur if the supply was shorted directly to ground, a reverse current temporarily flows through the MOSFET until the gate can be fully discharged. This reverse current is sourced from the load capacitance and from the parallel connected supplies. The LM5050-1 responds to a voltage reversal condition typically within 25 ns. The actual time required to turn off the MOSFET depends on the charge held by the gate capacitance of the MOSFET being used. A fast turnoff time minimizes voltage disturbances at the output as well as the current transients from the redundant supplies.

2.3.2 Power Input Protection Circuit

The power input protection circuit is implemented using the LM5069 controller. This circuit includes UVLO, OVLO, current limit, power limit and in-rush current limit. 図 4 shows the relevant part of the schematic.

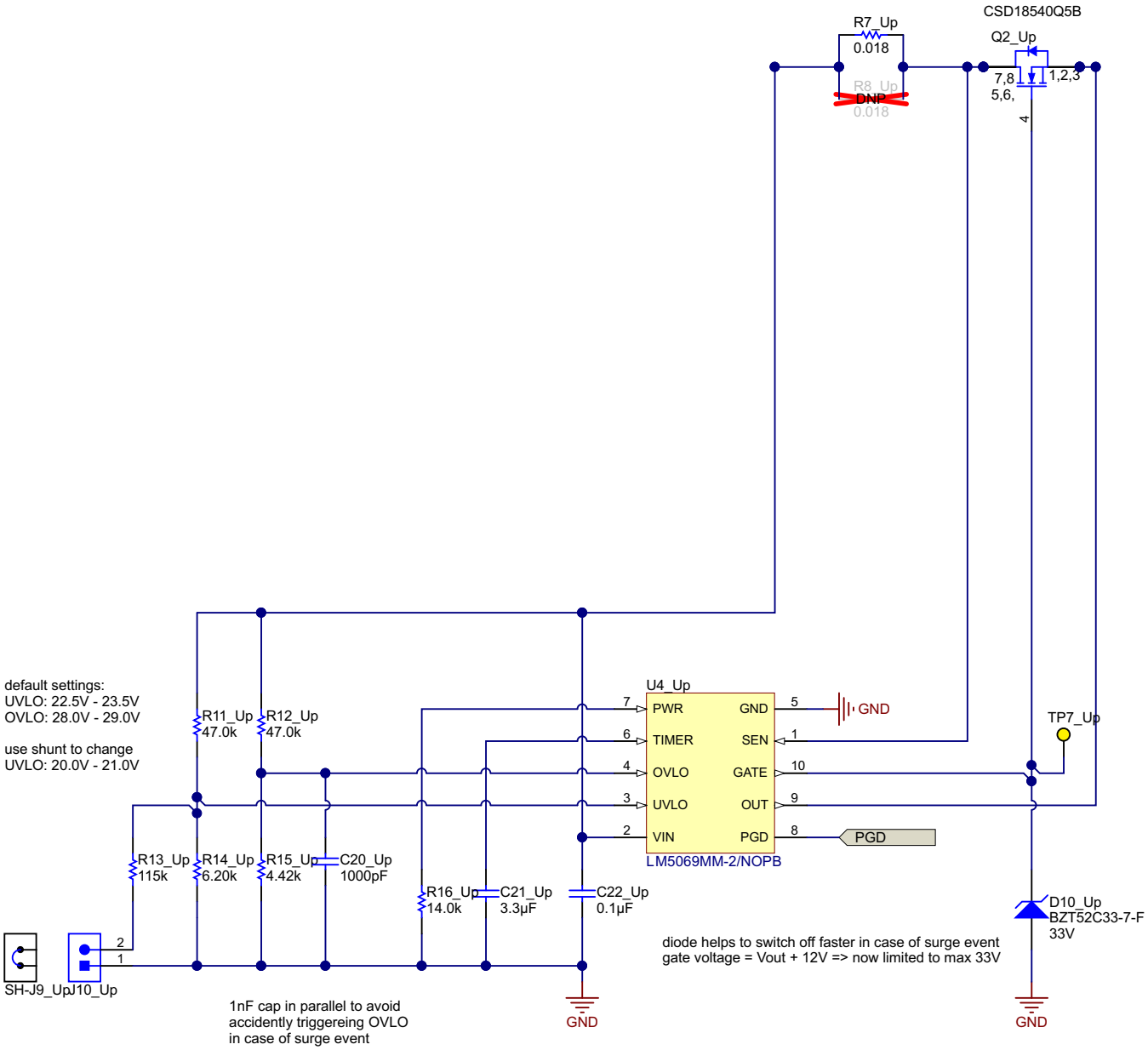


図 4. Schematic of UVLO, OVLO, Current Limit, Power Limit, and In-Rush Current Limit With LM5069

2.3.2.1 Undervoltage and Overvoltage Lockout

EtherCAT P devices need to operate between voltage levels of 24 V +20% –15%. MOSFET Q2 is enables when the input voltage is within the operating range defined by the programmable UVLO and OVLO levels. These levels can be defined using resistors R11 to R15. By default, jumper J10 is set. Following the EtherCAT P implementation guide, the UVLO is set to 23.0 V to 23.5 V, and the OVLO is set to 28.0 V to 28.8 V.

If wanted by the device manufacturer, the UVLO levels can be set lower. Lower voltage levels can for example occur in an EtherCAT P network, if a device is connected over a long cable. Today, EtherCAT P cables exist in 50-m lengths. If a device is now drawing 3A of current, this will results in a non negligible voltage drop across the 50-m cable. To address lower UVLO levels, jumper J10 can be removed so that the UVLO is changed to 20.4 V to 20.9 V. Moreover, this change gives additional flexibility to the user while testing the design.

For details on how to select the resistors for the UVLO and OVLO levels, refer to the UVLO and OVLO sections in *LM5069 Positive High-Voltage Hot Swap and In-Rush Current Controller With Power Limiting* .

2.3.2.2 Power-up Sequence of LM5069

The power-up of the LM5069 circuitry works as follows. As the voltage at V_{in} initially increases, MOSFET Q2 is held off by an internal 230-mA pulldown current at the GATE pin. The strong pulldown current at the GATE pin prevents an inadvertent turnon as the MOSFET's gate-to-drain (Miller) capacitance is charged. Additionally, the TIMER pin is initially held at ground.

When the V_{in} voltage reaches a threshold of 7.6 V, the insertion time begins. During the insertion time, the capacitor at the TIMER pin is charged by a 5.5-µA current source, and Q2 is held off by a 2-mA pulldown current at the GATE pin regardless of the V_{in} voltage. The insertion time delay allows ringing and transients at V_{in} to settle before Q2 can be enabled. The insertion time ends when the TIMER pin voltage reaches 4 V. Then the capacitor is quickly discharged by an internal 1.5-mA pulldown current.

After the insertion time, the LM5069 control circuitry is enabled when V_{in} reaches a threshold of 8.4 V. The GATE pin then switches on Q2 when the UVLO threshold is exceeded, the UVLO pin > 2.5 V. If V_{in} is above the UVLO threshold at the end of the insertion time, Q2 switches on. The GATE pin charge pump sources 16 µA to charge the gate capacitance of Q2. The maximum gate-to-source voltage of Q2 is limited by an internal 12-V Zener diode.

Taken from the LM5069 data sheet, 図 5 shows an example for the power-up sequence.

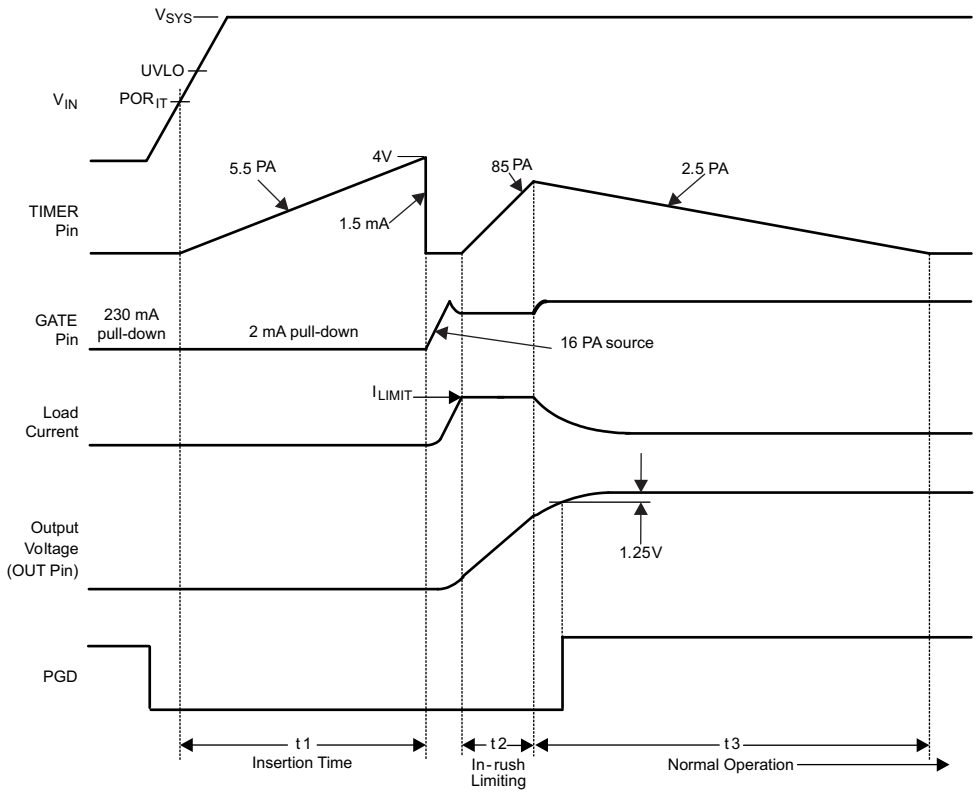


図 5. Power-up Sequence (Current Limit Only) of LM5069

2.3.2.3 Current Limit

The current limit threshold is reached when the voltage across the sense resistors R7 and R8 (VIN to SENSE) reaches 55 mV (typical). In the current limiting condition, the GATE voltage is controlled to limit the current in MOSFET Q2. While the current limit circuit is active, the LM5069 internal fault timer becomes active. The fault timer is running while the external capacitor at the TIMER pin is charged by a 85-µA source. If the fault condition subsides before the TIMER pin reaches 4 V, the LM5069 returns to normal operating mode and the capacitor at the TIMER pin is discharged by a 2.5-µA current sink.

For more information on the fault timer, see 2.3.2.6.

The continuous current must be limited to 3 A per supply. Using 式 1, the resistance of the parallel circuit of R7 and R8 is calculated to 18.3 mΩ.

$$R s e n s e = V s e n s e I l i m = 55 m V 3 A = 18 . 3 m \Omega \quad (1)$$

In the default assembly variant of the design, only R7 is used. Therefore, R7 is selected to 18 mΩ. The footprint of R8 can be used to adjust the parallel resistance.

2.3.2.4 Power Limit

In general, a lower power limit P_{lim} is preferred to reduce the stress on MOSFET Q2. However, when the LM5069 device is set to a very low power limit setting, it has to regulate the MOSFET current and hence the voltage across the sense resistor V_{sense} to a very low value. V_{sense} can be computed as shown in 式 2.

$$V s e n s e = P l i m \times R s e n s e V D S \quad (2)$$

To avoid significant degradation of the power limiting accuracy, a V_{sense} of less than 5 mV is not recommended. Based on this requirement the minimum allowed power limit $P_{lim,min}$ can be computed as in 式 3.

$$P_{lim,min} = V_{sense,min} \times V_{in,max} R_{sense} = 5\,mV \times 28.8\,V\,18\,m\Omega = 8\,W \quad (3)$$

Based on this requirement, the minimum allowed R_{power} to set the current limit can be computed with 式 4.

$$R_{power} = 1.3 \times 10^5 \times R_{sense} P_{lim} - 1.18\,mV \times V_{DS} R_{sense} \quad (4)$$

R_{power} is at a minimum when $V_{DS} = V_{in,max}$ = 28.8 V. R_{power} is then calculated to 14.3 kΩ and selected to 14 kΩ.

2.3.2.5 In-Rush Current Limit

In case of an in-rush current event, the voltage drop across R7 and R8 must not be higher than 105 mV. Otherwise, the gate of Q2 is pulled down with a 230-mA current sink. To make sure the current is never exceeding 7 A, the minimum resistance must be at least 15 mΩ (see 式 5). This resistance is given by the selected sense resistor of 18 mΩ.

$$R_{sense,min} = 105\,mV\,7\,A = 15\,m\Omega \quad (5)$$

2.3.2.6 Fault Timer

The LM5069 internal fault timer starts running when the LM5069 is in power limit or current limit, which can be the case during power-up. Thus the timer must be sized large enough to prevent a time-out during power-up. According to the EtherCAT P implementation guide, an EtherCAT P PSD must be able to load 2200 µF. Therefore, C_{out} is set to 2200 µF.

It is assumed that in case of a hot swap, the board starts in power limit and transitions into current limit. In that case, the estimated start time can be calculated with 式 6.

$$t_{start} = C_{out} \times 2 \times V_{in,max} \times \frac{2P_{lim} + P_{lim}}{I_{lim}} = 2200\,\mu F \times 2 \times 28.8\,V \times \frac{2 \times 8\,W + 8\,W}{3\,A} = 115\,ms \quad (6)$$

This start-time assumes a constant, typical current limit and power limit values. The actual startup time is slightly longer, as the power limit is a function of V_{DS} and decreases as the output voltage increases. To ensure that the timer never times out during power-up, TI recommends setting the minimum fault time t_{fault} to be greater than the start time t_{start} by adding an additional margin of 50% of the fault time. This margin accounts for the variation in power limit, timer current, and timer capacitance. As a result, capacitor C_{timer} is calculated to 3.7 µF and finally selected to 3.3 µF.

$$C_{timer} = t_{start} \times \frac{i_{timer,typ}}{V_{timer,typ}} \times 1.5 = 115\,ms \times \frac{85\,\mu A}{4\,V} \times 1.5 = 3.7\,\mu F \quad (7)$$

This results in a actual fault time t_{fault} of 155 ms, which is the typical time that the LM5069 shuts off MOSFET Q2.

$$t_{fault} = C_{timer} \times \frac{v_{timer,typ}}{i_{timer,typ}} = 3.3\,\mu F \times \frac{4\,V}{85\,\mu A} = 155\,ms \quad (8)$$

Now that the power limit and fault timer are chosen, check if the MOSFET stays within its SOA. During a hot-short, the circuit breaker trips and the LM5069 restarts into a power limit until this timer runs out. In the worst case, V_{DS} equals the maximum input voltage $V_{in,max}$ of 28.8 V. I_{DS} equals P_{lim} / $V_{in,max}$ = 280 mA, and the stress event lasts for t_{fault} = 155 ms. The SOA in CSD18540Q5B the data sheet states that the device can handle up to 2.5 A at V_{DS} = 30 V for 100 ms. Therefore, it is assumed that the MOSFET can also handle 230 mA for 155 ms and that it can be used for this reference design.

With C_{timer} = 3.3 µF, the insertion time of the power-up sequence of the design is expected to take 2.4 s (see 式 9 and 2.3.2.2).

$$3.3\,\mu F \times \frac{4\,V}{5.5\,\mu A} = 2.4\,s \quad (9)$$

2.3.3 Power Couple In-Couple Out Circuitry

To couple the 24 V in the data lines, one LC filter per 24-V rail is used. 図 6 shows the relevant part of the schematic. The upper LC filter couples in Up, and the lower LC filter couples in Us. Furthermore, the DC voltage blocking caps C3, C4, C6, and C7 of the data lines can be seen. These caps are necessary to protect the Ethernet transformer from the 24-V rails and prevent a short circuit across the windings of the Ethernet transformer.

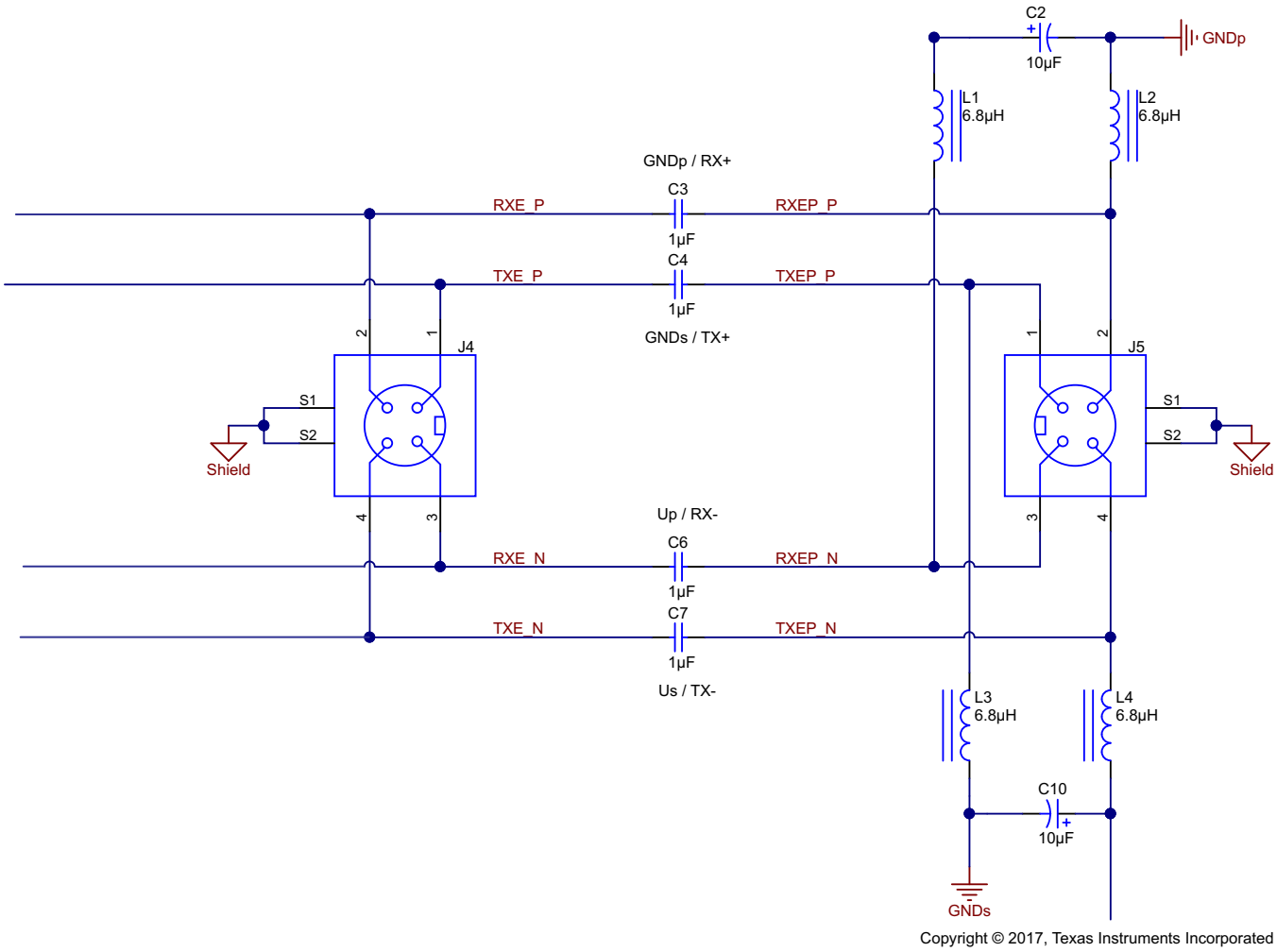


図 6. Schematic of Power Couple In-Couple Out Circuitry

The LC filter act as a second-order, low-pass filter for the communication lines. Following the EtherCAT P implementation guide, L is selected to 6.8 µH and C is selected to 10 µF. This results in a cutoff frequency of the LC filter of 19.3 kHz (see 式 10).

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{6.8\ uH \times 10\ uF}} = 19.3\ kHz \quad (10)$$

図 7 shows the bode plot of a second-order LC low-pass filter with L = 6.8 µH and C = 10 µF. 表 2 shows the attenuation at selected frequencies.

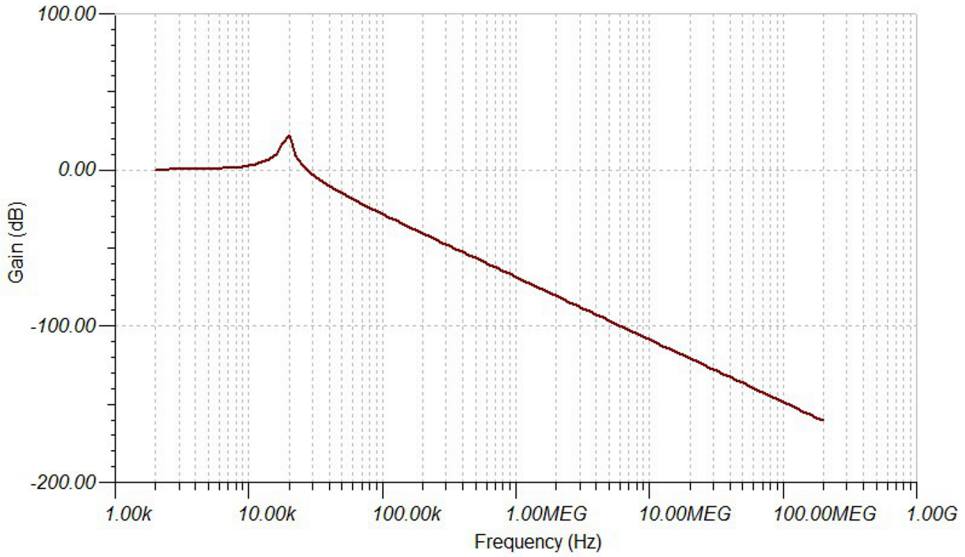


図 7. Bode Plot of Second-Order LC Low-Pass Filter (L = 6.8 µH and C = 10 µF)

表 2. Attenuation of LC Filter for Selected Frequencies

FREQUENCY	200 kHz	2 MHz	20 MHz	125 MHz
ATTENUATION	–40.54 dB	–80.62 dB	–120.62 dB	–152.45 dB

EtherCAT uses 100Base-TX to transfer data. 100Base-TX is operating at a frequency of 125 MHz. Therefore, the LC filter is attenuating the AC signals of the EtherCAT communication by about –152 dB. As a result, the EtherCAT communication signal is only decoupled a little from the data lines. However, the DC power signal can be coupled in to the data lines without big losses. However, it must be ensured that the selected inductor L can handle the maximum current of 3A continuously.

The same circuitry as shown in 図 6 is used to couple power out. Make sure that jumpers J2, J3 and J7, J8 on the board are set for power couple out. The power protection circuitry is then bypassed and the output voltage is available at connectors J1 and J7. The additional 5-V supply is available at connector J6.

2.3.4 Additional Protection on Power and Data Lines

For additional protection against ESD events on the data lines, ESD diodes are put in between the Ethernet connector and the EtherCAT P connector.

For additional protection on the power lines, a TVS diode rated for IEC 61000-4-2 (ESD minimum level 4), IEC 61000-4-4 (EFT), and IEC 61000-4-5 (surge) is placed after the power input connectors J1 and J7. Furthermore, a bidirectional TVS diode formed out of two TVS3300 devices is placed after the EtherCAT P connector to couple power out.

This additional protection is not hard requirement of the implementation guide. However, it is recommended to take precautions against any ESD, EFT, or surge events that might occur in the system.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

- Power supply: GW INSTEK GPS4303
- Scope: Tektronix MSO4034
- Multimeter: FLUKE 45
- Electronic load: PCE Power Control, Chroma 63102
- Laptop with TwinCAT® software
- Four TIDA-01461 reference designs
- Two AMIC110 ICE boards

3.2 Testing and Results

3.2.1 Test Setup

To characterize the design, two test setups are used: one to test the power functionality, and one to test the communication. The two setups are explained in the following two subsections.

3.2.1.1 Power Test Setup

To test the power transfer between two boards over an EtherCAT P cable:

1. Connect the power supply with two 24-V outputs to the first design board. Each output must be capable of providing a current of 3 A.
2. Use an EtherCAT P cable to connect the first design board to the second.
3. Connect the outputs of the second design board an electronic load that can draw up to 3 A per channel.
4. Use a scope to measure the overcurrent protection and to observe the start-up sequence.

図 8 shows a block diagram of the power test setup.

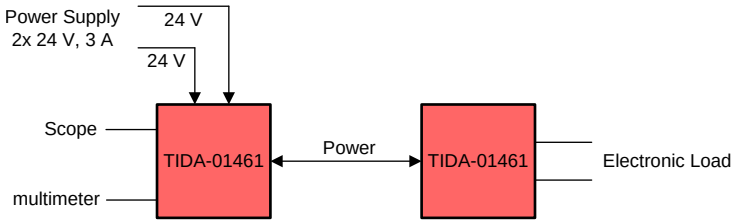


図 8. Power Test Setup

3.2.1.2 Communication Test Setup

To test the communication between an EtherCAT master and an EtherCAT slave in a daisy chain:

1. Connect the power supply to the first design board.
2. Use a battery-powered laptop that is running TwinCAT as an EtherCAT master.
3. Connect the laptop to the first design board using an Ethernet cable.
4. Connect the first design board to a second design board with an EtherCAT P cable.
5. Use the 5-V output of the second design board to power the first AMIC110 ICE board.
6. Connect this AMIC110 ICE board to the second and third design board with an Ethernet cable.
7. Connect the third and fourth design board with another EtherCAT P cable.
8. Connect the fourth design board to the second AMIC110 ICE board with an Ethernet cable.
9. Use the 5-V output of the fourth design board to power the second AMIC110 ICE board.

図 9 shows a block diagram of the communication test setup.

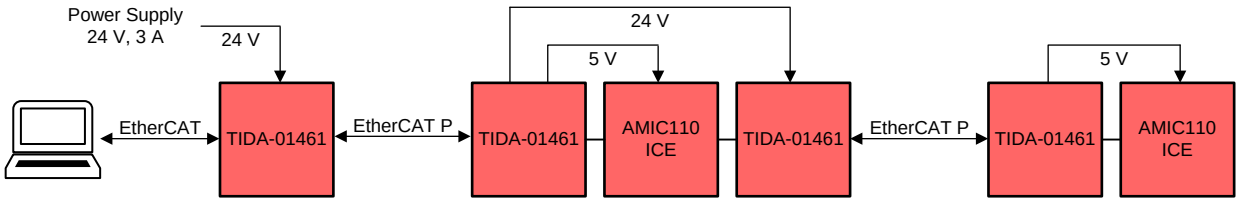


図 9. Communication Test Setup

3.2.2 Test Results

3.2.2.1 Reverse Polarity Protection

If any of the two 24-V rails is applied in a reverse way, Q1 does not switch on. This information is also indicated by a red LED at each input of the 24-V rails.

3.2.2.2 Power-up Sequence

The power test setup described in 3.2.1.1 is used to test this sequence.

図 10 shows a screen shot of the power-up sequence of one 24-V supply. As both 24-V supplies are built up in an identical way, this behavior is valid for both supplies.

Channel 1 is the voltage level of V_{in}. Channel 2 is the voltage level of GQ1, which is the signal at the gate of Q1. Channel 3 is the voltage level of GQ2, which is the signal at the gate of Q2. Channel 4 is the voltage level of V_{out}.

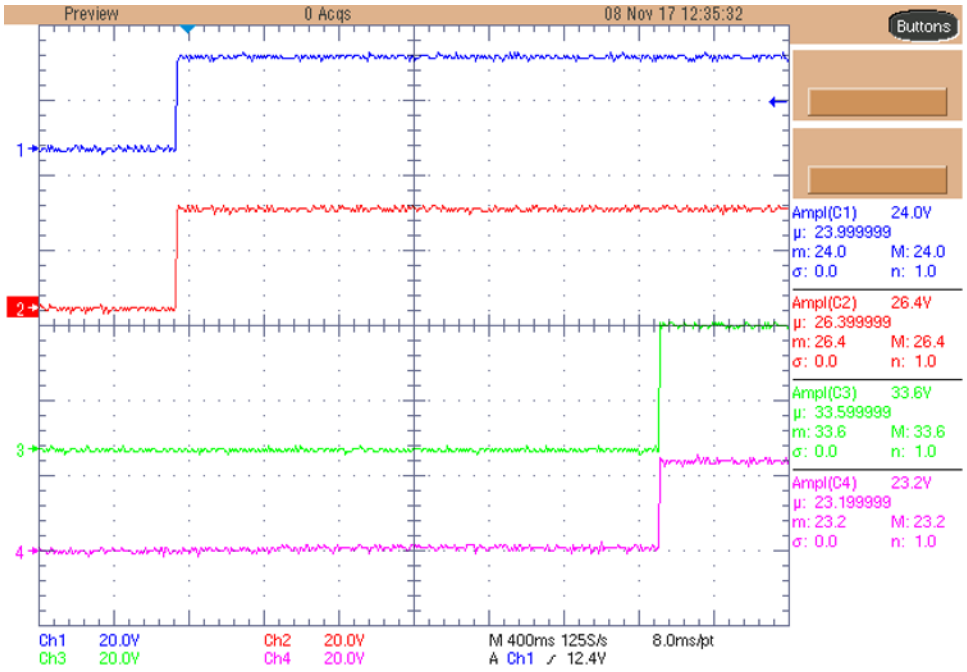


図 10. Power-up Sequence—V_{in} (1), GQ1 (2), GQ2 (3), V_{out} (4)

Q1 is enabled directly after the voltage is applied. Then the power-up sequence of the LM5069 device starts. As expected in 2.3.2.6, the power-up takes around 2.5 s. 図 11 shows the same power-up sequence, except that channel 3 is now showing the voltage level at C_{timer}.

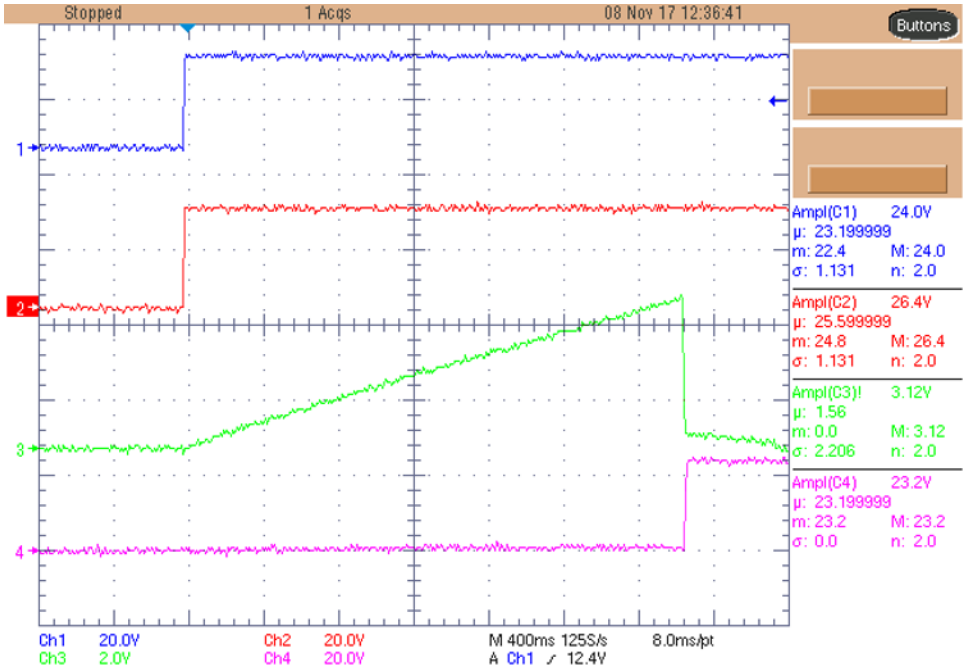


図 11. Power-up Sequence—V_{in} (1), GQ1 (2), C_{timer} (3), V_{out} (4)

3.2.2.3 Current Limit

The power test setup described in 3.2.1.1 is used to test the current limit.

The multimeter measures the voltage drop across the resistor R_{sense} while the electronic load is slowly increased. At a current of 2.86 A, the LM5069 turns off MOSFET Q2 and current is blocked. This results in a voltage drop of 2.86 A × 0.018 mΩ = 51.5 mV. This value complies with the voltage drop tolerances of 48.5 mV to 61.5 mV, as specified in the LM5069 data sheet.

3.2.2.4 Short-Circuit Behavior

The power test setup described in 3.2.1.1 is used to test the short-circuit behavior. However, this time the electronic load is disconnected and a short-circuit is done at the output of the second design board.

図 12 shows a screen shot of the short-circuit behavior of one 24-V supply. As both 24-V supplies are built up in an identical way, this behavior is valid for both supplies.

Channel 1 is the voltage level of V_{in}. Channel 2 is the voltage level of GQ1, which is the signal at the gate of Q1. Channel 3 is the voltage level of GQ2, which is the signal at the gate of Q2. Channel 4 is the voltage level of V_{out}.

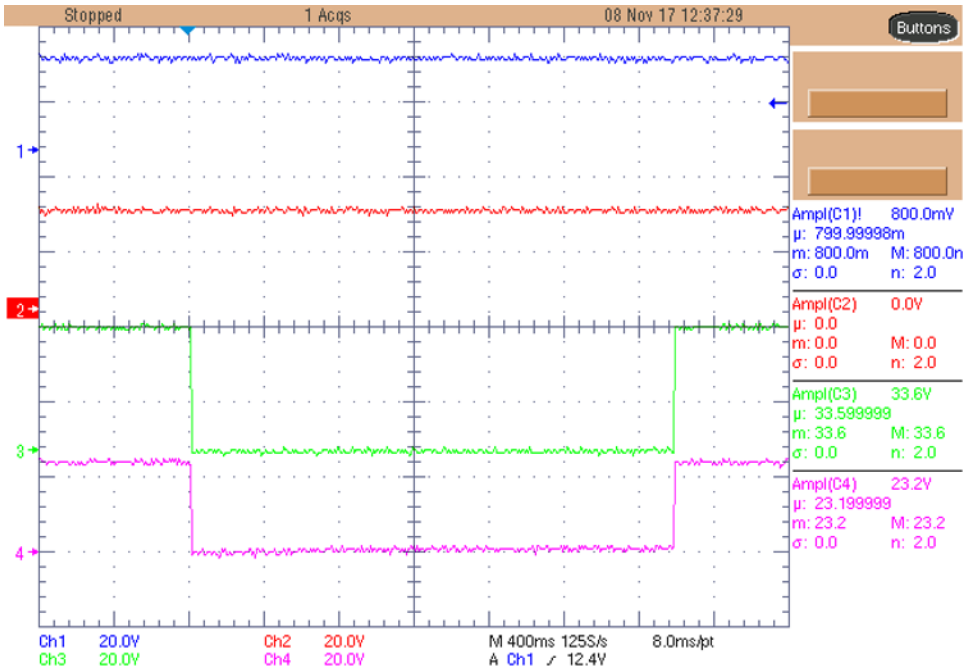


図 12. Short-Circuit Behavior—V_{in} (1), GQ1 (2), GQ2 (3), V_{out} (4)

Q2 is disabled directly when the short circuit is happening. Then the power-up sequence of the LM5069 device starts. Like in the normal power-up sequence, this takes again around 2.5 s.

図 13 shows the same power-up sequence, except that channel 3 is now showing the voltage level at C_{timer}.

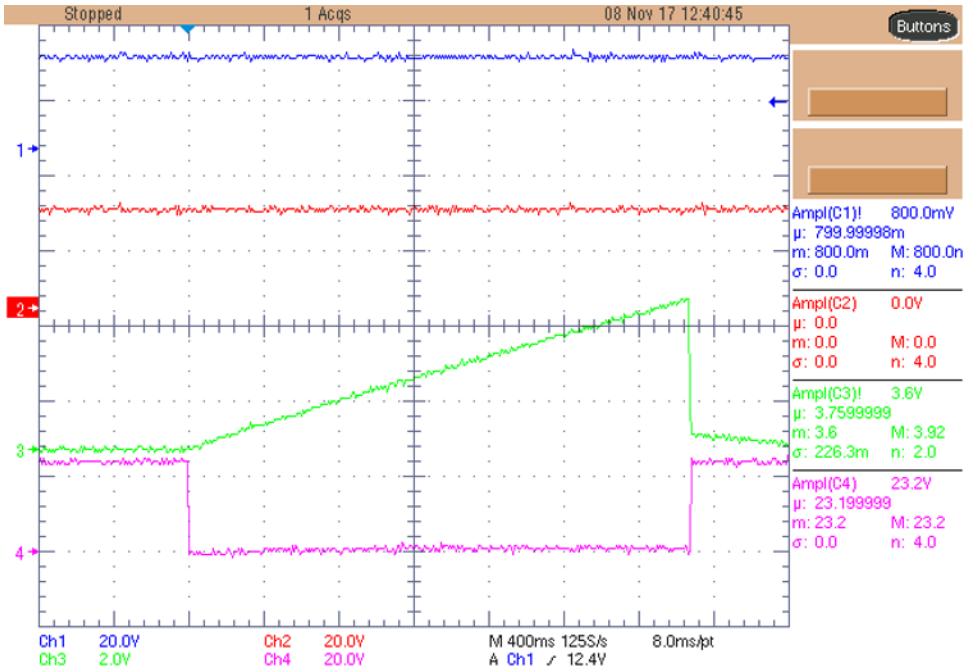


図 13. Short-Circuit Behavior—V_{in} (1), GQ1 (2), C_{timer} (3), V_{out} (4)

3.2.2.5 *Undervoltage and Overvoltage Lockout*

The power test setup described in 3.2.1.1 is used to test the UVLO and OVLO. The multimeter measures the voltage after Q1.

First, the input voltage is set to 24 V and then decreased slowly. At an input voltage of 22.5 V, the LM5069 turns off MOSFET Q2 and blocks the current from flowing. The input voltage must be increased to 23.5 V before MOSFET Q2 is turned on again.

Now, the input voltage is set to 24 V again and increased slowly. At an input voltage of 28.8 V, the LM5069 turns off MOSFET Q2 and blocks the current. The input voltage must be decreased to 28.0 V before MOSFET Q2 is turned on again.

3.2.2.6 Communication

The communication test setup described in 3.2.1.2 is used to test the communication. The laptop acts as an EtherCAT master and is running TwinCAT. In TwinCAT, the two connected AMIC110 ICE boards are detected. Then, the setup runs for several minutes and the number of transmit and receive errors are counted. 図 14 shows a screen shot of the TwinCAT software after the setup runs for several minutes. Zero frames were lost and zero Tx/Rx errors occurred.

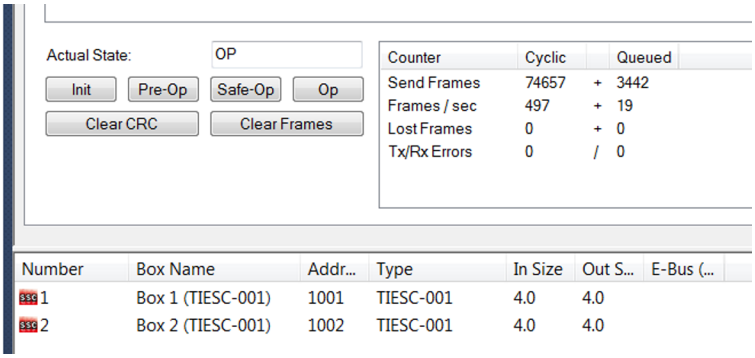


図 14. TwinCAT—Lost Frames and Tx/Rx Errors After Several Minutes Operation

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01461.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01461 .

4.3 PCB Layout Recommendations

This reference design is not layout optimized because in a final EtherCAT PSD, all communication and power circuitry are implemented on one board. However, this reference design only implements the power couple in-couple out circuitry. Therefore, for PCB layout recommendations, refer to the official *EtherCAT and EtherCAT P Slave Implementation Guide* .

Nevertheless, special care has been taken so that the line impedances and lengths of the EtherCAT lines from connector J4 to connector J5 match.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01461.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01461.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01461.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01461.

5 Software Files

To download the software files, see the design files at TIDA-01461.

6 Related Documentation

1. EtherCAT Technology Group, *EtherCAT and EtherCAT P Slave Implementation Guide*

6.1 商標

7 About the Author

TOBIAS PUETZ is a systems engineer in the Texas Instruments Factory Automation and Control team, where he is focusing on PLC and robotics. Tobias brings to this role his expertise in various sensing technologies as well as power design. Tobias earned his master's degree in electrical engineering and information technology at the Karlsruhe Institute of Technology (KIT), Germany in 2014.

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