BURR - BROWN®
APPLICATION BULLETIN
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USING DSP101 WITH MULTIPLEXED ANALOG INPUTS

The DSP101 and DSP102 sampling analog-to-digital converters have all the interface logic to connect directly to popular digital signal processor ICs from ADI, AT&T, Motorola, and Texas Instruments. A unique "tag" input allows additional serial data to be appended to the serial data stream that is sent to the DSP processor. When the DSP101[(1)] is coupled with an analog multiplexer, this tag feature can be used to construct a low cost multiple input A/D that will send a channel identification number along with that channel's conversion results. The channel ID can then be used by the DSP processor to separate the different inputs.

The DSP101 uses an internal data pipeline architecture to synchronize the data from the Successive Approximation Register (SAR) analog-to-digital converter to the data clock of the DSP processor IC. The block diagram of the DSP101 (Figure 1) shows how data moves through the part and how the tag bits are appended. The serial data from the SAR is clocked into a shift register and held by a latch. On the next convert command, the data is then loaded into an output shift register and clocked out to the DSP processor IC, synchronous to the bit transfer clock. As the serial data is clocked out to the DSP processor IC, serial data inputted to TAG is clocked into the output shift register. Figure 2 shows how the serial tag information is appended after the 18th bit of data.

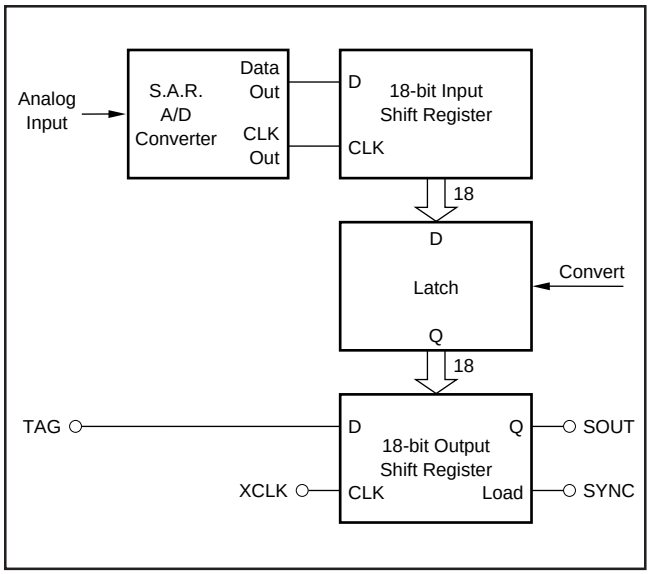

FIGURE 1. DSP101 Internal Block Diagram.

The schematic of Figure 3 shows a complete eight-channel analog input system. A 74HC163 counter is used to provide the scan sequence to a Burr-Brown HI-508A analog multiplexer. In order to allow the HI-508A enough time to switch to the next channel and settle before the DSP101 begins its conversion, a 74HC221 one shot is used to produce a 3ms delay for the DSP101 convert command input.

To avoid introducing distortion to the signal, the input to the DSP101 must be driven by a low impedance source. Due to the high output impedance of the HI-508A, an OPA627 in a unity gain configuration is used as a buffer for the DSP101 input.

Since the DSP101 has an internal data pipeline delay of one sample, a 74HC574 D-type latch is used to delay the tag bits by one sample also. This delay causes the channel identification tag to be appended directly to that channel's conversion results. Since the channel scanning shown in the schematic is sequential, this delay latch could be left out and the DSP processor software modified to recognize an N-1 channel ID. However, for systems using non-sequential scan lists, this delay latch would be essential to maintain the data and channel ID integrity.

The 74HC166 synchronous loading shift register is used so that the rising edge of the bit clock, in conjunction with the SYNC output of the DSP101, loads the tag data into the shift register in a predictable manner. The tag data is then clocked into the DSP101 by the bit clock, while conversion data is clocked out the other end of the shift register.

This circuit is constructed on Burr-Brown's DEM-DSP102/202 demonstration fixture. Software for recognizing channel tags and sorting the data was written for Burr-Brown's ZPB34 DSP board for the IBM PC/AT. This board is based on the AT&T WE® DSP32C and the software for this circuit is available from the ????.

Since the SYNC output of the DSP101 that is used to load the latches in this circuit is active low for AT&T DSP processors, the circuit must be modified for use with DSP processors from Texas Instruments, Motorola, and ADI. For these processors, tie the SSF pin of the DSP101 high, and use a 74HC04 hex inverter to invert the SYNC line input to the 74HC574 and 74HC166.

NOTE: (1) This discussion applies to both the DSP101 and the dual DSP102, but for simplicity we will talk only about the DSP101.

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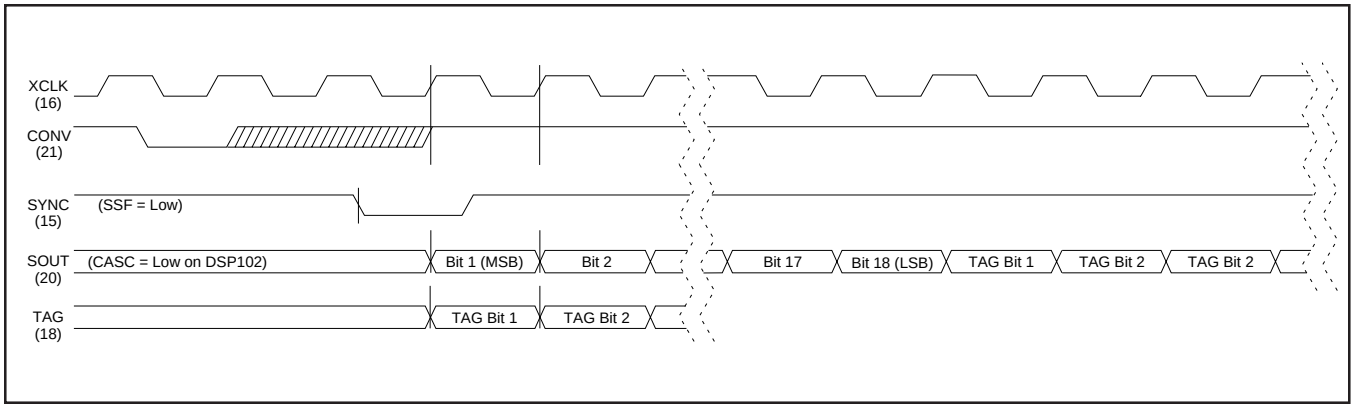

FIGURE 2. DSP101/102 SOUT Data Format with TAG Information. (See DSP101 data sheet for full timing information.)

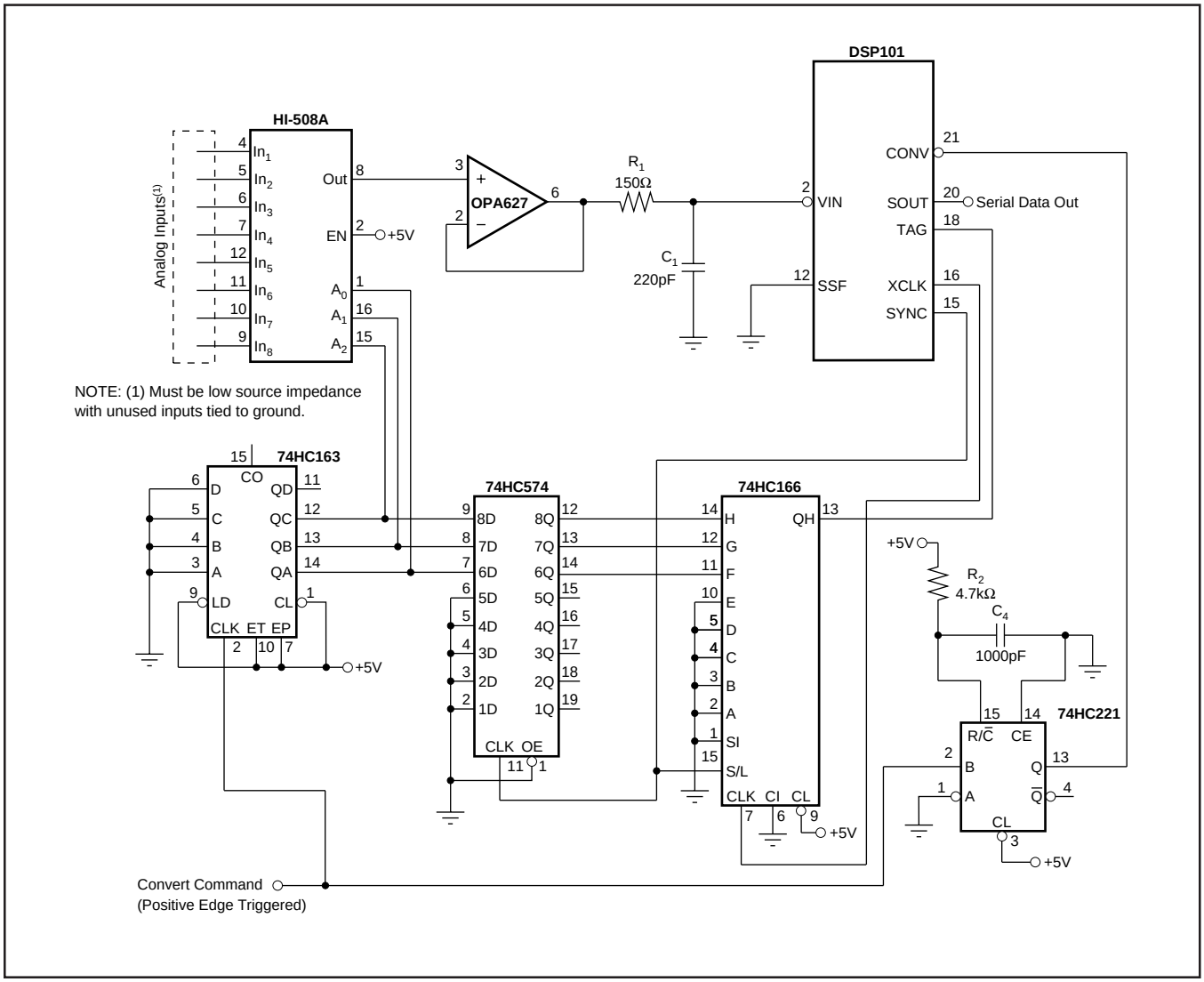

FIGURE 3. A Complete Eight-Channel Analog Input System Using the DSP101 and the HI-508A.

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