

Synchronizing the ADS1271

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ABSTRACT

The ADS1271 is a delta-sigma converter, and these types of converters are reputedly difficult to synchronize to external events. The ADS1271 has a synchronization input, however, which indicates that not only is synchronization possible, but useful.

Synchronization on the ADS1271 serves two purposes. Most often, it is used to enable simultaneous sampling by multiple ADS1271s, typically through a daisy-chain configuration. Synchronization can also be used to match the conversion cycle of the ADS1271 to external events. In the first section of this application note, we show how to synchronize multiple ADS1271s to each other. In the second section, we show how to make an ADS1271 perform conversions in response to an external event.

Contents

1	Synchronizing Multiple ADS1271 Devices	1
2	Synchronizing an ADS1271 to External Events	5

List of Figures

1	Simultaneous Sampling in SPI Mode	2
2	Simultaneous Sampling in FSYNC Mode	3
3	Synchronization Timing	4
4	Synchronizing the ADS1271 to a Pulse	5
5	PLL-Based Clocking.....	6
6	Resynchronization Timing	7

1 Synchronizing Multiple ADS1271 Devices

When multiple ADS1271s are synchronized, they sample simultaneously. Simultaneous sampling is often needed in multi-channel systems, and the ADS1271 was specifically designed to make this configuration as easy as possible. In fact, if you want to daisy-chain multiple ADS1271s, you have to synchronize them; successful daisy-chaining depends on it.

In order to synchronize multiple ADS1271s, do the following:

- Connect the CLK and SYNC pins together. If you are using FSYNC mode, also connect the DRDY/FSYNC pins together.
- After system power-up, wait long enough for the clock oscillator to start, and then apply a pulse to the SYNC pin.

[Figure 1](#) shows an example of this configuration for SPI™ format; [Figure 2](#) shows this configuration for FSYNC format.

Synchronizing Multiple ADS1271 Devices

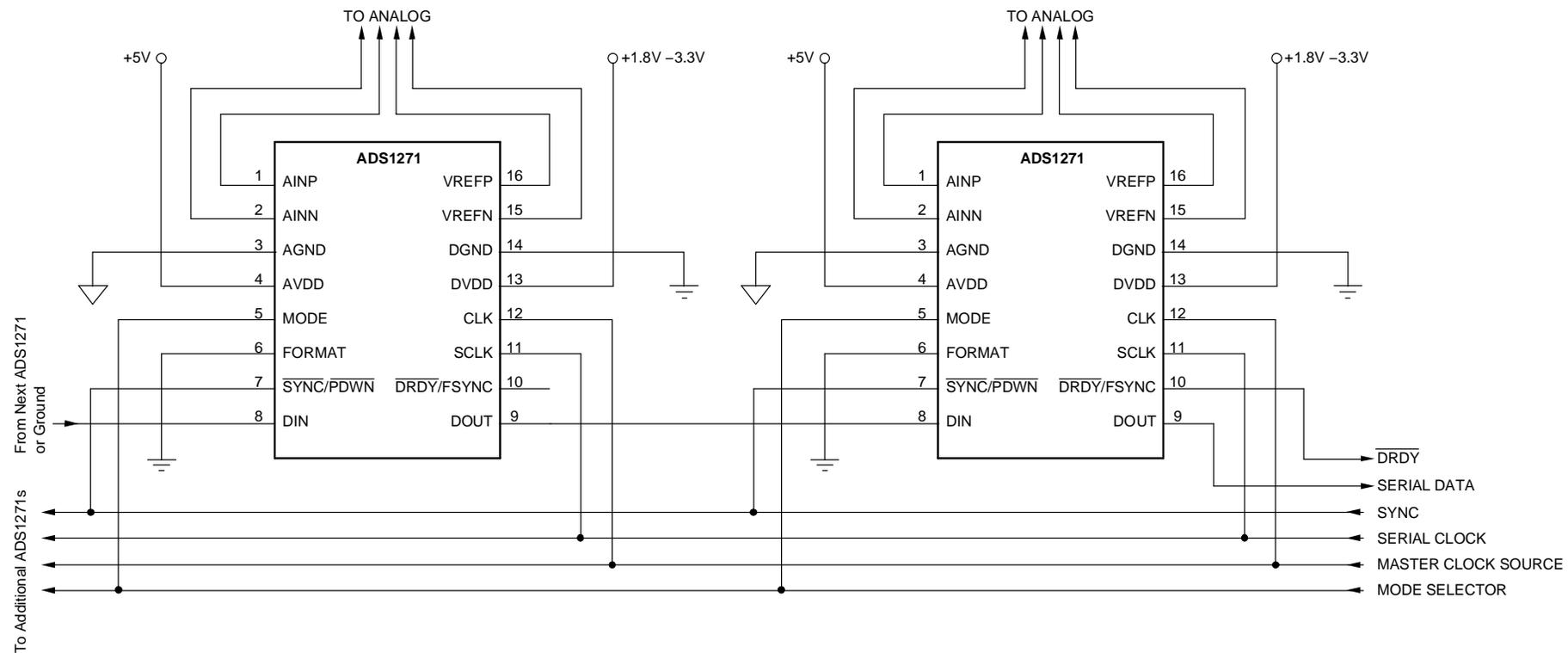


Figure 1. Simultaneous Sampling in SPI Mode

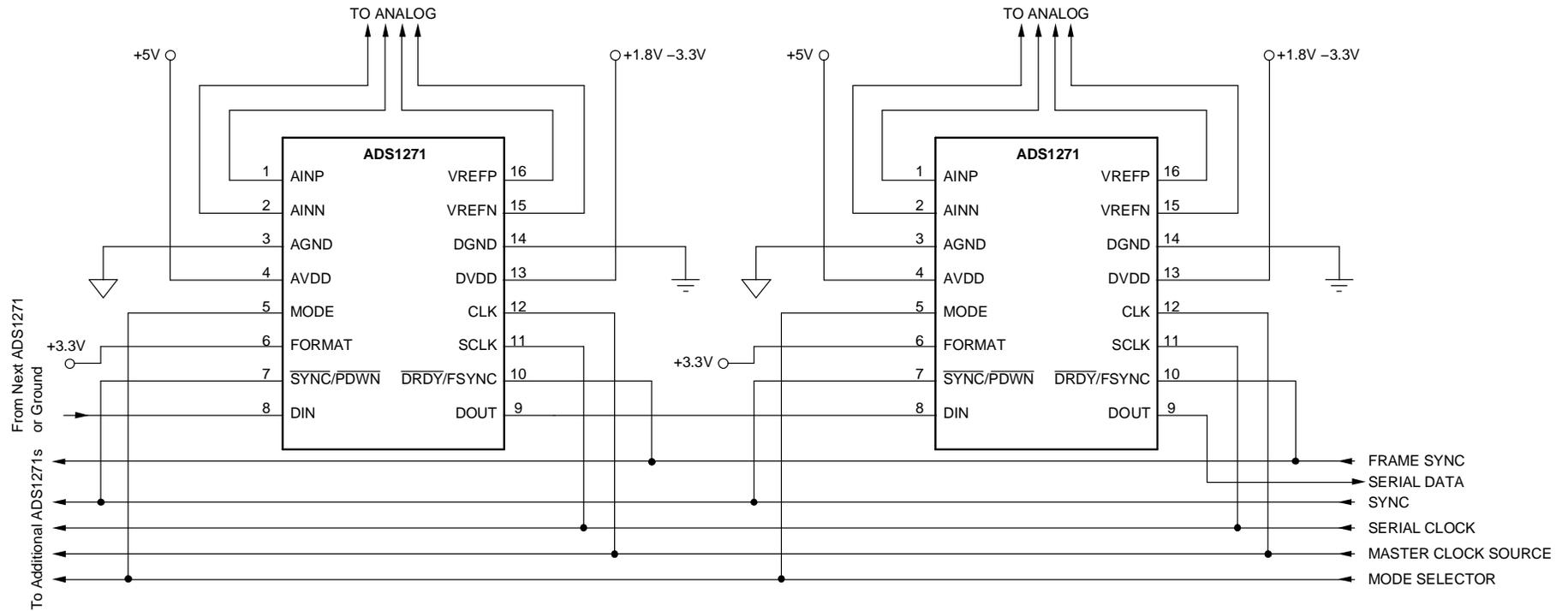


Figure 2. Simultaneous Sampling in FSYNC Mode

The CLK pins must be connected together so that the ADS1271s are operating from the same time reference. This condition is vital for synchronization. A delta-sigma converter is an inherently synchronous device: that is, it operates according to a clock, advancing to the next step of its operation only when a clock edge occurs. If multiple ADS1271s are operating on different clocks, they will sample at different rates; but if they are operating from the same clock, they will sample at exactly the same rate.

The other essential connection is the $\overline{\text{SYNC/PDWN}}$ pin. When the ADS1271 detects a pulse on this pin, it immediately starts a new conversion cycle (as well as a settling cycle, as explained in Section 2), thus resetting the conversion phase, as shown in Figure 3.

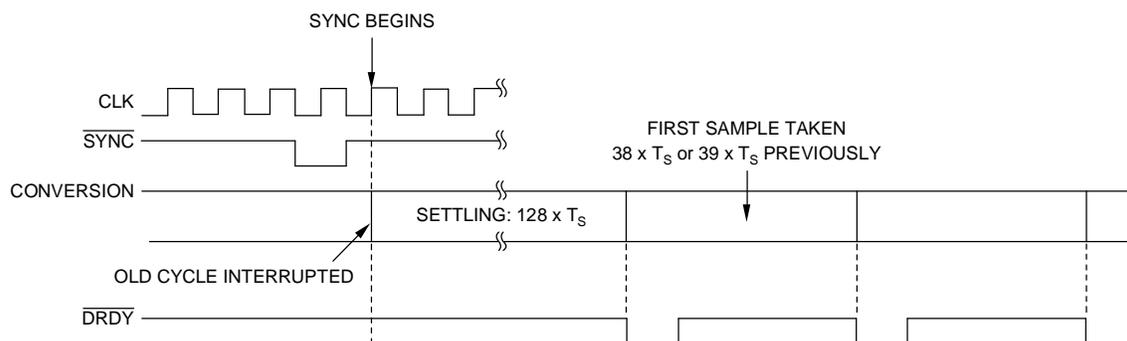


Figure 3. Synchronization Timing

The $\overline{\text{SYNC/PDWN}}$ pulse is detected synchronously with respect to the master clock. The ADS1271 samples the $\overline{\text{SYNC/PDWN}}$ line on falling edges of the master clock. It operates normally when the $\overline{\text{SYNC/PDWN}}$ line is high. When the $\overline{\text{SYNC/PDWN}}$ line is sampled low, the ADS1271 halts the conversion process and resets the digital filter. It then waits for the $\overline{\text{SYNC/PDWN}}$ line to return high. When the line is sampled high, the converter restarts and a settling cycle is initiated. Because sampling occurs on the falling edge of the master clock, it is recommended to transition $\overline{\text{SYNC/PDWN}}$ at rising edges of the master clock, but this is not absolutely critical.

The SYNC pulse is needed because the CLK pin gives the ADS1271 a time-base, but no frame of reference with regard to conversion. After power-up, until a SYNC pulse occurs, it is impossible to predict at which master clock cycle the conversions will begin, since the ADS1271 has an internal power-on reset circuit that triggers at an uncertain level. Two ADS1271s connected to the same CLK line will almost certainly start converting at slightly different times after power-up; however, if they receive the same SYNC pulse at the same time later on, they will all restart at the same time, and remain synchronized thereafter, as long as they continue to receive the same clock signal.

Note that the CLK line is typically a mid- to high-frequency signal. If the printed circuit board (PCB) layout is poor, the clock signal may be ringing or distorted by the time it arrives at the ADS1271. If the signal corruption is severe enough, the ADS1271 may miss clock edges, or interpret the ringing as extra edges. Different ADS1271s may do this at different times, and can lose synchronization with each other, despite being physically connected to the same clock line.

To prevent this problem, consider employing high-speed layout techniques, especially if the CLK line is very long or connected to many devices. If you have more than eight ADS1271s to synchronize, consider using buffers or clock distribution chips to distribute the clock signal.

In SPI mode, once the ADS1271s are synchronized to each other, all of the $\overline{\text{DRDY}}$ lines will deliver falling edges at the same time. This means that the user only needs to monitor one $\overline{\text{DRDY}}$ line in order to determine when to start the shift.

2 Synchronizing an ADS1271 to External Events

The $\overline{\text{SYNC/PDWN}}$ pin is also useful for synchronizing the ADS1271 to external events, with certain limitations.

The limitations are a result of the filter settling time. When a SYNC pulse occurs, the ADS1271 filter must be reset, and then must settle. Two things are at work here. First, it takes time for the ADS1271 filter to fill with incoming data; the filter must process 38 or 39 samples before it can generate a result. Therefore, there is a delay through the filter of 38 or 39 samples, depending on the conversion mode (38 samples in high-speed and low-power modes, 39 samples in high-resolution mode).

The ADS1271 filter delay is called *group delay* in the specification table in the [product datasheet](#), and is measured in units of samples. Group delay is often given for filters that delay frequencies by different amounts, but the ADS1271 finite impulse response (FIR) filter has a linear phase response, and has constant group delay. The ADS1271 time delay is not frequency-dependent.

The filter also has a settling time that is a result of the filter transfer function. The ADS1271 filter has a long step response: that is, when a step function is applied to the input, the filter takes a certain amount of time to settle to the final step value. Resetting the filter is equivalent to applying a step input, which may be full-scale.

To accommodate the filter delay and settling time, the ADS1271 suppresses output data for 128 conversion periods following synchronization. This period is more than enough time for the filter to settle and to fill with data. Unfortunately, this delay means that the ADS1271 cannot sample immediately in response to an external event, unlike a successive-approximation (SAR) converter.

Nevertheless, there are certain types of external events to which the ADS1271 can be synchronized. A good example is the rotation of a shaft through a position. Suppose the shaft has an encoder mechanism that generates a square wave with a frequency that is proportional to the rotation rate of the shaft; then, suppose that you want the ADS1271 to take a sample every time the shaft rotates through a certain position. The ADS1271 can be synchronized to this external event by deriving the master clock from the shaft rotation pulse using a phase-locked loop (PLL), and by delivering the synchronization pulse at the right time in relation to the shaft rotation position. The ADS1271 will then sample in time with the shaft rotation. The connection shown in [Figure 5](#) can be used for this type of synchronization.

Another kind of event to which the ADS1271 potentially can be synchronized is the beginning of a pulse, for pulse height measurement. If the pulse lasts a few milliseconds, and the ADS1271 is converting fast enough so that its synchronization delay is shorter than the pulse length, the ADS1271 can sample the latter part of the pulse, as illustrated in [Figure 4](#).

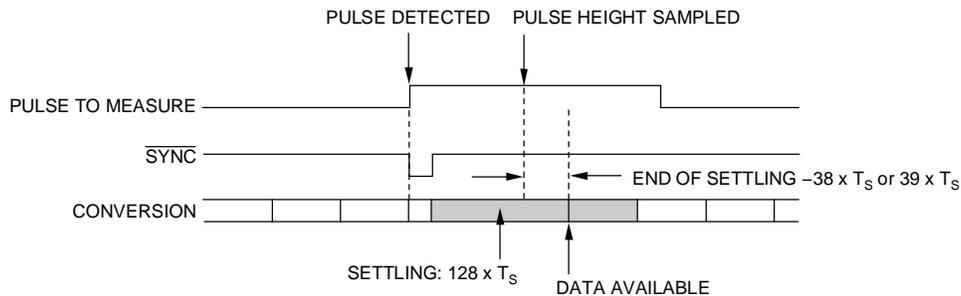


Figure 4. Synchronizing the ADS1271 to a Pulse

2.1 Synchronizing the ADS1271 to a Regularly Occurring Event

Figure 5 shows a possible connection for synchronizing to a regularly occurring event. Here, we want the ADS1271 to sample according to a sampling clock; whenever a rising edge appears on the clock, we want the ADS1271 to begin a new sampling period.

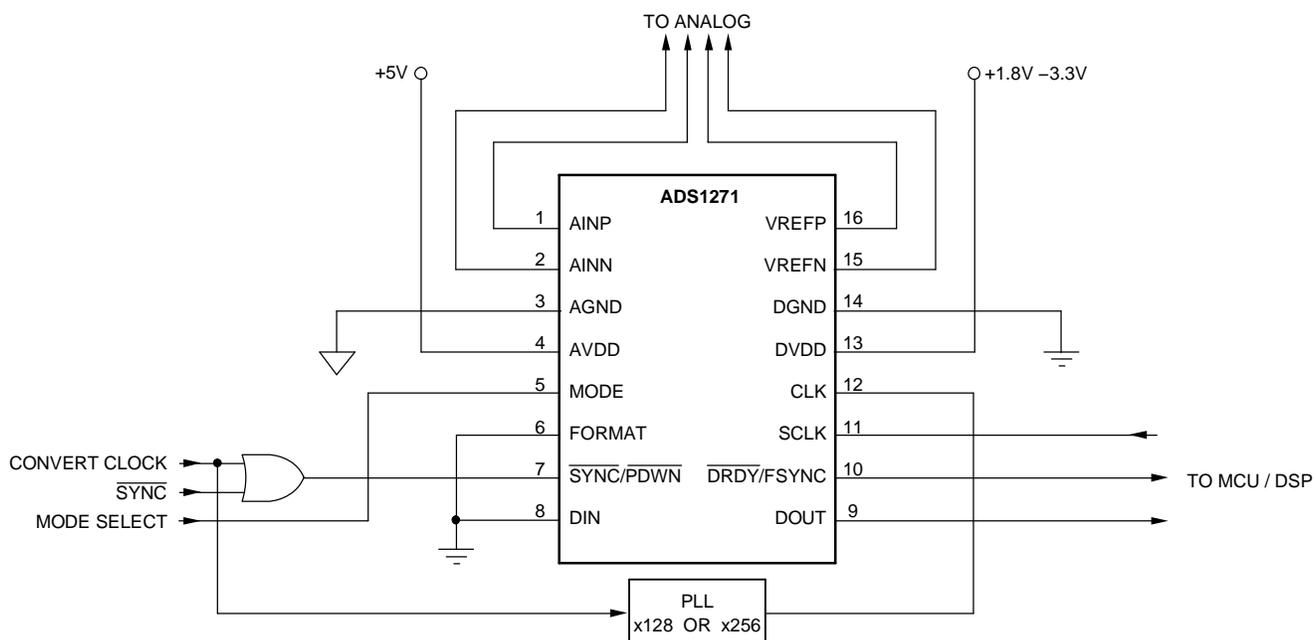


Figure 5. PLL-Based Clocking

To accomplish this synchronization, the ADS1271 is clocked by a PLL, which in turn is clocked from the conversion pulse. The PLL generates the right master clock frequency by multiplying the conversion pulse frequency. The frequency multiplier to use depends on the conversion mode: in high-speed and low-power modes, the multiplier should be 128, and in high-resolution mode, the multiplier should be 256.

PLLs can generate a great deal of jitter. Fortunately, delta-sigma converters tend to filter out much of the jitter that a PLL generates, especially cycle-to-cycle jitter. If the cycle-to-cycle jitter is uncorrelated, it will appear as noise in the modulator that will be reduced by or rejected at the ADS1271 filter. The ADS1271 is not generally as sensitive to jitter as a SAR-type converter, which converts entirely at the mercy of its sampling clock.

Note, however, that if the PLL is generating jitter at some regular frequency that appears in the sampling band, the jitter may cause unwanted tones in the output data. In this case, the PLL should be adjusted, or a different PLL should be used.

The PLL causes the ADS1271 to convert at the same rate as the conversion pulse; at startup, though, the ADS1271 conversion phase is uncertain, and must be synchronized to the conversion pulse. There are a few ways to synchronize the conversion phase. In this design, we use the microprocessor to gate the conversion clock into the SYNC pin through an OR gate. After system startup, the microprocessor briefly allows the conversion clock to drive the SYNC pin, so that the SYNC sees one falling and one rising edge from the conversion clock. At the rising edge, the ADS1271 begins converting in phase with the conversion clock. Figure 6 illustrates this approach.

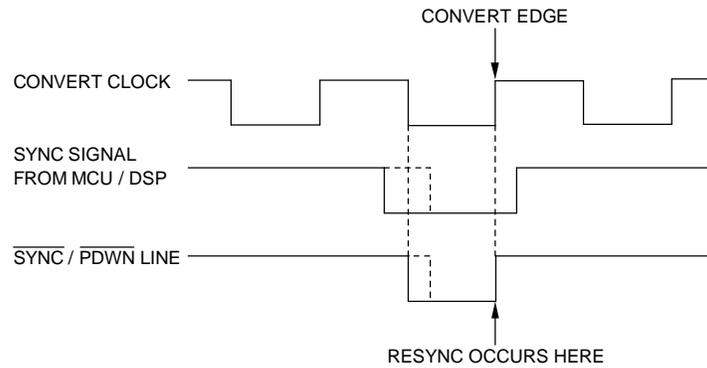


Figure 6. Resynchronization Timing

This connection can be expanded with multiple daisy-chained ADS1271s by connecting the respective SYNC and CLK lines together. In SPI mode, as noted earlier, only one $\overline{\text{DRDY}}$ line needs to be examined.

2.2 Synchronizing the ADS1271 to an Irregularly Occurring Event

Using the SYNC input, the ADS1271 can convert in *one-shot* fashion in response to an external event. It is important to understand how the filter affects this process. Because of the filter delay, the first sample retrieved from an ADS1271 after a SYNC pulse has been delivered corresponds to the filtered level of the input signal from 38 or 39 sample periods before the $\overline{\text{DRDY}}$ pulse occurred, as shown in Figure 3 and Figure 4. As described earlier, the precise delay depends on the conversion mode.

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