Pb-Free

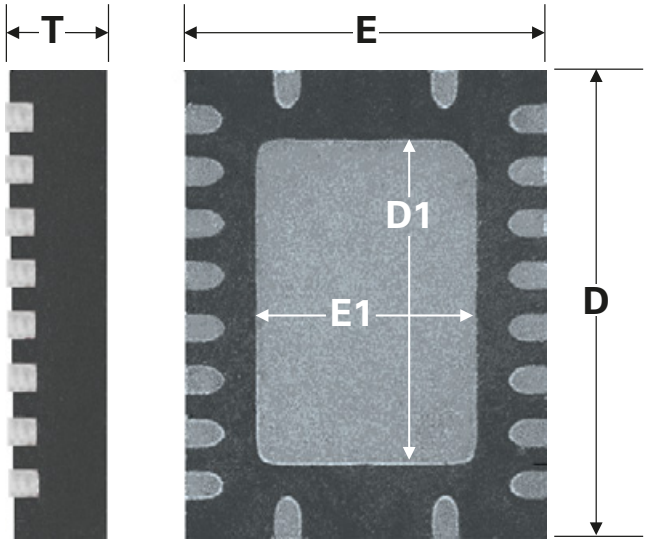
Design Summary for Quad Flat No-Lead Logic

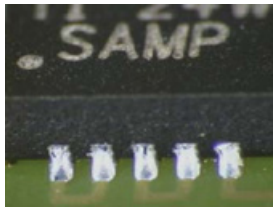
Introduction to QFN Logic

Advancing the logic industry trend toward smaller packaging technologies, Texas Instruments (TI) introduced 14-/16-/20-/24-pin Quad Flat No-Lead (QFN) packaging for gate and octal bit width logic devices. The QFN 14-/16-/20-pin RGY* packages and 24-pin RHL package have the same pinout as the thin scale small outline packages (TSSOP); however, it is up to 62% smaller than the TSSOP. According to QFN modeling data, thermal performance is improved from 60–70% and inductance improved up to 60% over the TSSOP. Designers can take advantage of reduced form factors in personal digital assistants, cell phones, and other portable consumer electronics by using this package.

TI is committed to the logic market with the introduction of QFN, the next standard in logic packaging, for both mature and advanced logic technologies. For more logic information, including application reports, samples and datasheets, visit: **logic.ti.com**

*RGY and RHL are the package designators found at the end of the orderable part number.





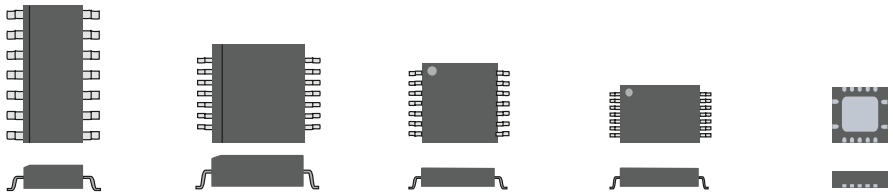
QFN Package Physical Characteristics

Characteristics	14-Pin QFN	16-Pin QFN	20-Pin QFN	24-Pin QFN
Pin Count (Per D Side/Per E Side)	5/2	6/2	8/2	10/2
D: Package Length (mm) nom.	3.5	4.0	4.5	5.5
E: Package Width (mm) nom.	3.5	3.5	3.5	3.5
T: Package Height (mm) nom.	0.9	0.9	0.9	0.9
D1: Max. Exposed Pad Length (mm)	2.15	2.65	3.15	3.15
E1: Max. Exposed Pad Width (mm)	2.15	2.15	2.15	2.15
Pitch (mm)	0.5	0.5	0.5	0.5
Lead Finger Width (mm) nom.	0.23	0.23	0.23	0.23
Lead Finger Length (mm) nom.	0.4	0.4	0.4	0.4
Package Weight (g)	0.032	0.036	0.043	0.053
Lead Finish	Matte Tin*	Matte Tin*	Matte Tin*	NiPdAu

*In transition to NiPdAu.

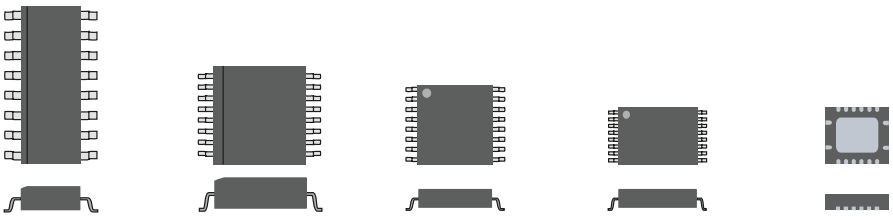
Package Comparisons

14-Pin Package



Characteristics	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Length (mm)	8.65 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	3.50 ±0.15
Width (mm)	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Max. Height (mm)	1.75	2.00	1.20	1.20	1.00
Pitch (mm)	0.50	0.50	0.50	0.40	0.50
Footprint Area (mm^2)	51.90	48.36	32.00	23.04	12.25
QFN Area Savings (%)	76.40	74.67	61.72	46.83	—
Weight (g)	0.127	0.122	0.055	0.040	0.032
$R_{\theta JA}$ (°C/W)	86.20	95.80	112.60	127.10	31.6
Avg. Resistance (Ω)	0.031	0.044	0.032	0.035	0.029
Avg. Inductance (nH)	3.109	3.551	2.378	2.499	0.791
Avg. Capacitance (pF)	0.473	0.402	0.314	0.361	0.226

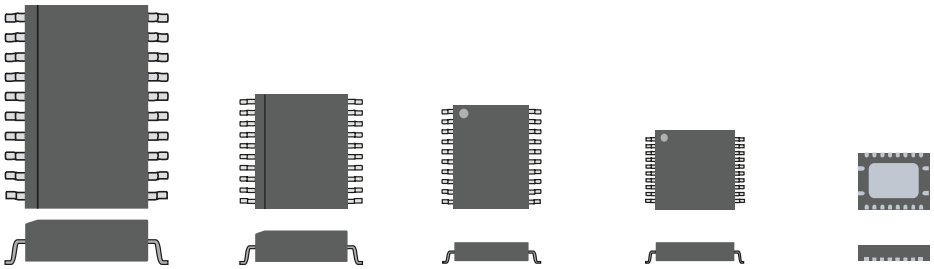
16-Pin Package



Characteristics	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Length (mm)	9.90 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	4.00 ±0.15
Width (mm)	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Max. Height (mm)	1.75	2.00	1.20	1.20	1.00
Pitch (mm)	0.50	0.50	0.50	0.40	0.50
Footprint Area (mm^2)	59.40	48.36	32.00	23.04	14.00
QFN Area Savings (%)	76.43	71.05	56.25	39.24	—
Weight (g)	0.150	0.140	0.062	0.040	0.036
$R_{\theta JA}$ (°C/W)	73.10	82.00	108.40	119.80	31.2
Avg. Resistance (Ω)	0.039	0.048	0.045	0.039	0.030
Avg. Inductance (nH)	3.453	3.536	2.593	2.543	0.818
Avg. Capacitance (pF)	0.521	0.376	0.281	0.386	0.236

Package Comparisons (Continued)

20-Pin Package



Characteristics	SOIC-20 (DW)	SSOP-20 (DB)	TSSOP-20 (PW)	TVSOP-20 (DGV)	QFN-20 (RGY)
Length (mm)	12.82 ±0.13	7.20 ±0.30	6.50 ±0.10	5.00 ±0.10	4.50 ±0.15
Width (mm)	10.40 ±0.25	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Max. Height (mm)	2.65	2.00	1.20	1.20	1.00
Pitch (mm)	0.50	0.50	0.50	0.40	0.50
Footprint Area (mm^2)	133.33	56.16	41.60	32.00	15.75
QFN Area Savings (%)	88.19	71.96	62.14	50.78	—
Weight (g)	0.495	0.151	0.075	0.055	0.043
$R_{\theta JA}$ (°C/W)	57.7	69.50	83.00	91.90	29.9
Avg. Resistance (Ω)	0.038	0.040	0.050	0.044	0.05
Avg. Inductance (nH)	5.012	3.495	2.808	2.561	1.119
Avg. Capacitance (pF)	0.717	0.420	0.317	0.342	0.352

24-Pin Package

Characteristics	SOIC-24 (DW)	SSOP-24 (DB)	TSSOP-24 (PW)	TVSOP-24 (DGV)	QFN-24 (RHL)
Length (mm)	15.4 ±0.20	8.20 ±0.30	7.80 ±0.10	5.00 ±0.10	5.50 ±0.15
Width (mm)	10.30 ±0.33	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Max. Height (mm)	2.65	2.00	1.20	1.20	1.00
Pitch (mm)	1.27	0.65	0.65	0.40	0.50
Footprint Area (mm^2)	158.62	63.96	49.92	32.00	19.25
QFN Area Savings (%)	87.8	69.9	61.4	39.8	—
Weight (g)	0.58	0.172	0.075	0.0587	0.053
$R_{\theta JA}$ (°C/W)	45.5	63.3	87.9	86.4	30.3
Avg. Resistance (Ω)	0.037	0.045	0.039	0.043	0.037
Avg. Inductance (nH)	5.146	3.668	2.685	2.601	0.806
Avg. Capacitance (pF)	0.758	0.416	0.320	0.358	0.188

IR Reflow Profile

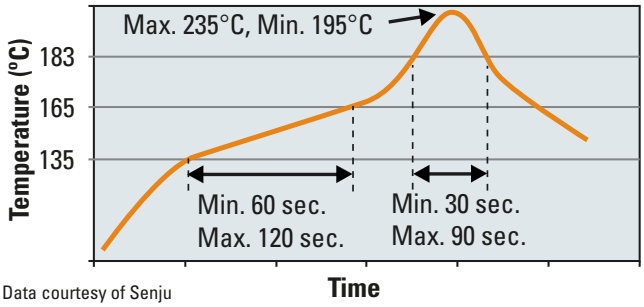
The RGY's matte Sn lead finish* and 24 RHL NiPdAu are compatible with lead and lead-free pastes. The recommended reflow profiles are provided for SnPb and Pb-Free.

*RGY in transition to NiPdAu.

Reflow Parameters

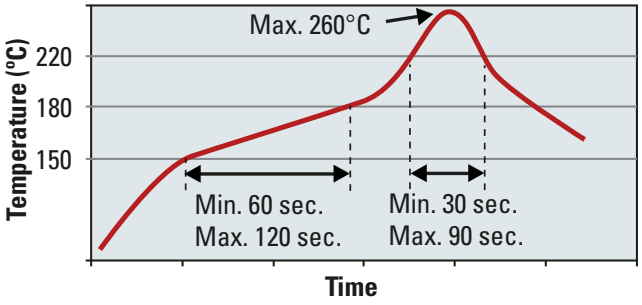
	SnPb	Pb Free
Ramp Rate	3°C/sec. Max.	3°C/sec. Max.
Preheat	135 to 165°C	150 to 180°C
	60 to 120 sec.	60 to 120 sec.
Time Above Liquidus	183°C	220°C
	30 to 90 sec.	30 to 90 sec.
Peak Temp.	235°C	255°C ±5°C
Time Within 5°C Peak Temp.	20 to 40 sec.	20 to 40 sec.
Ramp Down Rate	6°C/sec. Max.	6°C/sec. Max.

Recommended Temperature Profile for SnPb Eutectic (AT-Alloy and S2062)



Data courtesy of Senju

Pb-Free Recommended Temperature Profile for SnAgCu (#7100, M705, M31) Senju Pb-Free Paste

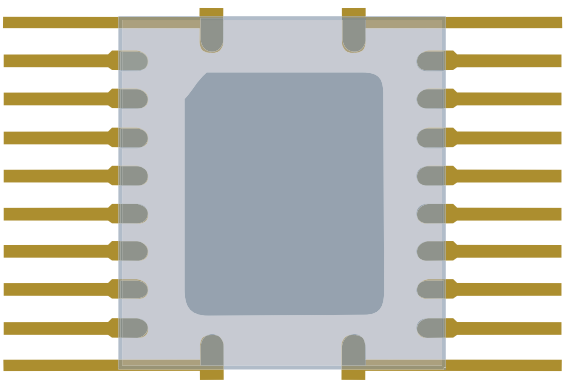


PCB Design Guidelines

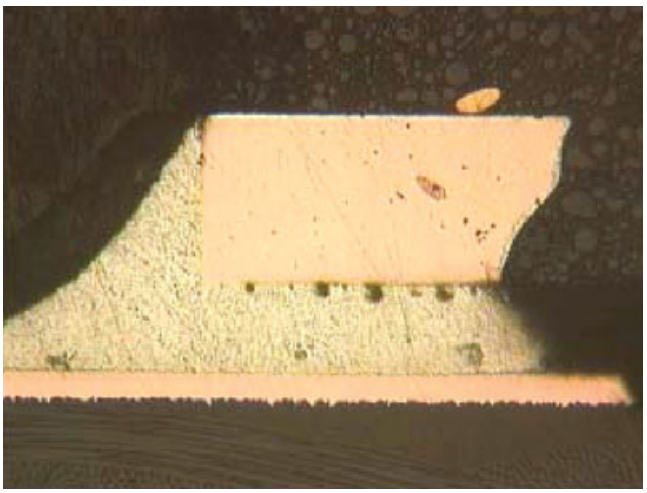
IPC-SM-782 is used as the standard for the PCB land-pad designs. Non-solder-mask-defined (NSMD) pads are recommended over solder-mask-defined pads because of the tighter tolerance on copper etching than solder masking. However, SMD pads are acceptable if mask registration is well controlled.

As a general rule, the PWB terminal pads should be designed 0.2 mm longer (away from package center) than the package terminal length for good solder filleting, and also should be extended 0.05 mm toward the centerline of the package. The pad width should be the maximum width of the component terminal for lead pitches below 0.65 mm to minimize solder bridging. Single-layer routing or standard via outside the package outline also is feasible because of flow-through design.

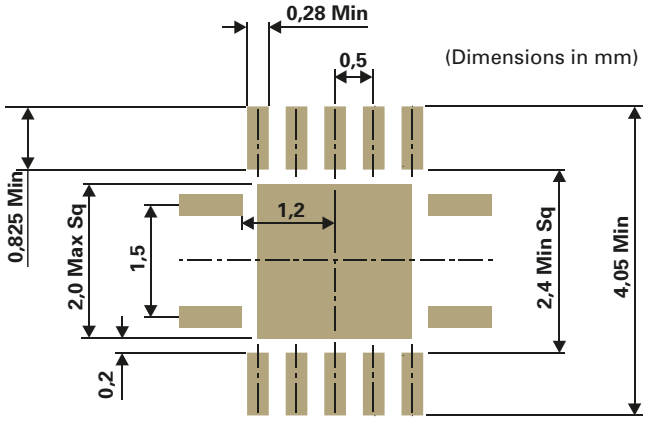
Sample Board Layout for Single-Layer Routing (Top View)



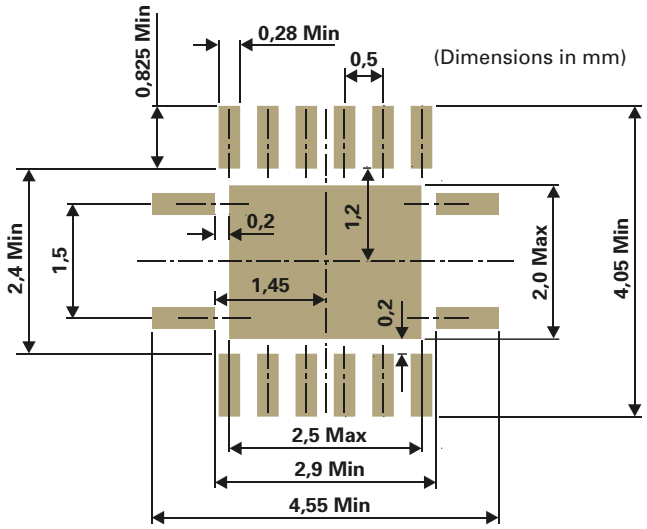
Cross-Section of Soldered QFN Terminal-Land-Pad Geometry



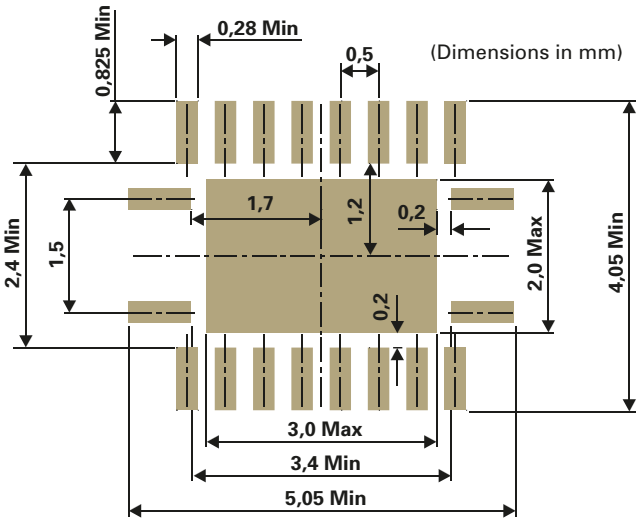
14-Pin QFN Recommended PCB Land-Pad Design



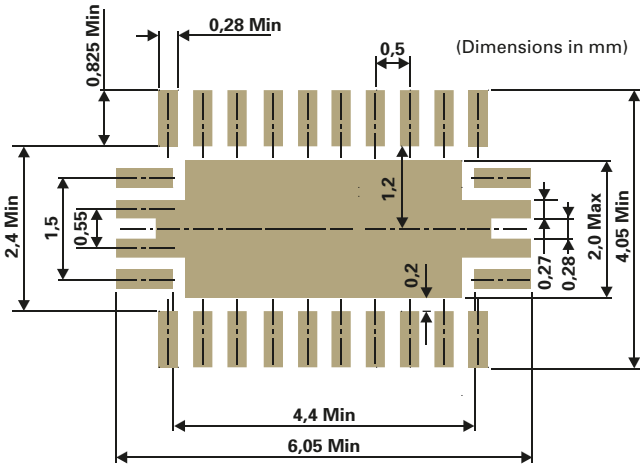
16-Pin QFN Recommended PCB Land-Pad Design



20-Pin QFN Recommended PCB Land-Pad Design



24-Pin QFN Recommended PCB Land-Pad Design



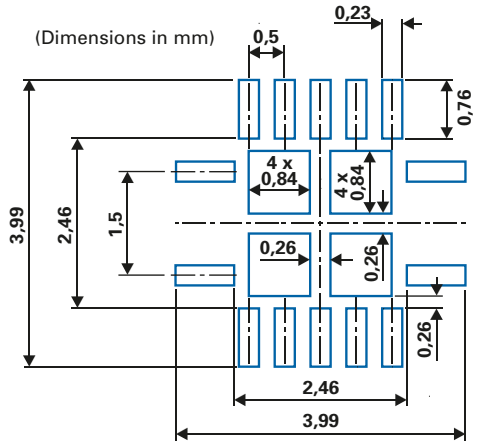
Solder Paste

TI recommends the use of type 3 or finer solder paste when mounting the QFN package. Successful solderability tests have been completed with SnPb and SnAgCu pastes. The use of these pastes offers the following advantages:

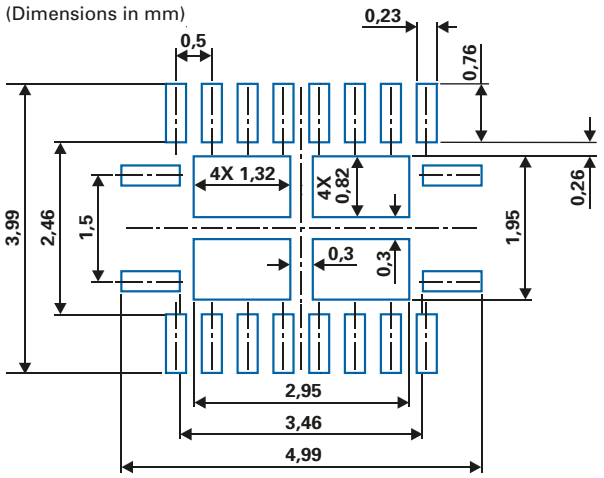
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, which allows the volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

As a guide, a stencil thickness of 0.1016 mm to 0.125 mm (4 mils to 5 mils) for these specific QFN packages is recommended. Stencil thickness greater than 0.125 mm requires larger openings for terminal pads and smaller openings for center pads. Area ratio constraints defined in IPC-7525 must be satisfied. The drawings to the right detail the stencil recommendations for the 14-, 16- and 20-QFN packages. All designs have area ratios >0.66 and paste-transfer efficiencies are 73% for terminal pads and 100% for thermal pads at a stencil thickness of 0.125 mm (5 mils). At a stencil thickness of 0.1016 mm (4 mils), the area ratio is 0.86, terminal-pad paste-transfer efficiency is 89% and 100% for the thermal pad. The slotted-thermal-pad stencil design is required so the QFN will not float during reflow and cause opens between the terminal leads and pads. This feature also allows adequate room for outgassing paste during the reflow operation, thus minimizing voids.

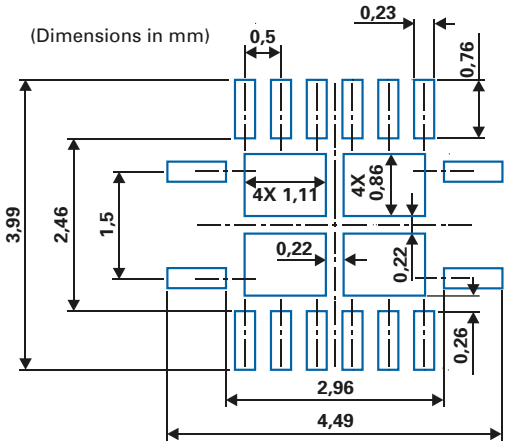
14-Pin QFN Stencil Design Recommendation



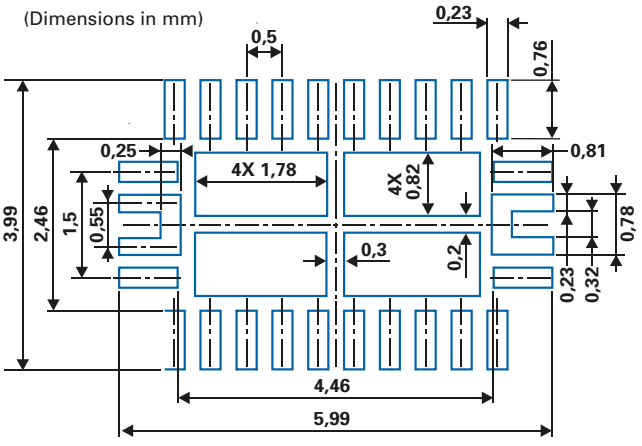
20-Pin QFN Stencil Design Recommendation



16-Pin QFN Stencil Design Recommendation



24-Pin QFN Stencil Design Recommendation

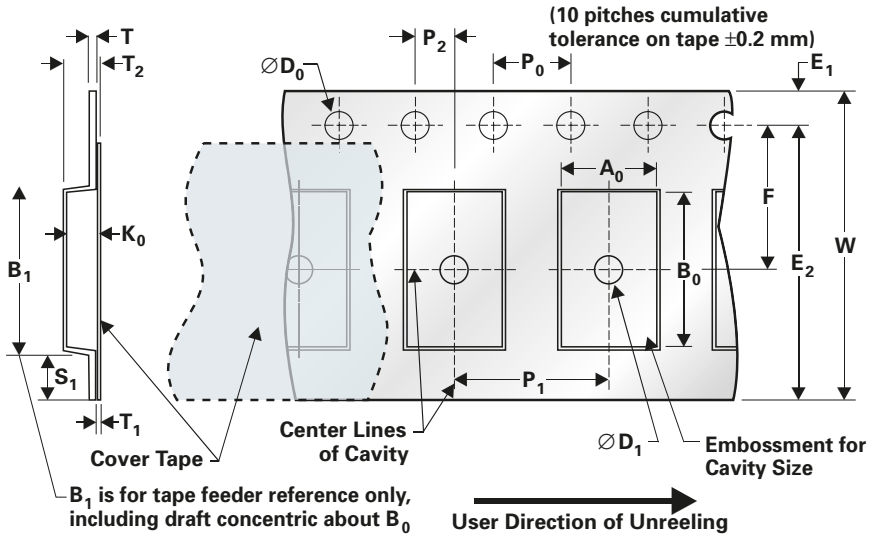


Packaging Tape and Reel

Carrier Tape Dimensions (Millimeters)

Package	Carrier-Tape Width (W)	Pocket Pitch (P)	Pocket Width (A_0)	Pocket Length (B_0)	Pocket Depth (K_0)	Device Qty. Per Reel (SPQ)
14-Pin QFN	12.0 ±0.30	8.0 ±0.10	3.80 ±0.10	3.80 ±0.10	1.20 ±0.10	1000
16-Pin QFN	12.0 ±0.30	8.0 ±0.10	3.80 ±0.10	4.30 ±0.10	1.20 ±0.10	1000
20-Pin QFN	12.0 ±0.30	8.0 ±0.10	3.80 ±0.10	4.80 ±0.10	1.20 ±0.10	1000
24-Pin QFN	12.0 ±0.03	8.0 ±0.10	3.80 ±0.10	5.80 ±0.10	1.20 ±0.10	1000

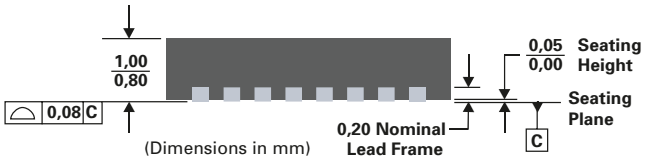
D_0	D_1 Min	E_1	P_0	P_2	S_1 Min.	T Max.	T_1 Max.
1.5 +0.1 –0.0	1.5	1.75 ±0.1	4.0 ±0	2.0 ±0.05	0.6	0.6	0.1



Geometric Dimensional Tolerances

Coplanarity

This geometric dimensioning and tolerancing (GD & T) term means this package meets a coplanarity of 0.08 mm as known. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane (Reference ASME Y14.5M - 1994).

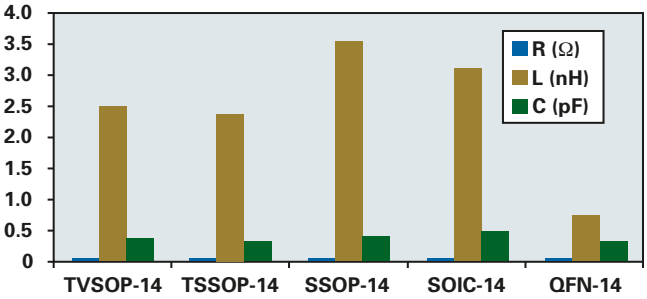


Electrical Characteristics

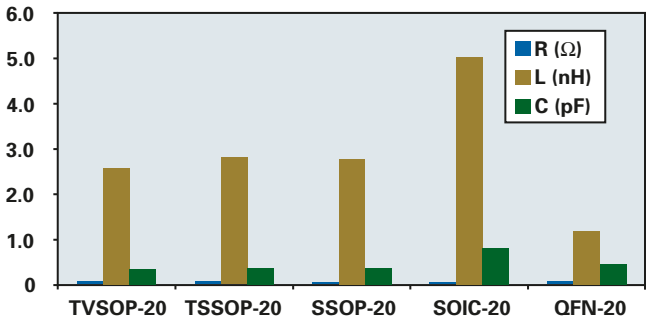
The unique construction of QFN packages reduces inductance. The exposed die pad of the QFN package is at board level following assembly, which minimizes inductance.

Electrical data shown is an approximation based on modeling.

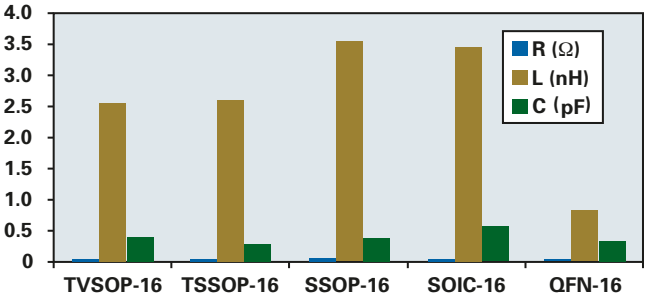
14-RGY Electrical Comparison



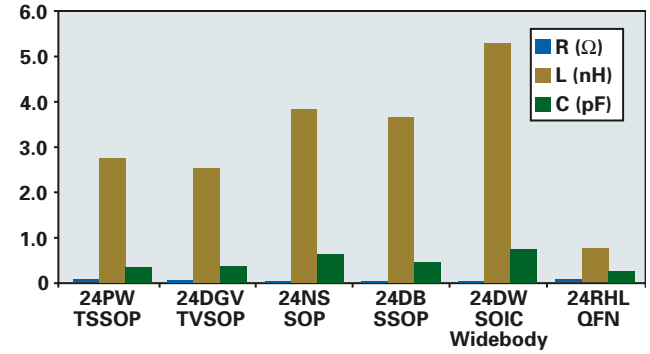
20-RGY Electrical Comparison



16-RGY Electrical Comparison



24-RHL Electrical Comparison



Thermal Characteristics

The tables give data for thermal impedance versus air flow, which show when thermal dissipation is crucial, the QFN package has an advantage over standard dual- and quad-leaded packages. The leadframe die pad is exposed at the bottom of the package and should be soldered to a properly designed thermal pad in the PWB. This provides a more direct heatsink path from the die to the board, and the addition of thermal vias from the thermal pad to an internal ground plane will dramatically increase power dissipation. Soldering the exposed pad also significantly improves board-level reliability during temperature cycling, key push, package shear drop test and similar board-level tests.

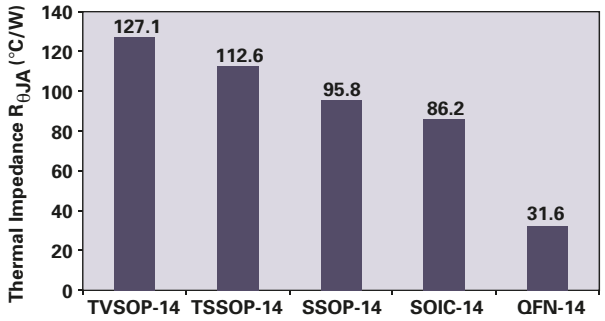
The bar graphs compare the junction-to-ambient thermal impedance of the QFN packages to popular packaging alternatives. These modeled values are on the applicable high-thermal-conductivity boards, per JESD 51-5.

Thermal data shown is an approximation based on modeling.

14-Pin QFN per JESD 51-5 (1S2P Direct-Attach Method)

	Airflow (linear ft/minute)			
	0	150	250	500
$R_{\theta JA}$ (°C/W)	31.6	25.1	23.1	21.4
$R_{\theta JC}$ (°C/W)	17.37	–	–	–
$R_{\theta JB}$ (°C/W)	4.9	–	–	–
$R_{\theta JP}$* (°C/W)	0.75	–	–	–

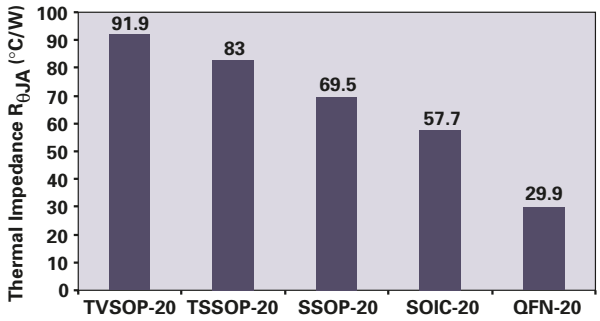
*$R_{\theta JP}$ = Resistance from junction to bottom of exposed pad.



20-Pin QFN per JESD 51-5 (1S2P Direct-Attach Method)

	Airflow (linear ft/minute)			
	0	150	250	500
$R_{\theta JA}$ (°C/W)	29.9	23.1	21.2	19.5
$R_{\theta JC}$ (°C/W)	15.2	–	–	–
$R_{\theta JB}$ (°C/W)	5.2	–	–	–
$R_{\theta JP}$* (°C/W)	0.52	–	–	–

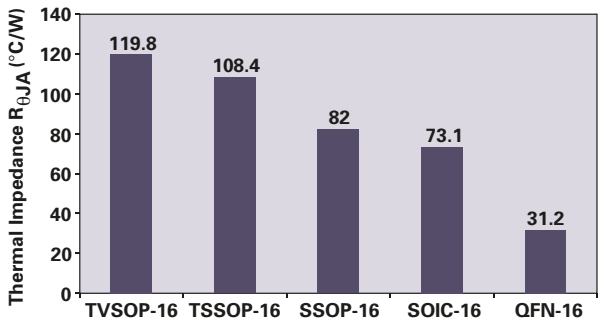
*$R_{\theta JP}$ = Resistance from junction to bottom of exposed pad.



16-Pin QFN per JESD 51-5 (1S2P Direct-Attach Method)

	Airflow (linear ft/minute)			
	0	150	250	500
$R_{\theta JA}$ (°C/W)	31.2	24.4	22.5	20.7
$R_{\theta JC}$ (°C/W)	16.23	–	–	–
$R_{\theta JB}$ (°C/W)	4.3	–	–	–
$R_{\theta JP}$* (°C/W)	0.6	–	–	–

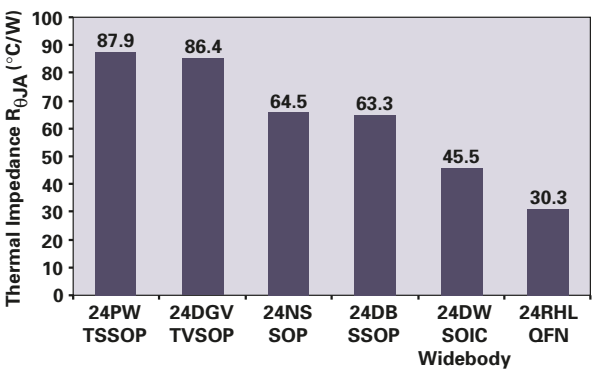
*$R_{\theta JP}$ = Resistance from junction to bottom of exposed pad.



24-Pin QFN per JESD 51-5 (1S2P Direct-Attach Method)

	Airflow (linear ft/minute)			
	0	150	250	500
$R_{\theta JA}$ (°C/W)	30.3	23.5	21.5	19.8
$R_{\theta JC}$ (°C/W)	13.3	–	–	–
$R_{\theta JB}$ (°C/W)	4.04	–	–	–
$R_{\theta JP}$* (°C/W)	0.50	–	–	–

*$R_{\theta JP}$ = Resistance from junction to bottom of exposed pad.



Sockets

Socket & Socket Manufacturer (Ordering Information)

Socket part numbers:

14 Pin: 14QN50T23535
16 Pin: 16QN50T23030
20 Pin: 20QN50T14535

Plastronics
2601 Texas Drive
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Board-Level Reliability Data

RGY units have passed 3000 cycles. Testing stopped at 8000 cycles.

Temperature Cycle

Board Level Reliability* (cycles to first failure)			
14 RGY		20 RGY	
Failure	Cycles	Failure	Cycles
1	3250	1	6712
2	5622	2	6712
3	5763	3	7140

*0.8-mm thick FR4 board.
IPC-9701, TC3 (–40 to 125°C, one cycle per hr).
SnAgCu solder paste, NiAu pad finish.

Drop Test

Conditions: 1500G, 1 millisecond pulse.
SnPb and Pb-Free soldered units pass > 40 drops.

Questions and Answers

Q. What is a QFN?

A: Quad Flat No-Lead (QFN) is a leadless package with peripheral terminal pads, and an exposed die pad for mechanical and thermal integrity. The package can be either square or rectangular.

Q: What applications should I consider using QFN packages in?

A: QFN package could be used in a variety of applications. Applications requiring low standoff heights, improved thermal performance, reduced size or reduced weight are good candidates for QFN design-in. Cell phones, PDAs, portable music and video players can significantly benefit from this package.

Q: How does QFN pin-out compare to TSSOP, SOIC or SSOP?

A: The new QFN package offerings from TI allow for a conventional pin-out scheme similar to traditional dual in-line packages. Function to pin number assignments in QFN are assigned the same pin number as TSSOP and other dual in-line packages.

Q: Is this a lead-free (Pb-Free) package?

A: Yes, these QFN packages are Pb-Free with matte tin finish (in transition with NiPdAu), and comply with lead-free environmental policies. The finish is two-way compatible, meaning both Pb-Free pastes and SnPb pastes solder well. The Pb-Free solder recommendation is the SnCuAg metallurgy. Check with your local TI Field Sales representative (listed on the last page) for sample availability.

Q: What size land pad should I design on my board for these packages?

A: Land-pad and exposed-pad design are the keys to board-level reliability, and TI strongly recommends following the design rules included in the application note, which complies with IPC-SM-782. Experimentation with QFN packages of similar size has shown these packages can easily withstand greater than 1000 cycles from –40 to 125°C on a 0.8-mm thick PCB with NiAu pads with the exposed pad soldered. Data has shown characteristic life values of >3000 cycles.

Q: What routing choices do I have when using QFN packages?

A: Single layer routing or standard via outside the package outline is feasible because of flow-through design.

Q: Can I mount QFN packages on the bottom side of the PCB?

A: Yes you can. The ideal second reflow profile is the same as the first (reflow profile is recommended in the application note). The package is adequately secured during the second reflow as long as the exposed pad is soldered. TI recommends designing stencils per the application note, which complies with IPC-SM-782.

Q: Can the packages be reworked on the boards?

A: Yes, there are rework and repair tools and equipment available. Rework processes will not differ significantly from BGA processes.

Q: How do QFN board assembly yields compare to BGAs?

A: The yields have been proven to be similar.

Q: What alignment accuracy is possible?

A: Alignment accuracy for the 0.50-mm pitch package is dependent on board level pad tolerance, placement accuracy and terminal lead position tolerance. Nominal terminal lead position tolerances are specified at ±50 microns.

Q: Are there specific recommendations for SMT processing?

A: TI recommends using a terminal lead for the alignment of QFN packages. This method is the most accurate assuming the machine is capable of indexing off the terminal lead, but this method could be slower than using the package outline for alignment. The package outline can also be used for alignment, but this could result in less accurate placement. Process characterization of placement, paste characteristics, stencil yield and reflow parameters should be accomplished so the placement process chosen requires minimal time, and self alignment corrects minor placement deviations.

Q: Can the solder joints be inspected after reflow?

A: Visual inspection can be used to inspect the outside part of the solder joint. Standard BGA inspection processes such as lamographic X-ray techniques can be used for a more thorough inspection.

IPC does not require side fillers for these package types, so the side joints may or may not be present. If side joints are not present, X-ray must be used.

Q: Can I probe test a mounted QFN?

A: Yes. Peripheral solder joints may be probed, and grounded exposed pads can be probed at the ends of the package where the tie bar has been exposed.

Q: Do I need to solder the exposed die pad to the board?

A: Power dissipation is greatly enhanced by soldering the exposed die pad to the board, and the board level reliability during temperature cycling and other board/package stress tests is greatly improved.

Q: Can I use thermal vias under the exposed pad/PWB interface?

A: Using thermal vias enhances power dissipation by approximately 20%. If your application requires enhanced thermal performance, thermal vias will help.

Q: Any EMI concerns for traces under the package and how can customers design their board to minimize EMI?

A: EMI can be controlled by minimizing any complex current loops on the PCB trace. Some helpful hints include: Solid ground and power planes should be used in the design. Partitioned ground and power planes must be avoided. These ground and power partitions may create complex current loops increasing radiation. Avoid right angles or "T" crosses on the trace. Right angles can cause impedance mismatch and increase trace capacitance causing signal degradation. Minimize power supply loops by keeping power and ground traces parallel and adjacent to each other. Significant package EMI can be reduced by using this method.

Q: What are the standard shipping quantities?

A: Currently, tape and reel quantities of 1000 units are available.

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