

SN74AXC8T245 Evaluation Module

This user's guide describes the characteristics, operation, and use of the SN74AXC8T245EVM Evaluation Module (EVM). A complete printed-circuit board layout, schematic diagrams, and bill of materials are included in this document.

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1 Introduction

The SN74AXC8T245EVM helps evaluate the operation of the SN74AXC8T245 device belonging to the AXC direction-controlled translation family. The board is setup to also accommodate the AVC and LVC family of direction-controlled translation devices.

1.1 Features

The SN74AXC8T245 is a dual-supply bus transceiver with configurable voltage translation and an operating range from 0.65 V to 3.6 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 0.65 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 0.65 V to 3.6 V. This device is fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry disables the outputs, thus preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at ground, both A and B data I/O ports are in the high-impedance state. There are two direction control pins, each controlling 4 data I/Os enabling independent and simultaneous up and down translation. The DIR1 pin controls the direction of data I/O channels 1 through 4, and the DIR2 pin controls the direction of data I/O channels 5 through 8. The functional table of the SN74AXC8T245 is listed in Table 1.

OE	DIR1	DIR2	Signal Direction
Н	Х	Х	Hi-Z
L	L	L	B to A
L	L	Н	B{1:4} to A{1:4} and A{5:8} to B{5:8}
L	Н	L	A to B
L	Н	Н	A{1:4} to B{1:4} and B{5:8} to A{5:8}

Table 1. SN74AXC8T245 Functional Table



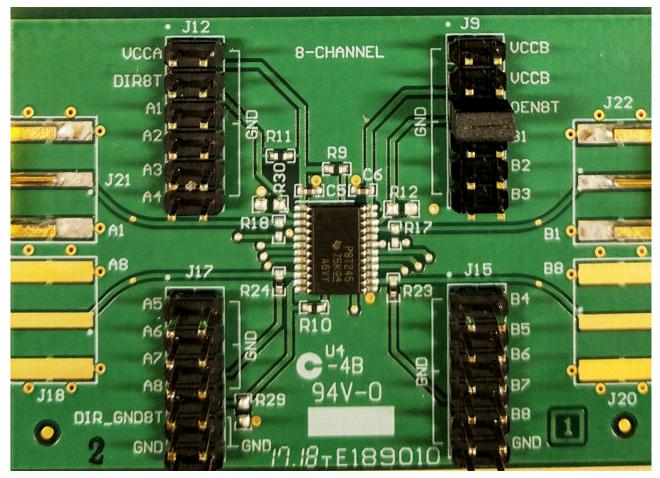


Figure 1. SN74AXC8T245EVM: 8-Channel PW Package

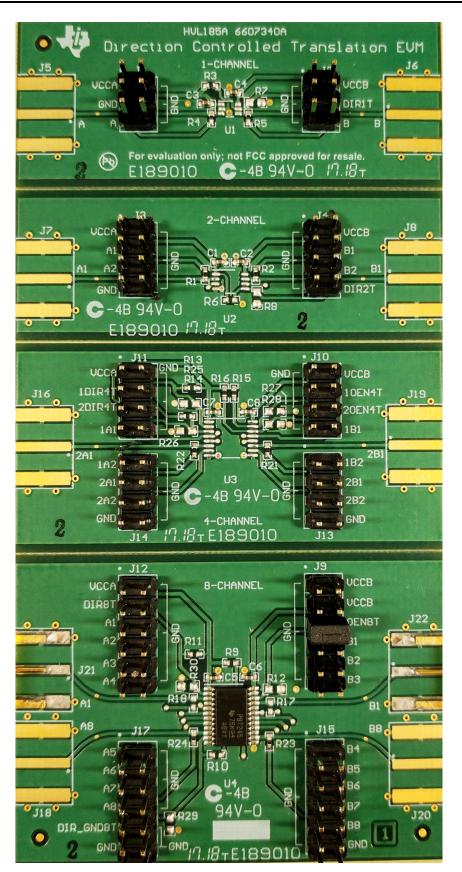


Figure 2. SN74AXC8T245EVM: 8, 4, 2, 1 Channel versions

The SN74AXC8T245EVM has the TSSOP (PW) package footprint, however, the device is also available in QFN (RHL) and Micro-QFN (RKT) packages. The various packages which the EVM supports are listed in Table 2.

Version	Package	Device Populated
One Channel	DCK	No
Two Channel	DCT	No
Four Channel	PW	No
Eight Channel	PW	Yes

Table 2. EVM Package Options

The EVM is generically built and therefore it supports various devices as listed in Table 3.

Version	Supported Devices	Order Samples
	SN74AVC1T45	SN74AVC1T45 samples
One Channel	SN74AVCH1T45	SN74AVCH1T45 samples
One Channel	SN74LVC1T45	SN74LVC1T45 samples
	SN74LVC1T45-Q1	SN74LVC1T45-Q1 samples
	SN74AVC2T45-Q1	SN74AVC2T45-Q1 samples
	SN74LVC2T45-Q1	SN74LVC2T45-Q1 samples
Two Channel	SN74AVC2T45	SN74AVC2T45 samples
	SN74AVCH2T45	SN74AVCH2T45 samples
	SN74LVC2T45	SN74LVC2T45 samples
	SN74AVC4T245	SN74AVC4T245 samples
Four Channel	SN74AVCH4T245	SN74AVCH4T245 samples
	SN74AVC4T245-Q1	SN74AVC4T245-Q1 samples
	SN74AXC8T245 (Installed)	SN74AXC8T245
	SN74AXCH8T245	SN74AXCH8T245 samples
	SN74AVC8T245	SN74AVC8T245 samples
Eiste Obersel	SN74AVCH8T245	SN74AVCH8T245 samples
Eight Channel	SN74LVC8T245	SN74LVC8T245 samples
	SN74LVCH8T245	SN74LVCH8T245 samples
	SN74LVC8T245-Q1	SN74LVC8T245-Q1 samples
	SN74AVC8T245-Q1	SN74AVC8T245-Q1 samples

Table 3. Supported Devices

1.2 Hardware Description

1.2.1 Headers

The EVM has standard 100-mil headers with the side closer to the device connected to ground. The side farther away from the device is mapped to the device pinout for easier connection as seen in Figure 1. The silkscreen indicates the pin function.

1.2.2 Bypass Capacitors

C1, C3, C5, and C7 are the bypass capacitors for V_{CCA} while C2, C4, C6, and C8 are the bypass capacitors for V_{CCB} with a value of 0.1 μ F.



1.2.3 Pullup and Pulldown Resistors

The direction control and output enable pins are the inputs for the devices and should never be left floating. The CMOS inputs must be held at a known state, either V_{CC} or ground, to ensure proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs* (SCBA004). The default state in the EVM is referenced to V_{CCA} using a 10-k Ω pull-up resistor. There is also the option of connecting the inputs to ground using pull-down resistors, or directly to ground via jumper on the header pins. *In order to enable the SN74AXC8T245EVM*, *connect a jumper on the OE pin to ground as shown in Figure 1*. In order to use the eight-channel version devices other than the SN74AXC8T245 (i.e SN74AVC8T245), the pull-up resistor R10 must be removed and the jumper to the ground needs to be connected on DIR_GND8T.



Table 4 lists the pullup and pulldown resistors.

Device	Pin	Pullup	Pulldown
One Channel ⁽¹⁾	DIR	R3	R7
Two Channel ⁽²⁾	DIR	R6	R8
	DIR1	R13	R25
Four Channel ⁽³⁾	DIR2	R14	R26
Four Channel	10EN	R15	R27
	20EN	R16	R28
Eight Channel	DIR1	R11	R30
(SN74AXC8T245 OR	DIR2	R10	R29
SN74AXCH8T245)	OEN	R9	R12

Table 4. Pullup and Pulldown Resistors

 $^{(1)}$ $\,$ One channel considering SN74AVC1T45 or SN74LVC1T45 $\,$

⁽²⁾ Two channel considering SN74AVC2T45 or SN74LVC2T45

⁽³⁾ Four channel considering SN74AVC4T245

1.2.4 SMB Connectors

The edge-mounted SMB connector option is provided for each of the channel versions on data I/O pins of A1 and B1, respectively, for high-speed operation. One pair of SMB connector is installed on the A1 and B1 data I/O pair of the SN74AXC8T245 while the corresponding header pin has an uninstalled 0- Ω resistor R18 and R17. The data I/O pins A8, B8 also have the uninstalled SMB connector option with 0- Ω resistors to headers.

7

Introduction

Board Layout

2 Board Layout

Figure 3 illustrates the EVM layout. Increase zoom level for clarity.

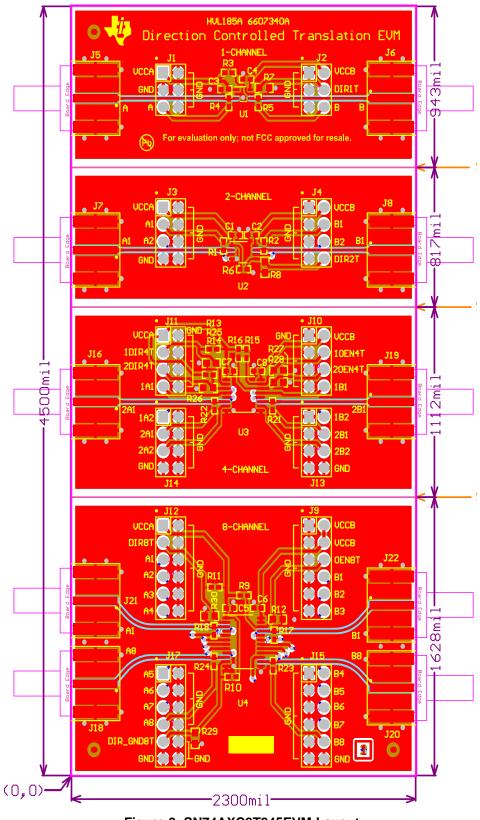


Figure 3. SN74AXC8T245EVM Layout



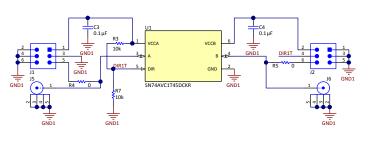
3 Schematic and Bill of Materials

3.1 Schematic

Figure 4 illustrates the EVM schematic. Increase the zoom level for clarity.

> R27 R28 10k R28

1-CHANNEL



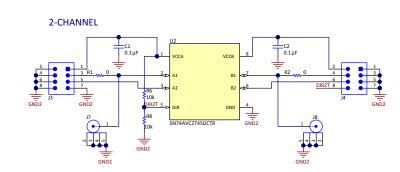
GND GND

GND

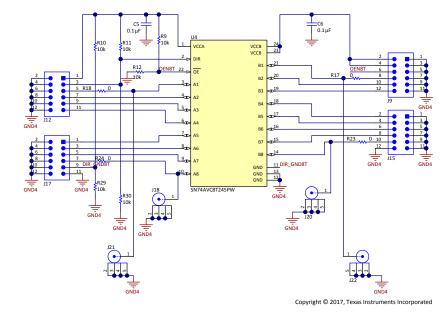
SN74AVC4T245PW

4-CHANNEL

R22 0



8-CHANNEL





GND3

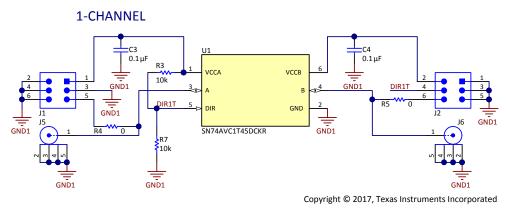
R25

R26

GND3

GND:







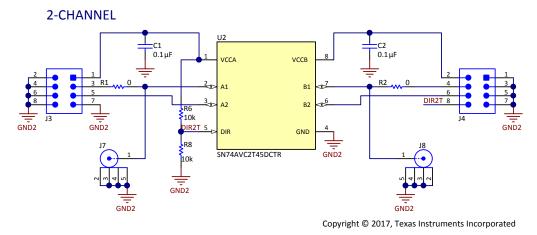


Figure 6. Two Channel

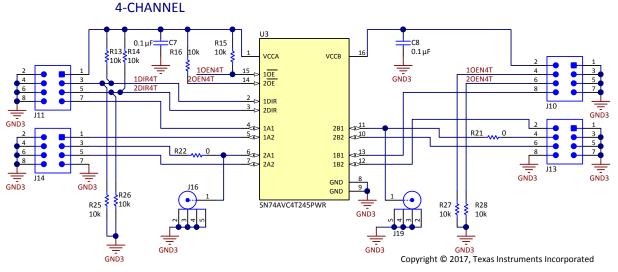
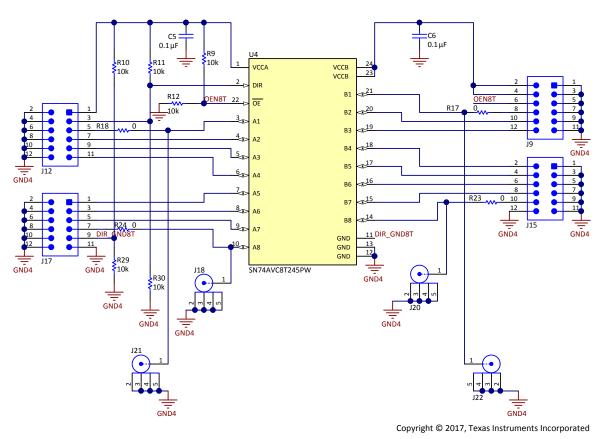


Figure 7. Four Channel



8-CHANNEL







Schematic and Bill of Materials

3.2 Bill of Materials

Table 5 lists the EVM bill of materials.

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		6607340	Any
C1, C2, C3, C4, C5, C6, C7, C8	8	0.1uF	CAP, CERM, 0.1 μF, 16 V, +/- 10%, X7R, 0402	0402	0402YC104KAT2A	AVX
J1, J2	2		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J3, J4, J10, J11, J13, J14	6		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J9, J12, J15, J17	4		Header, 100mil, 6x2, Gold, TH	6x2 Header	TSW-106-07-G-D	Samtec
J21, J22	2		Connector, SMB Jack, End launch, SMT	SMB End launch Jack, SMT	131-3701-801	Emerson Network Power
R1, R2, R4, R5, R21, R22, R23, R24	8	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
R3, R6, R9, R10, R11, R13, R14, R15, R16	9	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale
U4	1		Asynchronous Communication Between Data Buses, PW0024A (TSSOP-24)	PW0024A	SN74AXC8T245PWR	Texas Instruments
J5, J6, J7, J8, J16, J18, J19, J20	0		Connector, SMB Jack, End launch, SMT	SMB End launch Jack, SMT	131-3701-801	Emerson Network Power
R7, R8, R12, R25, R26, R27, R28, R29, R30	0	10k	RES, 10 k, 5%, 0.1 W, 0603	0603	CRCW060310K0JNEA	Vishay-Dale
R17, R18	0	0	RES, 0, 5%, 0.063 W, 0402	0402	ERJ-2GE0R00X	Panasonic
U1	0		Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting DCK0006A (SOT-6)	DCK0006A	SN74AVC1T45DCKR	Texas Instruments
U2	0		Dual-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation, DCT0008A (SSOP-8)	DCT0008A	SN74AVC2T45DCTR	Texas Instruments
U3	0		4-Bit Dual-Supply Bus Transceiver with Configurable Voltage-Level Shifting, PW0016A (TSSOP-16)	PW0016A	SN74AVC4T245PWR	Texas Instruments

Table 5. SN74AXC8T245EVM Bill of Materials

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