Product Overview
Combine Power Good Signals

TEXAS INSTRUMENTS
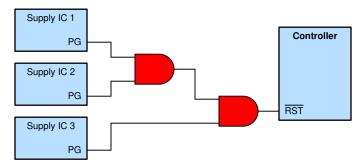
Power supply IC (LDOs, converters, PMICs) power-good outputs often have weak open-drain drivers. This fact combined with the common practice of physically separating a supply from the the digital and analog processing subsystems can result in very long traces. Long traces result in large parasitic capacitances and can negatively affect signal integrity. By adding a strong push-pull CMOS driver, the signal is improved. At the same time, signals can be combined through simple logic to reduce the number of inputs required.

See more about this use case in the *Logic Minute* video *Combining Power Good Signals*.

Design Considerations

- Open-drain outputs require pullup resistors
- Keep traces to the logic gate inputs relatively short to reduce capacitive loading and improve performance
- High-drive balanced CMOS output logic improves signal integrity while reducing the number of inputs required
- *[FAQ] How does a slow or floating input affect a CMOS device?*
- *[FAQ] Where do I find maximum power dissipation for a device?*
- Ask a question on our *Engineer-to-Engineer forum*

Recommended Parts

Part Number	AEC-Q100	V_{CC} Range	Channels	Features
SN74LVC1G08		1.65 V — 5.5 V	1	High Drive Strength - 32 mA
SN74LVC1G08-Q1	✓			
SN74AUP1G08		0.8 V — 3.6 V	1	Low power - Icc < 0.9 µA
SN74AUP1G08-Q1	✓			
SN74HCS08		2 V — 6 V	4	Schmitt-trigger inputs
SN74HCS08-Q1	✓			

For more devices, browse through the *online parametric tool* where you can sort by desired voltage, channel numbers, and other features.

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