*Application Report*

# *TCA9539-Q1 Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for TCA9539-Q1 (PW package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

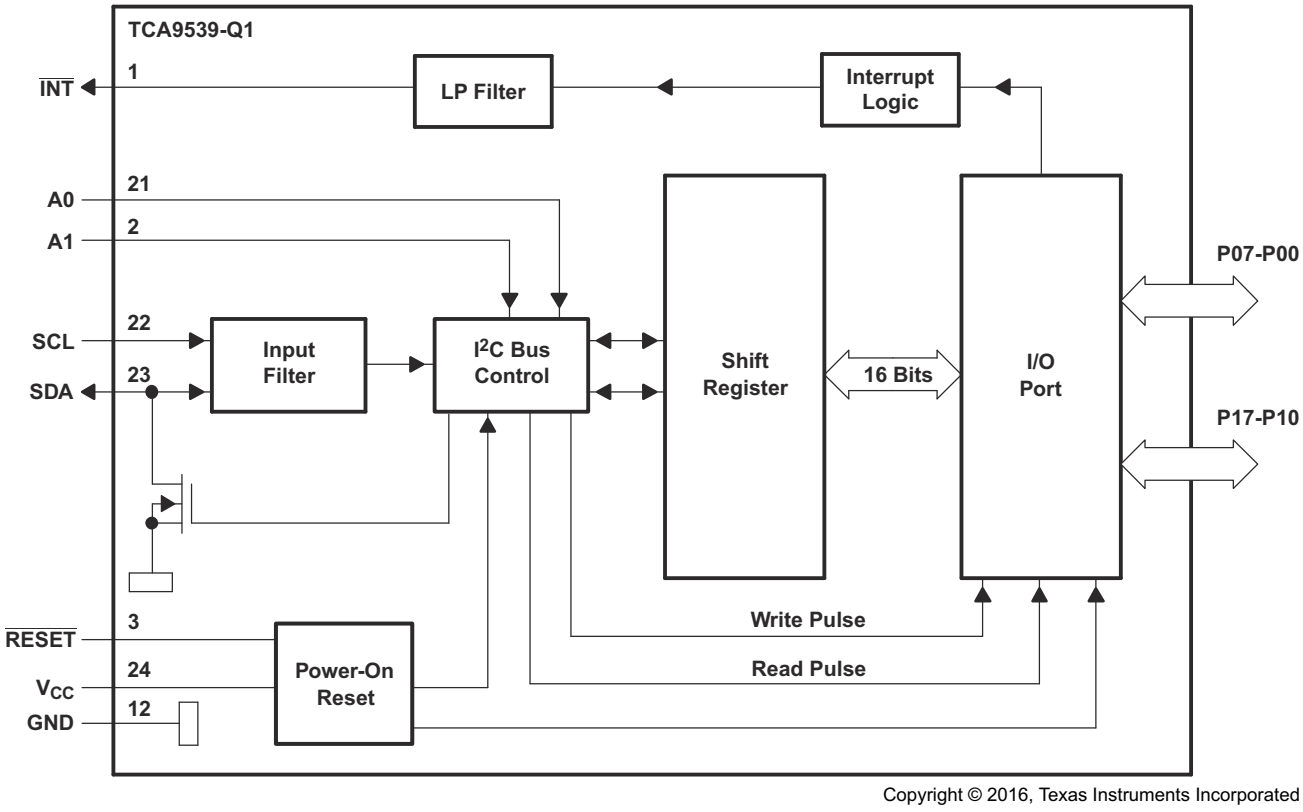


**Figure 1-1. Functional Block Diagram**

TCA9539-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCA9539-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total Component FIT Rate | 16 |
| Die FIT Rate | 2 |
| Package FIT Rate | 14 |

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 35 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 5 | CMOS, BICMOS<br>Digital, analog / mixed | 25 FIT | 55°C |

The Reference FIT Rate and Reference Virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for *TCA9539-Q1* in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| I2C control / communication error | 40% |
| I/O data bit error | 40% |
| I/O configuration error | 15% |
| INT false trip, fails to trip | 5% |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCA9539-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

Figure 4-1 shows the TCA9539-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the *TCA9539-Q1* data sheet.

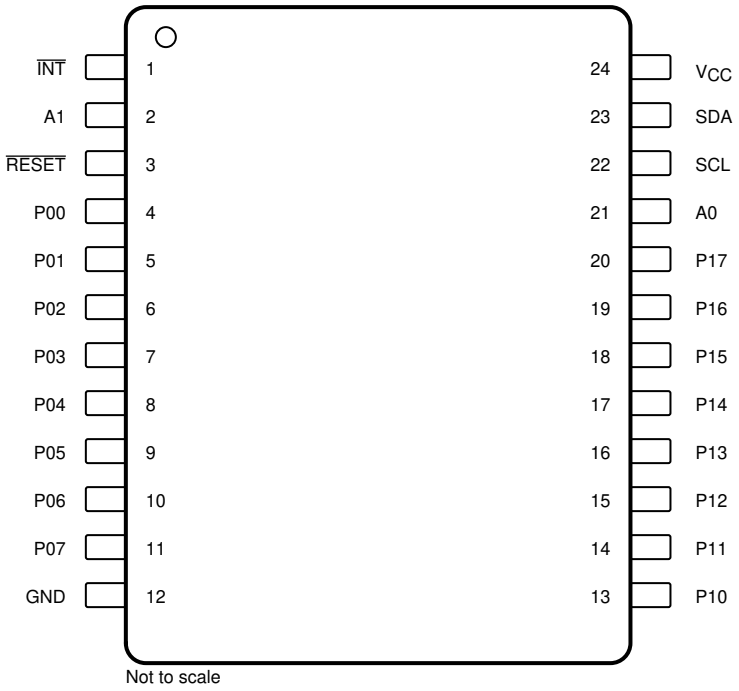


**Figure 4-1. Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- SDA/SCL/RESET/INT/PXX are pulled high with an external pull up resistor

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| INT | 1 | INT stuck low resulting in functionality loss, no device damage/harm expected | B |
| A1 | 2 | Device address A1 forced low, potential functionality lost if state was previously high. No device harm expected | B |

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 3 | Device is held in RESET. No device harm expected, but functionality loss due to NACKs and p-ports remain HI-Z inputs. | B |
| P00 | 4 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P01 | 5 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P02 | 6 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P03 | 7 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P02 | 8 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P05 | 9 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P06 | 10 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P07 | 11 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| GND | 12 | GND shorted to GND, no issues expected | D |
| P10 | 13 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P11 | 14 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P12 | 15 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P13 | 16 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P14 | 17 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P15 | 18 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P16 | 19 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| P17 | 20 | Potential damage if pin is configured to be an output HIGH and High ICC current. Damage to internal PFET may occur due to over current event. If pin is configured as an input or output low, no damage is expected. | A |
| A0 | 21 | Device address A0 forced low, potential functionality lost if state was previously high. No device harm expected | B |
| SCL | 22 | SCL stuck low resulting in functionality lost, no device damage expected. I2C bus would be stuck on the system level | B |
| SDA | 23 | SDA stuck low resulting in functionality lost, no device damage expected. I2C bus would be stuck on the system level | B |

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| $V_{CC}$ | 24 | Device would be held in reset and all functionality would be lost. All PXX pins would become HIGH-Z. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| INT | 1 | The INT pin is no longer asserted low, the processor is not informed of any INTs. No damage expected | B |
| A1 | 2 | Device address could float and the device slave address would be unknown (potential functional problem) and in worst case, it may become an address which is already occupied by another slave on the bus. No damage expected. | B |
| RESET | 3 | Device pin may float to an unknown state, if floats to LOW then the device is held in reset and is unresponsive (functional issue) | B |
| P00 | 4 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P01 | 5 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P02 | 6 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P03 | 7 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P04 | 8 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P05 | 9 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P06 | 10 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P07 | 11 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| GND | 12 | Device is not biased to GND, potential damage to device may occur. | A |
| P10 | 13 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality islost. No harm to device is expected. | B |
| P11 | 14 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P12 | 15 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality will be lost. No harm to device is expected. | B |
| P13 | 16 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |
| P14 | 17 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, it no longer drives the pin. Functionality is lost. No harm to device is expected. | B |

**Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| P15 | 18 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, will no longer be able to drive pin. Functionality is lost.<br>No harm to device is expected. | B |
| P16 | 19 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, will no longer be able to drive pin. Functionality is lost.<br>No harm to device is expected. | B |
| P17 | 20 | If pin is configured to be an input, larger supply current may occur. May trigger INT due to floating input. If configured as an output, itn can no longer drive the pin. Functionality is lost.<br>No harm to device is expected. | B |
| A0 | 21 | Device address could float and the device slave address is unknown (potential functional problem) and in worst case, it may become an address which is already occupied by another slave on the bus. No damage expected. | B |
| SCL | 22 | Larger supply current may occur due to this becoming a floating input. Functionality is lost due to I2C communication being cut off to this device. No damage expected.<br>When trying to communicate to the device, I2C shows NACKs when address is trying to be called. | B |
| SDA | 23 | Larger supply current may occur due to this becoming a floating input. Functionality will be lost due to I2C communication being cut off to this device. No damage expected.<br>When trying to communicate to the device, I2C shows NACKs when address is trying to be called. | B |
| $V_{CC}$ | 24 | Functionality is lost. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| INT | 1 | A1 | Device address may change if A1 is tied to a pull-up resistor whenever INT asserts. Address would change back when INT de-asserts.<br>If A1 is tied to a pull-down resistor, voltage at A1 may be at a mid voltage due to resistor divider between A1's pull down and INT's pull-up. Address of device may change due to any noise/coupling onto the pin. Increased leakage current on supply would be seen. When INT asserts, the address will set back to low. INT may also never go above $V_{iH}$ for any processor/mcu looking at the INT line. Additional leakage current may be expected at the processor/mcu input for the INT.<br>Functionality may be lost. | B |
| A1 | 2 | RESET | If A1 is tied to a pull-down resistor, A1 and RESET will form a voltage divider and the voltage at these pins will settle somewhere mid rail if pull-up and pull-down resistors are equal in value. RESET and device address may be in an unknown state because they are not above/below $V_{iH}$/$V_{iL}$ levels. Noise coupling onto these pins may toggle reset. Assume functionality is lost.<br>If A1 is tied HIGH and we assume RESET is tied HIGH with pull-up resistors, errors are expected. | B |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| RESET | 3 | P00 | If P00 is an INPUT (by default) and referenced with an external pull-up resistor then no functionality issues are expected.<br>If P00 is an INPUT (by default) and referenced with an external pull-down resistor then P00 and RESET will form a voltage divider and the voltage at these pins will settle somewhere mid rail if pull up and pull-down resistors are equal in value. RESET and P00 may be in an unknown state because they are not above/below $V_{iH}/V_{iL}$ levels. Noise coupling onto these pins may toggle reset. Assume functionality is lost.<br>If P00 is configured to be an OUTPUT HIGH, device would NOT be reset and functionality should be okay. Some additional leakage may be present.<br>If P00 is configured to be an OUTPUT LOW, device would be reset and then all GPIOs would return to their default power up state of an input. Functionality would be lost if P00 is ever configured to be an output LOW. | B |
| P00 | 4 | P01 | If P00 and P01 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P00 and P01 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P00 and P01 are both INPUTs, no damage is expected.<br>If P00 and P01 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P01 | 5 | P02 | If P01 and P02 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P01 and P02 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P01 and P02 are both INPUTs, no damage is expected.<br>If P01 and P02 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P02 | 6 | P03 | If P02 and P03 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P02 and P03 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P02 and P03 are both INPUTs, no damage is expected.<br>If P02 and P03 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P03 | 7 | P04 | If P03 and P04 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P03 and P04 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P03 and P04 are both INPUTs, no damage is expected.<br>If P03 and P04 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| P04 | 8 | P05 | If P04 and P05 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P04 and P05 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P04 and P05 are both INPUTs, no damage is expected.<br>If P04 and P05 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P05 | 9 | P06 | If P05 and P06 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P05 and P06 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P05 and P06 are both INPUTs, no damage is expected.<br>If P05 and P06 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P06 | 10 | P07 | If P06 and P07 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two will occur. If $I_{oH}$ exceeds 10mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P06 and P07 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P06 and P07 are both INPUTs, no damage is expected.<br>If P06 and P07 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P07 | 11 | GND | If P07 is set to an OUTPUT LOW, no functionality or damage is expected.<br>If P07 is an INPUT, no damage is expect, but functionality is lost as P07 will likely not see a logic HIGH and set the INT.<br>If P07 is an OUTPUT HIGH, damage is likely to occur as a large $I_{oH}$ current flows from the pin and likely exceed the $V_{oH}$ limit. | A |
| P10 | 13 | P11 | If P10 and P11 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P10 and P11 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P10 and P11 are both INPUTs, no damage is expected.<br>If P10 and P11 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P11 | 14 | P12 | If P11 and P12 are OUTPUTs, but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P11 and P12 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P11 and P12 are both INPUTs, no damage is expected.<br>If P11 and P12 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| P12 | 15 | P13 | If P12 and P13 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P12 and P13 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P12 and P13 are both INPUTs, no damage is expected.<br>If P12 and P13 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P13 | 16 | P14 | If P13 and P14 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P13 and P14 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P13 and P14 are both INPUTs, no damage is expected.<br>If P13 and P14 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P14 | 17 | P15 | If P14 and P15 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P14 and P15 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P14 and P15 are both INPUTs, no damage is expected.<br>If P14 and P15 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P15 | 18 | P16 | If P15 and P16 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P15 and P16 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P15 and P16 are both INPUTs, no damage is expected.<br>If P15 and P16 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |
| P16 | 19 | P17 | If P16 and P17 are OUTPUTs but logic levels are not the same (one is OUTPUT LOW and other is OUTPUT HIGH), then contention between the two occurs. If $I_{oH}$ exceeds 10 mA then damage may occur but may not be instantaneous. Failures overtime may occur.<br>If P16 and P17 are OUTPUTs and logic levels are the same (both are OUTPUT HIGH or OUTPUT LOW), no damage is expected but some leakage current may occur.<br>If P16 and P17 are both INPUTs, no damage is expected.<br>If P16 and P71 are configured such that the pair is an OUTPUT and an INPUT, then no damge is expected. | A |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|---|
| P17 | 20 | A0 | If P17 is an INPUT, no expected damage. Functionality may be lost depending on what is connected to P17 in the system which is now also connected to A0.<br>If P17 is an OUTPUT HIGH and A0 is referenced to a pull up to Vcc or if P17 is an OUTPUT LOW and A0 is referenced to a logic low, then no functionality or damage is expected.<br>If P17 is an OUTPUT HIGH and A0 is referenced to a low through a resistor or P17 is an OUTPUT LOW and A0 is referenced to a logic HIGH through a resistor, then A0 will now be a different state than intended/designed for. The processor will not be able to access the intended slave. If another slave shares the same address as this device, then signal integrity issues may be a concern. Device may end up being programmed incorrectly/unintentionally in this case. Functionality may be lost due to this. Direct damage is not expected though depending on how the system implements the GPIOs, damage may be possible due to unintended programming. | B |
| A0 | 21 | SCL | A0 will change its address during I2C communication, potential address conflict is possible. Device's state machine may NACK its own address if A0 were referenced HIGH during the ACK pulse due to SCL driving A0 low. Functionality will be lost and potential additional leakage current if A0 is referenced to LOW through a pull down due to SCL's pull up (voltage divider forms) during the idle state. | B |
| SCL | 22 | SDA | I2C communication will be lost both to the device and to the system's I2C bus. Functionality is lost, but no damage expected. | B |
| SDA | 23 | $V_{CC}$ | Device is likely to be damaged during ACKs and read transaction due to large excessive current through pin. If $I_{oL}$ exceeds 6 mA at 85°C or less, device may be damaged. Damage may not be instanteous but may occur over time. $V_{oL}$ from device may also be too large for master to accept as a valid low during ACKs. | A |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| INT | 1 | If INT is de-asserted/HIGH then there should not be concerns outside of potential leakage currents.<br>When INT asserts, large $I_{oL}$ current flows from $V_{CC}$ to GND through the INT pin, if $V_{CC}$ of device is low then the NFET (of INT) saturates and $V_{oL}$ on INT clamps as well as the $I_{oL}$ current. Damage may occur if $I_{oL}$ is larger than 6 mA at 85°C or below. At 105°C, $I_{oL}$ should not go above 3 mA. If $V_{CC}$ were a larger value, then the $V_{oL}$ and $I_{oL}$ current are much larger and likely to surpass the 6 mA limit at 85°C and below. Damage would be expected, but may not break the device instantly, likely damage over time.<br>From a system level, processor looking at the INT may not see an interrupt as the $V_{oL}$ could be larger than the $V_{iL}$ of a processor. | A |
| A1 | 2 | If A1 is tied to a pull up voltage, then there should be no concerns outside of leakage currents.<br>If A1 is referenced to GND with a pull up resistor, then the device interprets A1 as a logic HIGH and the master/processor is not able to communicate to the device (slave address has changed). If there is another device on the bus with the same address, then there could be signal integrity concerns or GPIOs could be set to the wrong settings.<br>Worst case is A1 is tied directly to GND. If $V_{CC}$ were shorted to A1 in this case, ther is a direct short to GND. No damage is expected to our device, but may cause damage to power supplying rail | B |
| RESET | 3 | If RESET is tied to a pull up voltage, then there should be no concerns outside of leakage currents. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| P00 | 4 | If P00 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P00 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25mA at 85C or lower then the device may be damaged. If P00 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P01 | 5 | If P01 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P01 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P01 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P02 | 6 | If P02 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P02 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P02 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P03 | 7 | If P03 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P03 is set to an OUTPUT LOW, then large current from Vcc to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P03 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P04 | 8 | If P04 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P04 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P04 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P05 | 9 | If P05 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P05 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P05 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P06 | 10 | If P06 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P06 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P06 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P07 | 11 | If P07 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P07 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P07 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| GND | 12 | Device may be damaged due to biasing of internal substrates which were previously only supposed to be biased to GND. | A |
| P10 | 13 | If P10 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P10 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P10 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P11 | 14 | If P11 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P11 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P11 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P12 | 15 | If P12 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P12 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P12 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P13 | 16 | If P13 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents. If P13 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged. If P13 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)**

| Pin Name | Pin No. | Description of Potential Failure Effect(s) | Failure Effect Class |
|---|---|---|---|
| P14 | 17 | If P14 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents.<br>If P14 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged.<br>If P14 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P15 | 18 | If P15 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents.<br>If P15 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged.<br>If P15 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P16 | 19 | If P16 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents.<br>If P16 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged.<br>If P16 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| P17 | 20 | If P00 is set to an OUTPUT HIGH, then there should be no concerns outside of leakage currents.<br>If P00 is set to an OUTPUT LOW, then large current from $V_{CC}$ to GND through the pin is expected. If current exceeds 25 mA at 85°C or lower then the device may be damaged.<br>If P00 is set to an INPUT, then there should be no concerns outside of leakage currents. | A |
| A0 | 21 | If A0 is tied to a pull up voltage, then there should be no concerns outside of leakage currents.<br>If A0 is referenced to GND with a pull up resistor, then the device will now interpret A0 as a logic HIGH and the master/processor will not be able to communicate to the device (slave address has changed). If there is another device on the bus with the same address, then there could be signal integrity concerns or GPIOs could be set to the wrong settings.<br>Worst case is A0 is tied directly to GND. If $V_{CC}$ were shorted to A1 in this case, we would have a direct short to GND. No damage is expected to our device but may cause damage to power supplying rail | B |
| SCL | 22 | SCL is an input, so no damage is expected to the device. The device may not see a valid $V_{oL}$ though as the master will likely have a larger $V_{oL}$ due to the excess current. Worst case for device is lose of I2C communication due to $V_{oL}$ master > $V_{iL}$ device.<br>Damage to the processor may occur or any device which supports clock stretching. | B |
| SDA | 23 | Device is likely to be damaged during ACKs and read transaction due to large excessive current through pin. If $I_{oL}$ exceeds 6 mA at 85°C or less, device may be damaged. Damage may not be instanteous but may occur over time.<br>$V_{oL}$ from device may also be too large for master to accept as a valid low during ACKs. | A |
| $V_{CC}$ | 24 | $V_{CC}$ is shorted to $V_{CC}$, this is expected and no damage should occur. | D |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (October 2020) to Revision A (April 2021)** **Page**

- Updated Table 4-2 ..... 5

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