Functional Safety Information

TLVH431A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TLVH431A-Q1 (DBV package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

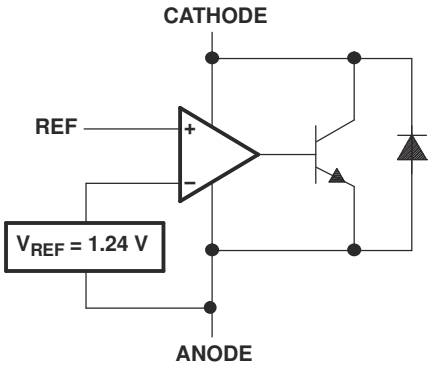


Figure 1-1. Functional Block Diagram

The TLVH431A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TLVH431A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

TABLE	CATEGORY	REFERENCE FIT RATE	REFERENCE VIRTUAL T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLVH431A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Cathode or Anode open (HIZ)	25
Cathode to Anode short	35
Cathode not in specification voltage or current	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLVH431A-Q1 (DBV package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to Cathode pin (see Table 4-5)

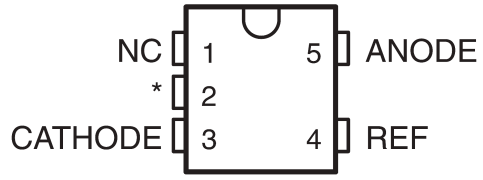
Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TLVH431A-Q1 pin diagram for the DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLVH431A-Q1 data sheet.

DBV (SOT-23-5) PACKAGE
(TOP VIEW)



NC – No internal connection

* Pin 2 is attached to Substrate and must be connected to ANODE or left open.

Figure 4-1. Pin Diagram (DBV) Package

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- CATHODE is connected to VDD through a series resistor
- ANODE is connected to the ground
- REF is connected to ground and cathode via resistors as shown in the Figure 4-2
- NC and * pin is left floating

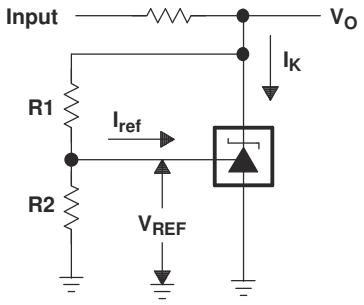


Figure 4-2. Test Circuit for $V_{KA} > V_{REF}$

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	Normal Operation	D
*	2	Works fine when anode is connected to Ground but can affect application functionality otherwise	C
CATHODE	3	Potential damage to the device depending on the location of the short. Shorts output voltage to ground, increases system current	A
REF	4	Turns off the regulator. No damage to device but can affect application functionality	B
ANODE	5	Works fine when anode is connected to Ground but can affect application functionality otherwise	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	Normal Operation	D
*	2	Normal Operation	D
CATHODE	3	No damage to device but can affect application functionality	C
REF	4	No damage to device but can affect application functionality	C
ANODE	5	No damage to device but can affect application functionality	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	*	Normal Operation	D
*	2	CATHODE	Potential damage to the device depending on the location of the short. Shorts output voltage to ground, increases system current	A
CATHODE	3	REF	Works fine when used in ref to cathode direct feedback but can affect application functionality otherwise	C
REF	4	ANODE	Turns off the regulator. No damage to device but can affect application functionality	B
ANODE	5	NC	Normal Operation	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Cathode

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	Normal Operation	D
*	2	Potential damage to the device depending on the location of the short. Shorts output voltage to ground, increases system current	A
CATHODE	3	Normal Operation	D
REF	4	Works fine when used in ref to cathode direct feedback but can affect application functionality otherwise	C
ANODE	5	Potential damage to the device depending on the location of the short. Shorts output voltage to ground, increases system current	A

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