Functional Safety Information

XTR111
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the XTR111 (HVSSOP and VSON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

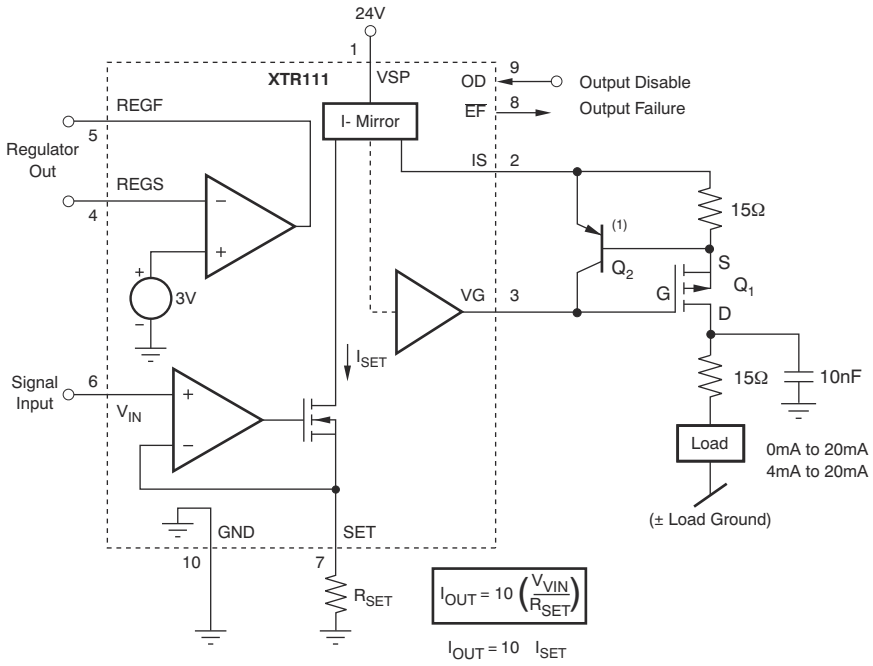

Figure 1-1. Functional Block Diagram

The XTR111 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 HVSSOP Package

This section provides functional safety failure in time (FIT) rates for the HVSSOP package of the XTR111 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	17
Die FIT rate	13
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 862 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	8 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the XTR111 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	20
Die FIT rate	15
Package FIT rate	5

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 862 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	12 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the XTR111 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20%
Output saturated high	25%
Output saturated low	25%
Output functional, not in specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the XTR111 (HVSSOP and VSON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- *Short circuit to Supply* means short to VSP.
- *Short circuit to Ground* means short to GND.
- The OD pin is driven by an external control signal. When the signal is low, the device output is enabled, and when the signal is high, the device output is disabled. Thus, although not a functional requirement for the device, the Output Disable function is variable (can be toggled) rather than fixed.
- The EF pin is monitored by external circuitry for use elsewhere in the system (not a functional requirement for the device).
- REGF is used to power other circuitry in the system, and is configured to a voltage other than 3 V through the use of a voltage divider, as shown in Figure 45b of the XTR111 data sheet (not a functional requirement for the device).

4.1 HVSSOP Package

Figure 4-1 shows the XTR111 pin diagram for the HVSSOP package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the XTR111 data sheet.

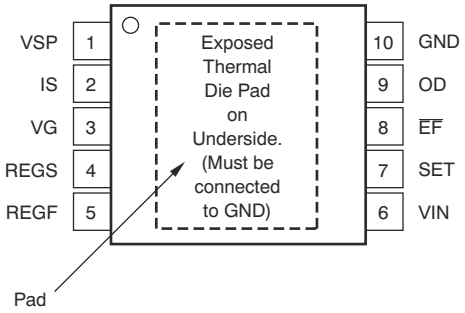

Figure 4-1. Pin Diagram (HVSSOP) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VSP	1	The device supplies are shorted together, leaving the VSP pin at some voltage between the VSP and GND sources (depending on source impedance).	A
IS	2	If the supply voltage is greater than 6.5 V, and the pin is not current limited to 50 mA, the device will be damaged.	A
VG	3	If the supply voltage is greater than 18 V, and the pin is not current limited to 25 mA, the device will be damaged. Additionally, the external FET and BJT will have a low voltage at the respective gate or collector. This low voltage causes erroneous or stuck device output current due to high V_{GS} voltage, which could theoretically damage the external FET.	A
REGS	4	The regulator voltage will be near the rail voltage, disrupting downstream circuitry that is powered from REGF.	B
REGF	5	The internal amplifier will try to force current through the short, maxing out at 15 mA to 25 mA.	B
VIN	6	The internal amplifier will rail out, completely disrupting the internal feedback mechanism, and result in erroneous output of device (stuck at 0 mA).	B
SET	7	Internal op-amp pins will be held apart, resulting in the op amp railing gate being driven high, and thus attempt to force more current out of the SET pin. This configuration completely disrupts the internal feedback mechanism, and results in erroneous output of device.	B
EF	8	The error flag will be stuck at low, meaning if read, the error flag will always indicate an error (such as a wire break) even if the device is actually working fine.	B
OD	9	The output will be stuck at enabled, meaning the output can no longer be disabled.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VSP	1	Device positive supply will float, potentially resulting in damage if external voltages are present at the device inputs.	A
IS	2	The external FET and BJT will not have any voltage at the respective source or emitter, giving no proper current path, and thus disrupting device output current.	B
VG	3	Pin voltage will likely drift up to the VSP rail. The external FET and BJT will have high voltage at the respective gate or collector, causing erroneous or stuck device output current due to a low V_{GS} voltage. Capacitive coupling to this open pin could cause oscillations in the device output.	B
REGS	4	Capacitive coupling to this open pin could cause oscillations in the device regulator output, disrupting any downstream circuitry that is powered from REGF. The pin voltage will probably float to one rail or the other.	B
REGF	5	Downstream circuitry will not be powered, which could cause erroneous circuit behavior.	B
VIN	6	Capacitive coupling to this open pin could cause oscillations in the gate drive output, which could in turn cause oscillations in the device output.	B
SET	7	With no path to GND other than through the inverting input, the internal op amp will rail to shut off the internal FET, completely disrupting the internal feedback mechanism, and result in erroneous output of device.	B
EF	8	If the EF pin is *open* and not connected to an external pullup resistor and monitoring circuitry, to that external circuit, the error flag will appear to be stuck at high. Therefore, if the device enters a state where an error is present (such as a wire break), the monitor circuit will not detect this error.	B
OD	9	The output will be stuck at disabled because of the internal pullup resistor on the OD pin, preventing the device output from being enabled. Possibility of glitches if a 4-µA internal pullup resistor is overpowered by capacitive coupling.	B
GND	10	The device negative supply will float, potentially resulting in damage if external voltages are present at the inputs.	A
PAD	P	The device will not be able to thermally dissipate and could overheat with high currents. Long-term reliability and structural integrity could be compromised.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VSP	1	2	The external FET and BJT will have higher voltage at the respective source or emitter than intended, causing erroneous device output current due to an incorrect V_{GS} voltage.	B
IS	2	3	The external FET and BJT will have the same voltage at the respective source or emitter as at the gate or collector, causing erroneous or stuck device output current due to a zero V_{GS} voltage.	B
VG	3	4	The regulator voltage will be disrupted. If the resistor divider used to set REGF uses low-value resistors, VG can become loaded, resulting in an erroneous gate drive.	B
REGS	4	5	The internal regulator acts as a buffer of the internal 3-V reference, which will lead to an incorrect REGF output voltage.	B
VIN	6	7	The amplifier inputs will be shorted out, so the amplifier will rail either high or low, leading to erroneous or stuck device output.	B
SET	7	8	The SET resistor acts as a pulldown resistor on the EF pin, possibly forming a resistor divider that disrupts EF functionality. The internal pullup resistor on EF forces some current through the SET resistor, causing a slight error in the output current of the device.	B
EF	8	9	If an external pullup resistor is used on the EF pin, this pullup resistor will fight any external pulldown resistor present on the OD pin, possibly forming a voltage divider that will cause a voltage at OD in between a true high or low. This configuration could force the output to be erroneously disabled or glitch. This configuration will also cause an in-between voltage on the EF pin, disrupting EF pin functionality.	B
OD	9	10	Output will be stuck at enabled, meaning that the output can no longer be disabled.	B
PAD	P	ALL	Same as *Short to GND*; see Table 4-2.	

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IS	2	The external FET and BJT will have a higher voltage at the respective source or emitter than intended, causing erroneous device output current due to an incorrect V_{GS} voltage.	B
VG	3	The external FET and BJT will have a high voltage at the respective gate or collector, causing erroneous or stuck device output current due to a low V_{GS} voltage.	B
REGS	4	Regulator voltage will rail out high, disrupting the downstream circuitry, and possibly damaging the device if the device is not prepared to take a high-output voltage.	B
REGF	5	The device will be damaged because REGF is not intended to sink more than 50 µA of current.	A
VIN	6	If the supply voltage is greater than 18 V, and the pin is not current limited to 25 mA, the device will be damaged. If the supply voltage is less than 18 V, the internal amplifier will rail out, completely disrupting the internal feedback mechanism and resulting in erroneous output.	A
SET	7	If the supply voltage is greater than 14 V, and the pin is not current limited to 25 mA, the device will be damaged. If the supply voltage is less than 14 V, then the internal op amp will rail and shut off the internal FET, completely disrupting the internal feedback mechanism and resulting in erroneous output.	A
EF	8	The error flag will be stuck high, so if the device enters a state where an error is present (such as a wire break), the flag will not indicate this error.	B
OD	9	The output will be stuck at disabled, meaning that the output can no longer be enabled.	B
GND	10	Device supplies will be shorted together, leaving the GND pin at some voltage between the VSP and GND sources (depending on source impedance).	A
PAD	P	Device supplies will be shorted together, leaving the GND/PAD pin at some voltage between the VSP and GND sources (depending on source impedance).	A

4.2 VSON Package

Figure 4-2 shows the XTR111 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the XTR111 data sheet.

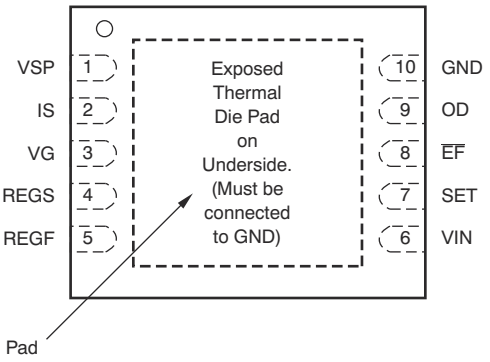

Figure 4-2. Pin Diagram (VSON Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VSP	1	The device supplies are shorted together, leaving the VSP pin at some voltage between the VSP and GND sources (depending on source impedance).	A
IS	2	If the supply voltage is greater than 6.5 V, and the pin is not current limited to 50 mA, the device will be damaged.	A
VG	3	If the supply voltage is greater than 18 V, and the pin is not current limited to 25 mA, the device will be damaged. Additionally, the external FET and BJT will have a low voltage at the respective gate or collector. This low voltage causes erroneous or stuck device output current due to high V_{GS} voltage, which could theoretically damage the external FET.	A
REGS	4	The regulator voltage will be near the rail voltage, disrupting downstream circuitry that is powered from REGF.	B
REGF	5	The internal amplifier will try to force current through the short, maxing out at 15 mA to 25 mA.	B
VIN	6	The internal amplifier will rail out, completely disrupting the internal feedback mechanism, and result in erroneous output of device (stuck at 0 mA).	B
SET	7	Internal op-amp pins will be held apart, resulting in the op amp railing gate being driven high, and thus attempt to force more current out of the SET pin. This configuration completely disrupts the internal feedback mechanism, and results in erroneous output of device.	B
EF	8	The error flag will be stuck at low, meaning if read, the error flag will always indicate an error (such as a wire break) even if the device is actually working fine.	B
OD	9	The output will be stuck at enabled, meaning the output can no longer be disabled.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VSP	1	Device positive supply will float, potentially resulting in damage if external voltages are present at the device inputs.	A
IS	2	The external FET and BJT will not have any voltage at the respective source or emitter, giving no proper current path, and thus disrupting device output current.	B
VG	3	Pin voltage will likely drift up to the VSP rail. The external FET and BJT will have high voltage at the respective gate or collector, causing erroneous or stuck device output current due to a low V_{GS} voltage. Capacitive coupling to this open pin could cause oscillations in the device output.	B
REGS	4	Capacitive coupling to this open pin could cause oscillations in the device regulator output, disrupting any downstream circuitry that is powered from REGF. The pin voltage will probably float to one rail or the other.	B
REGF	5	Downstream circuitry will not be powered, which could cause erroneous circuit behavior.	B
VIN	6	Capacitive coupling to this open pin could cause oscillations in the gate drive output, which could in turn cause oscillations in the device output.	B
SET	7	With no path to GND other than through the inverting input, the internal op amp will rail to shut off the internal FET, completely disrupting the internal feedback mechanism, and result in erroneous output of device.	B
EF	8	If the EF pin is *open* and not connected to an external pullup resistor and monitoring circuitry, to that external circuit, the error flag will appear to be stuck at high. Therefore, if the device enters a state where an error is present (such as a wire break), the monitor circuit will not detect this error.	B
OD	9	The output will be stuck at disabled because of the internal pullup resistor on the OD pin, preventing the device output from being enabled. Possibility of glitches if a 4-µA internal pullup resistor is overpowered by capacitive coupling.	B
GND	10	The device negative supply will float, potentially resulting in damage if external voltages are present at the inputs.	A
PAD	P	The device will not be able to thermally dissipate and could overheat with high currents. Long-term reliability and structural integrity could be compromised.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VSP	1	2	The external FET and BJT will have higher voltage at the respective source or emitter than intended, causing erroneous device output current due to an incorrect V_{GS} voltage.	B
IS	2	3	The external FET and BJT will have the same voltage at the respective source or emitter as at the gate or collector, causing erroneous or stuck device output current due to a zero V_{GS} voltage.	B
VG	3	4	The regulator voltage will be disrupted. If the resistor divider used to set REGF uses low-value resistors, VG can become loaded, resulting in an erroneous gate drive.	B
REGS	4	5	The internal regulator acts as a buffer of the internal 3-V reference, which will lead to an incorrect REGF output voltage.	B
EF	8	9	If an external pullup resistor is used on the EF pin, this pullup resistor will fight any external pulldown resistor present on the OD pin, possibly forming a voltage divider that will cause a voltage at OD in between a true high or low. This configuration could force the output to be erroneously disabled or glitch. This configuration will also cause an in-between voltage on the EF pin, disrupting EF pin functionality.	B
OD	9	10	Output will be stuck at enabled, meaning that the output can no longer be disabled.	B
PAD	P	ALL	Same as *Short to GND*; see Table 4-6.	

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IS	2	The external FET and BJT will have a higher voltage at the respective source or emitter than intended, causing erroneous device output current due to an incorrect V_{GS} voltage.	B
VG	3	The external FET and BJT will have a high voltage at the respective gate or collector, causing erroneous or stuck device output current due to a low V_{GS} voltage.	B
REGS	4	Regulator voltage will rail out high, disrupting the downstream circuitry, and possibly damaging the device if the device is not prepared to take a high-output voltage.	B
REGF	5	The device will be damaged because REGF is not intended to sink more than 50 µA of current.	A
VIN	6	If the supply voltage is greater than 18 V, and the pin is not current limited to 25 mA, the device will be damaged. If the supply voltage is less than 18 V, the internal amplifier will rail out, completely disrupting the internal feedback mechanism and resulting in erroneous output.	A
SET	7	If the supply voltage is greater than 14 V, and the pin is not current limited to 25 mA, the device will be damaged. If the supply voltage is less than 14 V, then the internal op amp will rail and shut off the internal FET, completely disrupting the internal feedback mechanism and resulting in erroneous output.	A
EF	8	The error flag will be stuck high, so if the device enters a state where an error is present (such as a wire break), the flag will not indicate this error.	B
OD	9	The output will be stuck at disabled, meaning that the output can no longer be enabled.	B
GND	10	Device supplies will be shorted together, leaving the GND pin at some voltage between the VSP and GND sources (depending on source impedance).	A
PAD	P	Device supplies will be shorted together, leaving the GND/PAD pin at some voltage between the VSP and GND sources (depending on source impedance).	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2022) to Revision A (December 2022)	Page
• Added VSON package and associated content to document	2

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