Application Note TIOL112(x) Functional Safety FIT Rate, FMD and Pin FMA

TEXAS INSTRUMENTS

Table of Contents

1 Overview	2
2 Functional Safety Failure In Time (FIT) Rates	3
3 Failure Mode Distribution (FMD)	
4 Pin Failure Mode Analysis (Pin FMA)	
5 Revision History	

List of Figures

Figure 1-1. Functional Block Diagram (TIOL112)	. 2
Figure 1-2. Functional Block Diagram (TIOL1123, TIOL1125)	
Figure 4-1. Pin Diagram (TIOL112)	
Figure 4-2. Pin Diagram (TIOL1123, TIOL1125)	

List of Tables

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 (TIOL1123, TIOL1125)	3
Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 (TIOL112)	. 3
Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2	3
Table 3-1. Die Failure Modes and Distribution	4
Table 4-1. TI Classification of Failure Effects	5
Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (L-)	. 6
Fable 4-3. Pin FMA for Device Pins Open-Circuited	6
Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin	7
Table 4-5. Pin FMA for Device Pins Short-Circuited to L+	7
Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC_OUT (TIOL1123, TIOL1125)	8
Table 4-7. Pin FMA for Device Pins Short-Circuited to VCC_IN (TIOL112)	<mark>8</mark>

Trademarks

All trademarks are the property of their respective owners.

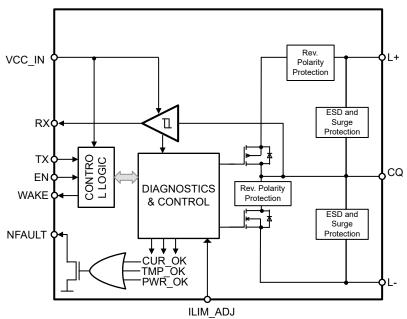
1

1 Overview

This document contains information for TIOL112(x) family of devices (TIOL112, TIOL1123 and TIOL1125) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 and Figure 1-2 show the device functional block diagram for reference.





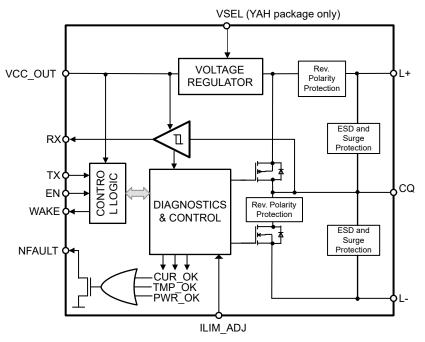


Figure 1-2. Functional Block Diagram (TIOL1123, TIOL1125)

The devices were developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.



2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TIOL112(x) family based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates for TIOL1123/TIOL1125 (with LDO) based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates for TIOL112 (without LDO) based on IEC TR 62380 / ISO 26262 part 11
- Table 2-3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 (TIOL1123, TIOL1125)

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours) DRC-10 (VSON Package)
Total Component FIT Rate	9
Die FIT Rate	5
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 550 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11 (TIOL112)

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours) DRC-10 (VSON Package)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 200 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-3. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	BICMOS, ASIC, Analog & Mixed ≤ 50 V Supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.



3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TIOL112, TIOL1123 and TIOL1125 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Die Failure Modes	ie Failure Modes Failure Mode Distribution (%) (TIOL1123, TIOL125)	
Transmitter failure	72%	72%
Receiver failure	3%	3%
VCC_OUT LDO failure	5%	Not applicable
VCC_IN internal logic failure	Not applicable	5%
NFAULT logic failure	10%	10%
Wake logic failure	5%	5%
Control logic failure	5%	5%

Table 3-1. Die Failure Modes and Distribution

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TIOL112, TIOL1123, and TIOL1125. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (L-) (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to L+ (see Table 4-5 and)
- Pin short-circuited to VCC_OUT (for TIOL1123, TIOL1125, see Table 4-6)
- Pin short-circuited to VCC_IN (for TIOL112, see Table 4-7)

Table 4-2 through Table 4-7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
В	No device damage, but loss of functionality
С	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 and Figure 4-2show the pin diagram for TIOL112(x) family. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TIOL112(x) datasheet.

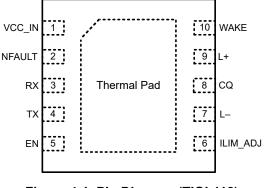
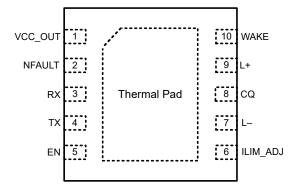
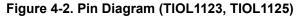


Figure 4-1. Pin Diagram (TIOL112)





Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

· All conditions meet recommended operating conditions

5

Pin Name	Pin No.	Description of Potential Failure Effect(s)	
VCC_OUT (TIOL1123, TIOL1125)	1	Device I/O logic blocks unpowered. Although LDO current is internally limited to 35 mA ±20%, thermal shutdown may be activated depending upon ambient temperature and the power dissipation in the LDO.	В
VCC_IN (TIOL112)		Device not functional. Logic I/O blocks powered by VCC_IN will be unpowered. No communication with MCU.	В
NFAULT	2	Incorrect fault indicator output. Microcontroller will assume device is in the fault state for the duration of the short event.	В
RX	3	Receiver output stuck at low fault.	В
ТХ	4	CQ output will be stuck at high (high-side switch ON) for the duration of the short event if EN is high. Device transmitter is not functional.	В
EN	5	Device Driver is always tri-stated. Device transmitter is not functional.	В
ILIM_ADJ	6	Device operates with a different current limit setting than intended. Overcurrent fault will be indicated without blanking time and the driver will not be disabled due to overcurrent fault.	В
L-	7	None	D
CQ	8	CQ output stuck at low and no commnunication is possible. When EN=H and TX=LOW, device will go into current fault due to overcurrent condition cycling into driver turn-off and auto-recovery cycles. Thermal shutdown may be triggered.	В
L+	9	Device is unpowered and not functional.	В
WAKE	10	IO-link wake-up functionality will not work as intended. Microprocessor may recognize the short event as a wake-up event and turn-off the driver.	В
Thermal Pad	-	None	D

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (L-)

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	
VCC_OUT (TIOL1123, TIOL1125)	1	Sensor/Microcontroller will not be functional if VCC_OUT is powering the sensor/microcontroller.	В
VCC_IN (TIOL112)		Device will not be functional. Logic I/O blocks powered by VCC_IN will be unpowered. No communication with MCU.	В
NFAULT	2	No NFAULT information provided to the microcontroller	В
RX	3	Data will not be received by the microcontroller	В
ТХ	4	No data can be transmitted from the Sensor FE/Micro to the output	В
EN	5	Device is always tri-stated. Device can only receive data.	В
ILIM_ADJ	6	Device operates with a different current limit setting than intended. Overcurrent fault will be indicated without blanking time and the driver will not be disabled due to overcurrent fault.	В
L-	7	Device is unpowered	В
CQ	8	No communication over the bus.	В
L+	9	Device is unpowered	В
WAKE	10	Wake signal will not be indicated to the microcontroller	В
Thermal Pad	-	If thermal pad is not connected to GND planes in the PCB, thermal performance will not be optimal	С

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCC_OUT (TIOL1123, TIOL1125)	1	NFAULT	High ICC current during internal NFAULT active conditions. No external NFAULT active indication	В
VCC_IN (TIOL112)			High ICC_IN current during internal NFAULT active conditions. No external NFAULT active indication	В
NFAULT	2	RX	Contention between driver output at the RX pin and the MCU output driving the TX input. Device functionality is lost.	В
RX	3	ТХ	Contention between driver output at RX pin and driver output at the NFAULT pin. Receiver & fault detection functionality is lost.	В
тх	4	EN	If IN and EN are driven to different states communication and device state can be compromised	В
EN	5	NA	None	D
ILIM_ADJ	6	L-	Device operates at the maximum current limit. Overcurrent fault will not be indicated and the driver will not be disabled due to overcurrent fault.	В
L-	7	CQ	CQ output stuck at low and no commnunication is possible. When EN=H and TX=LOW, device will go into current fault due to overcurrent condition cycling into driver turn-off and auto-recovery cycles. Thermal shutdown may be triggered.	В
CQ	8	L+	No communication over the bus. Internal reverse polarity protection helps protect the device as long as absolute maximum operating conditions are not exceeded.	В
L+	9	WAKE	Absolute maximum operating condition exceeded for the WAKE pin	А
WAKE	10	NA	None	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Note

The VSON package includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad (recommended connection is L-).

Pin Name	Pin No.	Description of Potential Failure Effect(s)	
VCC_OUT/ VCC_IN	1	ABS Max violation on VCC_OUT/VCC_IN pin. Sensor FE/MCU damaged by VCC_OUT/VCC_IN over-voltage.	
NFAULT	2	Absolute maximum operating condition exceeded	
RX	3	Absolute maximum operating condition exceeded	
ТХ	4	Absolute maximum operating condition exceeded	
EN	5	Absolute maximum operating condition exceeded	
ILIM_ADJ	6	Absolute maximum operating condition exceeded	
L-	7	Device not functional. Ensure that the absolute maximum ratings are not exceeded otherwise device damage may be plausible.	
CQ	8	Device not functional. Ensure that the absolute maximum ratings are not exceeded otherwise device damage may be plausible.	
L+	9	NA	
WAKE	10	Absolute maximum operating condition exceeded	



Table 4-6. Pin FMA for Device Pins Short-Circuited to VCC_OUT (TIOL1123, TIOL1125)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	
VCC_OUT	1	NA	
NFAULT	2	High current draw from the internal LDO current when the NFAULT is pulled low internal to the device. No fault indication to the microcontroller.	
RX	3	Receiver output will be in stuck at high fault.	
ТХ	4	Device transmitter will always output low on the bus. Device transmitter functionality is lost.	
EN	5	Transmitter is always enabled. Receiver will loop back the data on TX pin	
ILIM_ADJ	6	May cause degradation in the current limiting functionality.	
L-	7	Device I/O logic blocks unpowered . Thermal shutdown may be activated due to excessive current draw from the internal LDO.	
CQ	8	Device not functional. Ensure that the absolute maximum ratings are not exceeded otherwise device damage may be plausible on the VCC_OUT pin	
L+	9	Absolute maximum operating condition exceeded on VCC_OUT pin	
WAKE	10	IO-link wake-up functionality is lost	

Table 4-7. Pin FMA for Device Pins Short-Circuited to VCC_IN (TIOL112)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	
VCC_IN	1	NA	
NFAULT	2	High current draw from the external LDO that's supplying VCC_IN when the NFAULT is pulled low internal to the device. No fault indication to the microcontroller.	
RX	3	Receiver output will be in stuck at high fault. If the receiver output is internally pulled low, there could be high current draw from VCC_IN.	
ТХ	4	Device transmitter will always output low on the bus. Device transmitter functionality is lost.	
EN	5	Transmitter is always enabled. Receiver will loop back the data on TX pin	
ILIM_ADJ	6	May cause degradation in the current limiting functionality.	
L-	7	Device I/O logic blocks unpowered. High current draw from the external LDO supplying VCC_IN.	В
CQ	8	Communication is not possible over the bus.	В
L+	9	Absolute maximum operating condition exceeded on VCC_IN pin	A
WAKE	10	IO-link wake-up functionality is lost	

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2022, Texas Instruments Incorporated