Operational Amplifier (OA)

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The most recent version of the full user's guide is available from http://www.ti.com/lit/pdf/slau208.

The operational amplifier (OA) module is a general-purpose operational amplifier. This chapter describes the OA.

Topic **Page**

1.1 OA Introduction

The OA operational amplifiers can be used to support front-end analog signal conditioning before analog-to-digital conversion as well as other general-purpose applications.

Features of the OA include:

- Single-supply low-current operation
- Software selectable rail-to-rail input
- Rail-to-rail output
- Input switches on positive and negative inputs individually software selectable
- Internal voltage follower setting
- Low-impedance ground switches individually software selectable (not available on all devices)

NOTE: Multiple OA Modules

Some devices may integrate more than one OA module. If more than one OA is present on a device, the multiple OA modules operate identically.

Throughout this chapter, nomenclature appears such as OAnCTL0 to describe register names. When this occurs, the *n* indicates which OA module is being discussed. In cases where operation is identical, the register is simply referred to as OAnCTL0.

NOTE: Switches and Configurations

The connections of the amplifier to device pins or internal connections are device specific. Refer to the device-specific data sheet for specific interconnections and device pin connections. The information in this chapter applies to all operational amplifiers in the family.

Figure 1-1 shows the block diagram of the OA module.

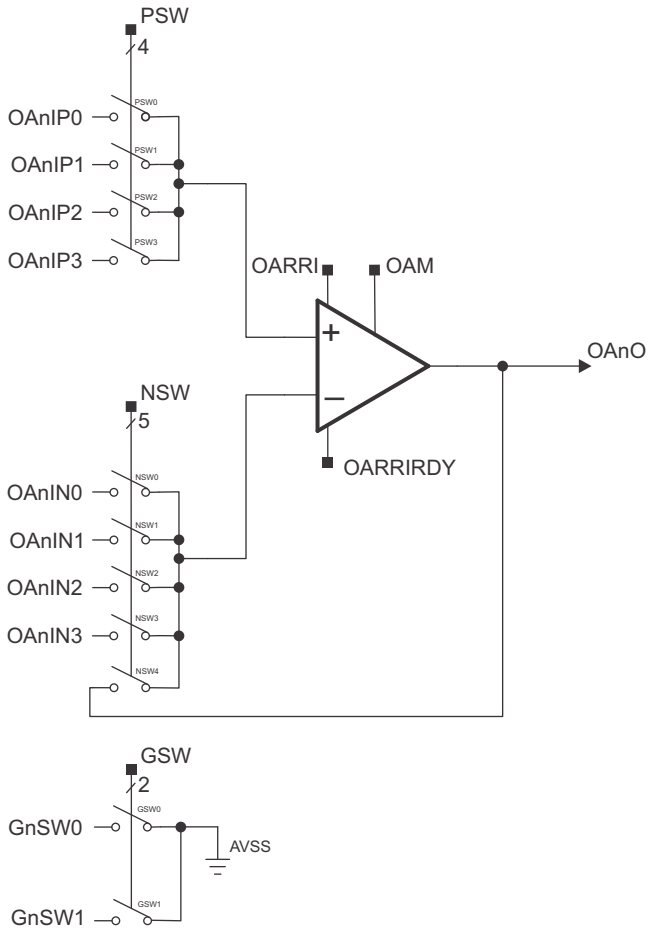

Figure 1-1. OA Block Diagram

1.2 OA Operation

The OA module is configured with user software. The setup and operation of the OA is discussed in the following sections.

1.2.1 OA Modes

The OA can be enabled and disabled using OAM as listed in Table 1-1. To speed up the enable time of the OA, The REF module REFON bit in the REFCTL register can be set before enabling OA to allow the AFE bias, required by the OA, to turn on.

Table 1-1. OA Mode Select

OAM	OA Function
0	Disabled. Output high impedance. All input switches opened, regardless of PSW or NSW settings.
1	Enabled. If OA output is shared with a digital I/O port, the digital I/O port is automatically disabled regardless of the PxSEL settings of the respective port.

1.2.2 Rail-to-Rail Input Modes

Each operational amplifier supports rail-to-rail input swings. Setting OARRI = 1 enables the rail-to-rail input mode but requires additional current. Thus, to save current, rail-to-rail input mode (OARRI) should be selected only if the dynamic range required for the application requires it. Refer to the common-mode voltage range V_{CM} specified in the device-specific data sheet for OARRI = 0 and 1. Rail-to-rail operation is made possible by an integrated charge pump that increases the internal supply of the respective amplifier's input stage to allow linear operation over the complete common mode range. The charge pump is shared with all operational amplifier instantiations. Setting any OARRI = 1 of any respective OA will enable the charge pump independently of the OAM setting. The charge pump can also be enabled from the CTSD16 module if in rail-to-rail input mode, CTSD16RRI = 1. When OARRI = 1 is set, the charge pump, if not already enabled, is enabled. OARRIRDY = 1 indicates the charge pump is ready and stable, and the rail-to-rail input mode is ready for usage. Setting OARRI = 0 causes OARRIDY = 0 for the corresponding OA. The charge pump does incur additional power to operate. The charge pump requires a single external capacitor from the CPCAP terminal to ground for proper operation. See the device-specific data sheet for proper value and tolerances. Setting OARRI = 0 provides for a reduced input swing range on the respective amplifier. Setting OARRI = 0 of all OA instances and setting CTSD16RRI=0 is required to disable the charge pump. See the device-specific data sheet for input ranges supported for all OARRI settings.

NOTE: On devices that contain the CTSD16, the charge pump is also used for PGA buffers when rail-to-rail input mode is selected, CTSD16RRI = 1. Therefore, the charge pump may remain enabled although OARRI = 0 for all OA instances.

NOTE: On devices that contain the CTSD16, the charge pump uses a clock that is provided by the CTSD16CLK. If any OA is enabled and set to rail-to-rail input mode, the CTSD16CLK will automatically be enabled regardless if the CTSD16 is enabled or not. In addition, the CTSD16CLK has fault detection logic that may cause an NMI to occur. Any existing fault should be corrected for proper OA operation.

1.2.3 OA Inputs

The OA has a configurable input selection. The signals for the + and – inputs are individually selected with the OAxPSW and OAxNSW bits, respectively. Each switch is independently selectable. The connection of inputs can either be internal or external connections and are device specific. Refer to the device-specific data sheet for all operational amplifier connections. When OAM = 0, the OA is disabled and all input switches are opened regardless of the OAxPSW and OAxNSW settings.

Negative input terminal switch 4 control, NSW4, allows for an internally connected voltage follower configuration. Refer to device-specific data sheet for other internal connection options.

1.3 Ground Switches

Ground switches are an optional feature of the operational amplifier module. Refer to device-specific data sheet for availability and connections. Each ground switch can be enabled individually by software using the GSW bits. Setting GSW = 1 closes the switch and provides a low-ohmic connection to the analog ground to the GxSWx external pin and internal connections (see device-specific data sheet for internal connections available). If a ground switch output is shared with a digital I/O port, the digital I/O port is automatically disabled when GSW = 1, regardless of the PxSEL settings of the respective port.

1.4 OA and Power Modes

The OA can be used in all power modes except LPMx.5 modes. Note that although the respective LPM mode can be entered, there is additional power dissipation due to the OA being active. Therefore, entering some of the lower-power modes, such as LPM2 through LPM4, while the module is enabled has reduced low-power benefits.

1.5 OA Registers

Table 1-2 lists the OA module registers. The base address can be found in the device-specific data sheet. The address offset is listed in Table 1-2.

NOTE: All registers have word or byte register access. For a generic register*ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 1-2. OA Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	OAnCTL0	OAn Control 0	Read/write	Word	0000h	Section 1.5.1
00h	OAnCTL0_L		Read/write	Byte	00h	
01h	OAnCTL0_H		Read/write	Byte	00h	
02h	OAnPSW	OAn Positive Input Terminal Switches	Read/write	Word	0000h	Section 1.5.2
02h	OAnPSW_L		Read/write	Byte	00h	
03h	OAnPSW_H		Read/write	Byte	00h	
04h	OAnNSW	OAn Negative Input Terminal Switches	Read/write	Word	0000h	Section 1.5.3
04h	OAnNSW_L		Read/write	Byte	00h	
05h	OAnNSW_H		Read/write	Byte	00h	
0Eh	OAnGSW	OAn Ground Switches	Read/write	Word	0000h	Section 1.5.4
0Eh	OAnGSW_L		Read/write	Byte	00h	
0Fh	OAnGSW_H		Read/write	Byte	00h	

1.5.1 OAnCTL0 Register

Operational Amplifier n Control 0

Figure 1-2. OAnCTL0 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved	OARRIRDY	OARRI	Reserved	Reserved			OAM
r0	r-0	rw-0	r0	r0	r0	r0	rw-0

Table 1-3. OAnCTL0 Register Description

Bit	Field	Type	Reset	Description
15-7	Reserved	R	0h	Reserved. Always reads as 0.
6	OARRIRDY	R	0h	Rail-to-rail input ready status. 0b = Rail-to-rail input not ready 1b = Rail-to-rail input ready
5	OARRI	RW	0h	Rail-to-rail input enable. 0b = Rail-to-rail input disabled 1b = Rail-to-rail input enabled
4	Reserved	R	0h	Reserved. Always read as 0.
3-1	Reserved	R	0h	Reserved. Always read as 0. These bits are reserved for future amplifier mode (OAM) settings.
0	OAM	RW	0h	Amplifier mode selection. 0b = Disabled. Output high impedance. All input switches opened, regardless of PSW and NSW settings. 1b = Enabled. If OA output is shared with a digital I/O port, the digital I/O port is automatically disabled regardless of the PxSEL settings of the respective port.

1.5.2 OAnPSW Register

Operational Amplifier n Positive Terminal Switches

Figure 1-3. OAnPSW Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved				PSW3	PSW2	PSW1	PSW0
r0	r0	r0	r0	rw-0	rw-0	rw-0	rw-0

Table 1-4. OAnPSW Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved. Always reads as 0.
3	PSW3	RW	0h	Positive input terminal switch 3 control. 0b = Switch open 1b = Switch closed
2	PSW2	RW	0h	Positive input terminal switch 2 control. 0b = Switch open 1b = Switch closed
1	PSW1	RW	0h	Positive input terminal switch 1 control. 0b = Switch open 1b = Switch closed
0	PSW0	RW	0h	Positive input terminal switch 0 control. 0b = Switch open 1b = Switch closed

1.5.3 OAnNSW Register

Operational Amplifier n Negative Terminal Switches

Figure 1-4. OAnNSW Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved			NSW4	NSW3	NSW2	NSW1	NSW0
r0	r0	r0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-5. OAnNSW Register Description

Bit	Field	Type	Reset	Description
15-5	Reserved	R	0h	Reserved. Always reads as 0.
4	NSW4	RW	0h	Negative input terminal switch 4 control. Voltage follower configuration. 0b = Switch open 1b = Switch closed. Amplifier output internally connected to negative input terminal.
3	NSW3	RW	0h	Negative input terminal switch 3 control. 0b = Switch open 1b = Switch closed
2	NSW2	RW	0h	Negative input terminal switch 2 control. 0b = Switch open 1b = Switch closed
1	NSW1	RW	0h	Negative input terminal switch 1 control. 0b = Switch open 1b = Switch closed
0	NSW0	RW	0h	Negative input terminal switch 0 control. 0b = Switch open 1b = Switch closed

1.5.4 OAnGSW Register

Operational Amplifier n Ground Switches

Figure 1-5. OAnGSW Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved						GSW1	GSW0
r0	r0	r0	r0	r0	r0	rw-0	rw-0

Table 1-6. OAnGSW Register Description

Bit	Field	Type	Reset	Description
15-2	Reserved	R	0h	Reserved. Always reads as 0.
1	GSW1	RW	0h	Ground switch. 0b = Switch open 1b = Switch closed and external GxSW1 pin and internal connections (see device-specific data sheet for internal connections available) are connected to analog ground. If ground switch output is shared with a digital I/O port, the digital I/O port is automatically disabled regardless of the PxSEL settings of the respective port.
0	GSW0	RW	0h	Ground switch. 0b = Switch open 1b = Switch closed and external GxSW0 pin and internal connections (see device-specific data sheet for internal connections available) are connected to analog ground. If ground switch output is shared with a digital I/O port, the digital I/O port is automatically disabled regardless of the PxSEL settings of the respective port.

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