

This user's guide describes the function and use of the ADS54J69 evaluation module. Included in this document are a quick-start guide, instructions for optimizing evaluation results, software description, alternate hardware configurations, and jumper, connector, and LED descriptions.

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Overview

1 Overview

The ADS54J69EVM is an evaluation module (EVM) designed to evaluate the ADS54J69 high-speed, JESD204B interface ADCs. The EVM includes an onboard clocking solution (LMK04828), transformer-coupled inputs, full power solution, and easy-to-use software GUI and USB interface.

The following features apply to this EVM:

- Transformer-coupled signal input network allowing a single-ended signal source from 0.4 MHz to 800 MHz
- LMK04828 system clock generator that generates field-programmable gate array (FPGA) reference clocks for the high-speed serial interface and may be used to generate the ADC sampling clock (default setting)
- Transformer-coupled clock input network to test the ADC performance with a very low-noise clock source
- High-speed serial data output over a standard FPGA Mezzanine Card (FMC) interface connector

The ADS54J69EVM is designed to work seamlessly with the TSW14J56EVM, Texas Instruments' JESD204B data capture/pattern generator card, through the High Speed Data Converter Pro (HSDC Pro) software tool for high-speed data converter evaluation. The ADS54J69EVM was also designed to work with many of the development kits from leading FPGA vendors that contain an FMC connector.

1.1 Required Hardware

The following equipment is **included** in the EVM evaluation kit:

- ADS54J69 Evaluation Board (EVM)
- · Power supply cable
- Mini-USB cable

The following list of equipment are items that are **not included** in the EVM evaluation kit but are items required for evaluation of this product in order to achieve the best performance:

- TSW14J56EVM Data Capture Board, two +5-V power supplies, and Mini-USB cable
- Computer running Microsoft® Windows® 8, Windows 7, or Windows XP
- One Low-Noise Signal Generator. Recommendations:
 - RF generator, > +17 dBm, < -40 dBc harmonics, < 500 fs jitter 20 kHz-20 MHz, 10-MHz to 2-GHz frequency range
 - Examples: TSW2170EVM, HP HP8644B, Rohde & Schwarz SMA100A
- Bandpass filter for desired analog input. Recommendations:
 - Bandpass filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
 - Examples: Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
- Signal path cables, SMA and/or BNC with BNC-to-SMA adapters

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1.2 Required Software

The following software is required to operate the ADS54J69EVM and available online. See References, Section 1.4 for links.

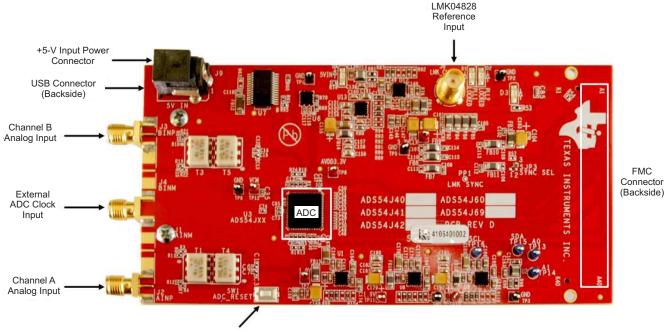
ADS54Jxx EVM GUI

The following software is required to operate the TSW14J56EVM and available online. See References, Section 1.4 for links.

- High Speed Data Converter Pro software, version 4.1 or higher
- HSDC Pro GUI Updates (Rev. I) for High Speed Data Converter Pro Software, version 4.0 or lower

1.3 Evaluation Board Feature Identification Summary

The EVM features are labeled in Figure 1.



ADC Reset Switch

Figure 1. EVM Feature Locations

1.4 References

- ADS54Jxx EVM software, available at: www.ti.com/tool/ADS54J69EVM
- ADS54J69 datasheet (SBAS713), available at www.ti.com/product/ADS54J69
- LMK04828 datasheet (SNAS605), available at www.ti.com/product/lmk04828
- TSW14J56EVM User's Guide (SLWU086), available at www.ti.com/tool/TSW14J56EVM
- High Speed Data Converter Pro software (SLWC107) and User's Guide (SLWU087), available at www.ti.com/tool/dataconverterpro-sw
- HSDC Pro GUI Updates (SLWC106), available at www.ti.com/tool/dataconverterpro-sw

NOTE: Schematics, layout, and BOM are available on the ADS54J69EVM product page on www.ti.com.

Overview



2 Quick Start Guide

This section guides the user through the EVM test procedure to obtain a valid data capture from the ADS54J69EVM using the TSW14J56EVM capture card. This should be the starting point for all evaluations.

2.1 Software Installation

The proper software must be installed before beginning evaluation. See Section 1.2 for a list of the required software. The References section of this document contains links to find the software on the TI website.

Important: The software must be installed before connecting the ADS54J69EVM and TSW14J56 to the computer for the first time.

2.1.1 ADS54Jxx EVM GUI Installation

The ADS54Jxx EVM GUI is used to control the ADS54J69EVM. It must be used to properly configure the devices on the EVM.

- 1. Download the ADS54Jxx EVM GUI from the TI website. The References section of this document contains links to find the software on the TI website.
- 2. Extract the files from the zip file.
- 3. Run setup.exe and follow the installation prompts.

2.1.2 High Speed Data Converter Pro GUI Installation

High Speed Data Converter Pro (HSDC Pro) is used to control the TSW14J56EVM and analyze the captured data. Please see the HSDC Pro user's guide (SLWU087) for more information.

- 1. Download HSDC Pro from the TI website. The References section of this document contains the link to find the software on the TI website.
- 2. Extract the files from the zip file.
- 3. Run setup.exe and follow the installation prompts.
- If the version of HSDC Pro is 4.0 or lower, download HSDC Pro GUI Updates from the TI website. The References, Section 1.4 section of this document contains the link to find the software on the TI website.
- 5. Extract the files from the zip file, run HSDC Pro Patch vx.xx.exe and follow the installation instructions.

2.2 Hardware Setup Procedure

A typical test setup using the ADS54J69EVM and TSW14J56EVM is shown in Figure 2. This is the test setup used for the quick start procedure. The rest of this section describes the hardware setup steps.

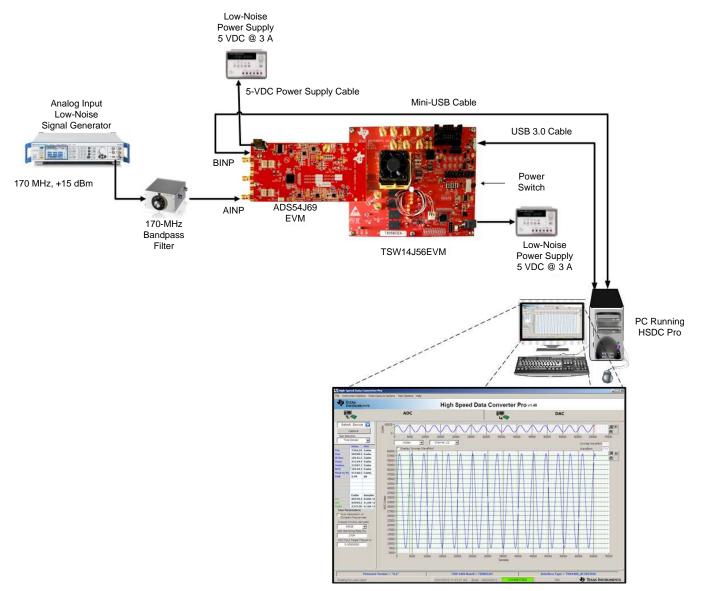


Figure 2. Quick Start Test Setup

2.2.1 TSW14J56EVM Setup

First, setup the TSW14J56EVM using the following steps:

- 1. Connect the ADS54J69EVM to the TSW14J56EVM using the FMC connectors.
- 2. Connect one end of the provided 5-V power supply cable to connector J11 (+5 V IN) and the other end to a +5 VDC source with a minimum current rating of 3 A. Turn on the power supply.
- 3. Connect the included USB cable between the host computer and USB connector (J9).
- 4. Flip the power switch (SW6) to the ON position.



Quick Start Guide

2.2.2 ADS54J69EVM Setup

Next, setup the ADS54J69EVM using the following:

- Connect the included 5-V power supply cable to connector J9 of the EVM. Connect the red wire to +5 VDC ±0.1 VDC of a power supply rated for at least 3 A. Connect the black wire to GND of the power supply.
- 2. Turn on the 5-VDC power supply. The power draw should be around 0.66 A. When the board is configured, it will draw approximately 1.12 A.
- 3. Connect one end of the included mini-USB cable to a host computer and the other end to the USB connector J8, located on the backside of the board.
- 4. Set an analog input signal generator for 170 MHz, and about +15 dBm of power.
- 5. Place a narrow pass-band bandpass filter at the output of the signal generator to remove noise and harmonics.
- 6. Connect the output of the filter to SMA connector AINP (J2) of the EVM.

2.3 Software Setup Procedure

The software can be opened and configured once the hardware is properly setup.

2.3.1 ADS54J69 GUI Configuration for Decimate-by-2 Low Pass Filter Mode

- 1. Open the ADS54Jxx EVM GUI by going to *Start Menu* → *All Programs* → *Texas Instruments ADCs* → *ADS54Jxx EVM GUI*.
- 2. Verify that the green USB Status indicator is lit in the top right corner of the GUI. If it is not lit, click the *Reconnect USB* button and check the USB Status indicator again. If it is still not lit, then verify the EVM is connected to the computer through the included mini-USB cable.
- 3. Click on the Low Level View tab then click the Load Config button.
- 4. Navigate to C:\Program Files(86)\Texas Instruments\ADS54Jxx EVM GUI\Configuration Files, select the file called LMK_Config_Onboard_983p04_MSPS.cfg, then click OK. This programs the LMK04828 to provide a 983.04 MHz clock to the ADC.
- 5. Verify that the LMK04828 phase lock loop (PLL) is locked by checking that the *PLL2 LOCKED* LED (D2) is lit.
- 6. Once the LMK04828 PLL is locked, press SW1 (*ADC RESET*) to provide a hardware reset to the ADC. This switch is located on the bottom left of the EVM.
- In the Low Level View tab, click Load Config. Select the file called ADS54J69_2x_dec_lowpass_4222.cfg and click OK. The ADS54J69EVM is now configured for decimation by 2 and using 4 JESD204B lanes.



			AC)S5	4Jxx	USB Status
DS54Jxx LMK04828	Low Level View	w				USB Status 🔵 Reconnect FI
egister Map						Write Data Desister Deta
Block / Register Name	Address	Default	Mode	Size	Value 🔺	x 0
LMK04828						RW
×000	0×00	0x00	R/W	8	0x00 =	Write Register
×002	0x02	0x00	R/W	8	0x00	
×003	0x03	0x00	R	8	0x00	Write All
×004	0×04	0x00	R	8	0x00	Bead Data
×005	0×05	0x00	R	8	0x00	
×006	0×06	0x00	R	8	0x00	x 0
×00C	0×0C	0x00	R	8	0x00	Read Register
×00E	0×0E	0x00	R	8	0x00	Read Register
×100	0×100	0x02			0x02	Read All
×101	0x101	0x55	R/W	8	0x55	Read All
x103 x104	0x103 0x104	0x00 0x00	R/W R/W	8	0x00 0x00	Current Address
×104 ×105	0x104	0x00	R/W	8	0x00	x 0
x105	0x105 0x106	0x00	R/W	8	0x00 0x79	
x106 x107	0x108 0x107	0x/9	RAW	8	0x79 0x00	Note: Load
x107 x108	0x107 0x108	0x00 0x04	R/W	8	0x00 0x04	Config will Coverwrite all Load Config
x100	0x108	0x55	R/W	8	0x55	Overwrite all
x109	0x109	0x55 0x00	R/W	8	0x55 0x00	Registers.
x10D	0x10B	0x00	R/W	8	0x00	
x10C	0x10C	0x00	R/W	8	0x00	Load Config
×10E	0×10E	0x79	R/W	8	0x79 _	
105	0.100			1.		Save Config
egister Description						
						Divit Address Mich Data Davidante Are
						Block Address Write Data Read Data_Gen
						▼ × 0 × 0 × 0

Figure 3. ADS54Jxx GUI Low Level View Tab

2.3.2 HSDC Pro GUI Configuration

1. Open High Speed Data Converter Pro by going to *Start Menu* → *All Programs* → *Texas Instruments* → *High Speed Data Converter Pro*. The GUI main page looks as shown in Figure 4.

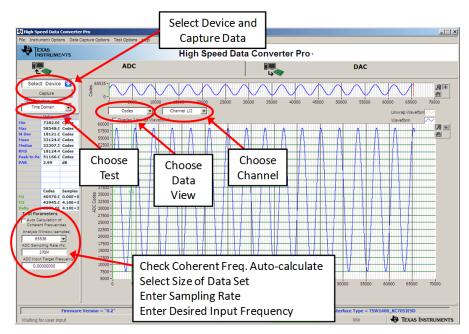


Figure 4. HSDC Pro GUI Main Panel

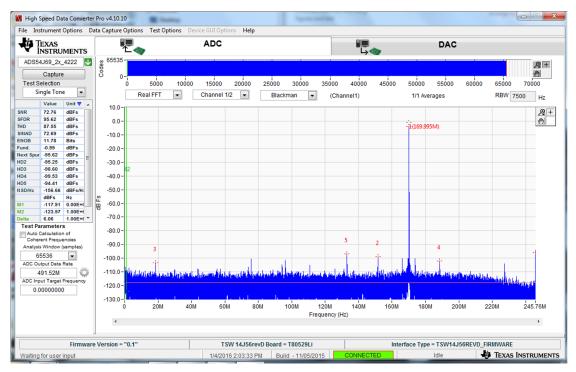
- 2. When prompted to select the capture board, select the TSW14J56 whose serial number corresponds to the serial number on the TSW14J56EVM and click *OK*. This popup can be accessed through the *Instrument Options* menu.
- 3. If no firmware is currently loaded, there is a message indicating this. Click on OK.

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Quick Start Guide

- 4. Verify the ADC tab at the top of the GUI is selected.
- 5. Use the Select ADC drop-down menu at the top left corner to select ADS54J69_2x_4222.
- 6. When prompted to update the firmware for the ADC, click Yes and wait for the firmware to download to the TSW14J56. This takes about 3 seconds.
- 7. Enter "491.52M" into the ADC Output Data Rate field at the bottom left corner then click outside this box or press return on the PC keyboard.
- 8. The GUI displays the new lane rate of the SerDes interface based off of the sample rate and other parameters from the loaded configuration files. Click *OK*.
- 9. Click the Instrument Options menu at the top of HSDC Pro and select Reset Board.
- 10. Click Capture in HSDC Pro to capture data from the ADC.
- 11. The results from the captured data of Channel 1 should look like Figure 5 and the performance should be similar to Table 1. If this result is not achieved, then see the Quick Start Troubleshooting section of this document.





Result	Measured Value	Units
SNR	72.76	dBFs
SFDR	95.62	dBFs

 Table 1. Quick Start Performance Measurements



2.4 Quick Start Trouble Shooting

Use Table 2 to assist with problems that may have occurred during the quick start procedure.

Issue	Troubleshooting Tips			
General Problems	Verify the test setup shown in Figure 2 and repeat the setup procedure as described in this document.			
	Check power supplies to the EVMs. Verify that the power switches are in the ON position.			
	Check signal and clock connections to the EVM.			
	Check that all boards are properly connected together.			
	Try pressing the CPU_RESET button on the TSW14J56EVM.			
	Try power-cycling the external power supply to the EVM and reprogram the LMK and ADC devices.			
TSW14J56 LEDs are not correct:	Verify the settings of the configuration switches on the TSW14J56EVM.			
D1, D5 – N/A D2, D4 – <i>Blinking</i> D3, D6, D7 – <i>OFF</i>	Verify that the EVM configuration GUI is communicating with the USB and that the configuration procedure has been followed.			
D8, D28 – ON	(LEDs Not Blinking) Reprogram the LMK device.			
	Try pressing the CPU_RESET button on the TSW14J56EVM.			
	Try capturing data in HSDC Pro to force an LED status update.			
Device GUI is not working properly	Verify that the USB cable is plugged into the EVM and the PC.			
	Check the computer's Device Manager and verify that a <i>USB Serial Device</i> is recognized when the EVM is connected to the PC.			
	Verify that the green USB Status LED light in the top right corner of the GUI is lit. If it is not lit, press Reconnect FTDI button.			
	Try restarting the configuration GUI.			
	Check default jumper connections as shown in Appendix A.			
HSDC Pro Software is not capturing good data or analysis	Verify that the TSW14J56EVM is properly connected to the PC with an USB cable and the board serial number is properly identified by the HSDC Pro software.			
results are incorrect.	Check that the proper ADC device is selected. In default conditions, ADS54J69_2x_4222 should be selected.			
	Check that the analysis parameters are properly configured.			
	Check that the fundamental power is no larger than -1 dBFs.			
HSDC Pro Software gives a Time-	Try to reprogram the LMK device and reset the JESD204 link.			
Out error when capturing data	Verify that the ADC sampling rate is correct in the HSDC Pro software.			
Sub-Optimal Measured Performance	Make sure an ADC hardware reset was issued after loading the LMK but before loading the ADC configuration file.			
	Check that the spectral analysis parameters are properly configured.			
	Verify that bandpass filters are used in the clock (external ADC Clock Mode) and input signal paths and that low-noise signal sources are used.			

Table 2. Troubleshooting Tips

Quick Start Guide

3 Optimizing Evaluation Results

This section assists the user in optimizing the performance during evaluation of the product.

3.1 Clocking Optimization

The sampling clock provided to the ADC needs to have very low phase noise to achieve optimal results. The default EVM configuration uses the LMK04828 clocking device to generate the sampling clock. There are two options to improve the clock noise performance.

- 1. To achieve the best performance, the LMK04828 can be bypassed in favor of an externally provided clock that is transformer-coupled to the ADC. The clock must have very low noise and must use an external narrow pass-band filter to achieve optimal noise performance. The clock amplitude must be within the datasheet limits. See Section 5 for more information regarding this setup.
- The LMK04828 can be used as a clock distributor by using an external clock as the input to the LMK04828. Filters should still be used on the clock to optimize the noise performance. See Section 5.2 for more information regarding this setup.

3.2 Coherent Input Source

A *Rectangular* window function can be applied to the captured data when the sample rate and the input frequency are set precisely to capture an integer number of cycles of the input frequency (sometimes called coherent frequency). This may yield better SNR results. The clock and analog inputs must be frequency-locked (such as through 10-MHz references) in order to achieve coherency.

3.3 HSDC Pro Settings

HSDC Pro has some settings that can help improve the performance measurements. These are highlighted in Table 3.

HSDC Pro Feature	Description
Analysis Window (samples)	Selects the number of samples to include in the selected test analysis. Collect more data to improve frequency resolution of Fast-Fourier Transform (FFT) analysis. If more than 65,536 samples are required, the setting in the <i>Data Capture Options</i> needs to be increased to match this value.
Data Windowing Function	Select the desired windowing function applied to the data for FFT analysis. Select <i>Blackman</i> when sampling a non-coherent input signal and <i>Rectangle</i> when sampling a coherent input signal.
Test Options \rightarrow Notch Frequency Bins	Select bins to be removed from the spectrum and back-filled with the average noise level. May also customize which Harmonics/Spurs are considered in SNR and THD calculations and select the method for calculating spur power.
Test Options \rightarrow Bandwidth Integration Markers	Enable markers to narrow the Single-Tone FFT test analysis to a specific bandwidth.
Data Capture Options \rightarrow Capture Options	Configure the number of contiguous samples per capture (capture depth). May also enable Continuous Capture and FFT Averaging.

Table 3. HSDC Pro Settings to Optimize Results



4 Software Description

4.1 ADS54Jxx EVM GUI

Figure 6 shows the front page of the ADS54Jxx EVM GUI as it should be seen upon opening the GUI. Descriptions for each of the tabs of the GUI are shown in Table 4.

ADS54Jxx EVM GUI v1.0	n		10000000000000000000000000000000000000						
ADS54Jxx EVM GUI v1.0									
ADS54Jxx LMK04828	Low Level View			USB Status 🧿 Reconnect FTDI ?					
RESET, Miscellaneous	JESD Test Patterns	LMFC Control	EVM Startup Sequence						
Analog Core Reset Digtal Core Reset (Not self-clearing) Flip ADC Data Ignore SYSREF Digtal Core Reset Layer Test Pattern Link Layer Testmode Testmode Disabled		LMFC Reseting Disabled	"Low Level View" tab. Choose the file onboard clock is used or choose the clock. Note that for the ADS54J69 det	external clock file to use an external cimation modes, the sampling rate should the final data rate. For instance, if the ecimation, then 1024 Msps should be					
JESD204B Core Setup		Powerdown	2. Press the "ADC RESET" button (SW reset to the ADC.	V1) on the EVM to provide a hardware					
JESD Mode Enable /A/ Character 40> JESD PLL Mode Enable /F/ Character Alignment Monitoring JESD PLL Mode Enable /F/ Character 20x mode. 4 Lanes/ADC		Global PDN		ing the "Load Config" button on the "Low					
20x mode, 4 Lanes/ADC Alignment Monitoring EN Programming of K Scrambling EN Frames per Mutti-Frame (K) JESD2048 Subclass 1 Subclass 0									
Manual SYNC Control	ILA Sequence								
Enable Software SYNC Software SYNC Sync Deasserted	Disable ILA Sequence ILA Sequence Delay No Delay								
Updated the Tree with register detail	s 4/20/2015 2:25:18 PM	Build: CC	NNECTED Idle	TEXAS INSTRUMENTS					

Figure 6. ADS54Jxx GUI

Table 4. ADS54Jxx GUI Tab Descriptions

Tab	Description	
ADS54Jxx	Enables control of the ADS54Jxx features. None of these controls need to be touched for basic operation. Instead, use the Low Level View tab to load configuration files.	
LMK04828	Enables control of many of the LMK04828 features. Configuration files can be used to setup the LMK04828 in known working configurations, however, this tab can be used to setup more advanced clocking schemes.	
Low Level View	Allows write and read access to all device registers. Also allows loading and saving of configuration files. The device configurations can be saved from this tab for use in the user's system. See Section 4.2 for more information.	



Software Description

4.2 Low Level View

The Low Level View tab, shown in Figure 7, allows configuration of the devices at the bit and field level. At any time, the controls described in Table 5 may be used to configure or read from the device.

		ADS54	Jxx GUI v1.5	Select the d	ADS54J40
DS54Jxx LMK04828	Low Level View				USB Status 🔵 Reconnect FTDI ?
Register Map			Write Data	Register Data	Register Data
Block / Register Name	Address Dofe		alue x 80		7
x17C x17D ADS54Jxx_ANALOG	Register	Map 🛛 🖁	x15 x0F Write Register	R W 0 TX_LINK_DIS	
0x00 MASTER 0x20 MASTER 0x21 MASTER 0x22 MASTER 0x26 MASTER 0x55 MASTER 0x55 ■ ADS54Jxx_DIGITAL MAID IGITAL 0x00 JESD DIGITAL 0x00 JESD DIGITAL 0x00 JESD DIGITAL 0x01 JESD DIGITAL 0x01 JESD DIGITAL 0x02 JESD DIGITAL 0x05 JESD DIGITAL 0x06 JESD DIGITAL 0x06 JESD DIGITAL 0x06 JESD DIGITAL 0x16 JESD DIGITAL 0x16 JESD ANALOG 0x16 DEC FLITER 0x00		RWW 8 00 RWW	x81 Write All x00 Read Data x00 x x00 Read Register x00 Read All x00 Read All x00 Read All x00 Read Adress x 69000 Note: Load Config will Overwrite all Registers. Load Config x00 Save Config	1 FRAME_ALIGN 2 LANE_ALIGN 3 FLIP_ADC_D4 4 TESTMODE_E 5 UNUSED 6 UNUSED 7 VCTRL_K[1	1/1] XTA[1/1]
Register Description	¥				¥
CTRL_K[7:7] Enable bit for number of frames pe 0x6906 TESTMODE_EN[4:4] Generates long transport layer test		set K is set in register	Block ADS54Jxx_DIGIT	Address	Write Data Read Data_Generic x 80 x 0 Write Register Read Register

Figure 7. Low Level View Tab

Table 5. Low Level View Controls

Control	Description
Register Map	Displays the devices on the EVM, registers for those devices, and the states of the registers.
	Selecting a register field allows bit manipulation in the Register Data section.
	• The Value column shows the value of the register at the time the GUI was last updated due to a read or write event.
Write Register button	Write to the register highlighted in the Register Map with the value in the Write Data field. This button must be clicked after changing bits in the register data section.
Write All button	Update all registers shown in the Register Map with the values shown in the Register Map log. The log can be viewed by double left clicking in the bottom left status bar of this page.
Read Register button	Read from the register highlighted in the Register Map and display the results in the Value column.
Read All button	Read from all registers in the Register Map and display the current state of hardware. Also updates the controls in the other tabs.
Load Config button	Write the ADC and LMK registers with data from the selected configuration file.
Save Config button	Create and save a configuration file that contains the current register information of both the ADC and LMK devices.
Register Data	Manipulate individual accessible bits of the register highlighted in the Register Map.
Generic Read/Write Register buttons	Perform a generic read or write command to the device shown in the <i>Block</i> drop-down box using the Address and Write Data information



5 Alternate Hardware Configurations

This section describes alternate hardware configurations in order to achieve better results or to more closely mimic the system configuration.

5.1 Clocking Options

The default clocking mode uses the LMK04828 to generate the ADC sampling clock and FPGA clocks. There are three additional clocking options that the EVM supports. These options are described in the following sections.

5.1.1 External ADC Sampling Clock

An external clock can be used as the sampling clock for the ADC. This clock can be provided through a transformer using the *ADC CLK* connector (J5). For this option, C65 and C73 need to be uninstalled and installed at C64 and C72. The LMK04828 must still be used to provide the device clock to the TSW14J56 and the SYSREF signals to both boards. This option provides the best performance, as long as the clock source has better phase-noise performance than the LMK04828. The source of the EXT ADC clock must be synchronized with the LMK04828. To accomplish this, send the 10-MHz reference output from the signal generator and connect it to J6 (LMK_CLKIN1) of the ADS54J69EVM. This causes LED D1 to illuminate indicating the LMK VCXO source is locked to the external reference clock. The provided LMK configuration files will work in this mode as well. If D1 does not illuminate, the signal from the outside source may be to low. To correct for this, click on the LMK04828 tab at the top of the GUI. When the LMK04828 page opens, click on the "PLL1 Configuration" tab. On the left middle side of the GUI, change the Buffer Type of CLKin1 from "Bipolar" to "CMOS" as shown in Figure 8.

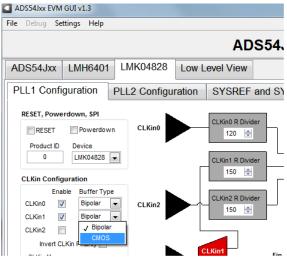


Figure 8. GUI CMOS Selection



Alternate Hardware Configurations

To turn off the ADC clock provided by the LMK04828 to reduce switching noise, click on the *LMK04828* tab, then click on *Clock Outputs* tab, then select *Powerdown* for *DCLK Type* under *CLKout 2 and 3*, as shown in Figure 9.

ADS54J40	LMK048	4828 Low Level View			
PLL1 Config	guration	PLL2 (Configur	ation	
CLKout 0 and 1 FPGA Clock & S	-	LKout 2 and DC Clock &		CLKout + Not Used	
Group Power Output Drive Input Drive	Level	Group Powe Output Driv Input Driv		Group Outpu Inpu	
DCLK Divider 16		DCLK Divider 4	•	DCLK D	
DCLK Source Divider	•	DCLK Source Divider	•	DCLK S Divider	
DCLK Type LVDS	Invert	DCLK Type Powerdown	Invert 🕅	DCLK T	
SDCLK Source		SDCLK Source	ce	SDCLK	

Figure 9. LMK04828 Clock Outputs Tab

5.1.2 External LMK04828 Clock (Clock Distribution Mode)

The LMK04828 can be used as a clock distributor. In this case, the LMK04828 uses in input clock source from LMK_CLKIN1 SMA connector (J6). SJP2 (XO_PWR) can be left open to turn off the onboard VCXO to avoid crosstalk. To use this mode, load the configuration file named *LMK_Config_External_Clock.cfg*. This mode allows generation of frequencies that are not possible with the LMK when using the on-board VCXO.

5.1.3 Clock Generator Using Onboard VCXO

The LMK04828 is used as a clock generator using the onboard 122.88 MHz VCXO. SJP2 must be shorted to turn on the onboard VCXO. The internal PLLs of the LMK04828 can be used with the onboard VCXO to generate the desired frequencies. To use this mode, load one of the configuration files named *LMK_Config_Onboard_xxx_MSPS.cfg*, where *xxxx* corresponds to the desired ADC sampling rate. A 10-MHz signal can be brought into the LMK_CLKIN1 input to synchronize to external instruments. This is the board default mode of operation.

5.2 Analog Input Options

The ADS54J69EVM allows for a differential analog input configuration in addition to the default using the single-ended transformer-coupled input. This option is described in the following section.

5.2.1 Differential Input

The analog input transformers can be bypassed in favor of a differential input source. This allows for a wider range of input frequencies, including the possibility of DC coupling. To configure the EVM for a differential analog input on Channel A, remove C6, C7, and R7 and install R3, R4, C1, and C3. For channel B, remove R8, C14, and C15 and install R21, R22, C12, and C13. All resistor values are 0 Ohms and capacitor values 0.1 uF. For a DC-coupled application, swap the series capacitors with 0- Ω resistors. The input signal must be biased to the required ADC input common mode voltage.



Jumper, Connector, and LED Descriptions

A.1 Jumper Descriptions

The EVM jumpers are shown in Table 6 as well as the default settings for the jumpers. Use this table to reset the EVM in the default configuration, in case of issues.

Table 6. Jumper	Descriptions and Default Settings
-----------------	--

Jumper	Description	Default setting
SW1	ADC hardware reset (active high)	Logic low
SJP2		
SJP1		
SJP3	Selects either diff sync or single-ended sync from FMC. Default is diff.	Shunt pins 2-3

A.2 Connector Descriptions

The EVM connectors and their function are described in Table 7.

Table 7. Connector Descriptions

Connector	Description	
J2	Channel A positive analog input	
J1 (Not installed)	Channel A negative analog input. Used for differential input mode only.	
J3	Channel B positive analog input	
J4 (Not installed)	Channel B negative analog input. Used for differential input mode only.	
J5	External ADC sample clock input	
J6	LMK04828 reference clock input	
J7	JESD204B FMC connector. Interfaces to TSW14J56EVM or FPGA evaluation boards	
J8 (USB)	USB interface connector. Not used.	
J9 (+5V IN) 5-V power supply input		



LED Descriptions

A.3 LED Descriptions

The EVM LEDs are described Table 8.

Table 8. LED Descriptions

Connector	Description
D3	Not used
D4	5 VDC power present
D2	LMK04828 locked to VCXO
D1	VCXO locked to external reference applied to J6

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2016) to B Revision

Page

•	Deleted ADS54J69 GUI Configuration for Decimate-by-4 with Digital Mixer section from Software Setup Procedure	
	section.	6
•	Deleted HSDC Pro GUI Configuration section from Software Setup Procedure section.	6

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- Increase the separation between the equipment and receiver.
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