TAS3204 Low Power Operation

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ABSTRACT

For portable or other power-sensitive applications, it may be desirable to decrease the power consumption of the TAS3204 at the expense of decreasing performance and/or increasing external circuitry.

Power Reduction Techniques

The first technique for reducing power consumption is reducing the clock speed of the digital core. The default clock frequency of the TAS3204 is 135 MHz. Reducing this frequency causes a corresponding linear loss in DSP programming cycles. For example, when operating at 135 MHz (assuming 48-kHz Fs), 2816 cycles are available to the programmer. However, at 67.5 MHz, only 1408 cycles are available. Another drawback of reclocking the digital core is that it can only be done when the part is operated in slave mode and is provided with an external 512Fs clock to drive the analog circuitry. The reason for this can be seen in Figure 1.

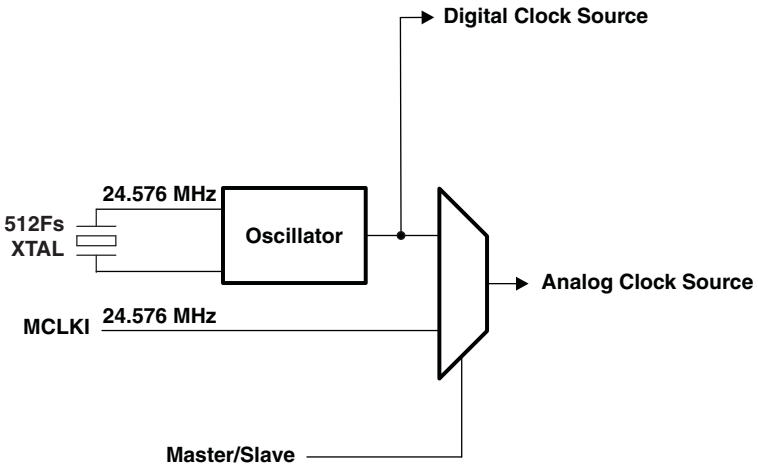

Figure 1. Master/Slave Clock Diagram

The digital core clock is driven by the crystal oscillator regardless of master/slave mode. The analog clock (which must be 24.576 MHz to guarantee analog performance) is driven by the crystal oscillator when the TAS3204 is in master mode, and by an external MCLK when in slave mode. The clock speed of the digital core can be decreased simply by changing crystals.

Using a 12.288-MHz crystal rather than the default 24.576-MHz crystal reduces the operating frequency from 135 MHz to 67.5 MHz. The digital core consumes approximately 130 mA during normal operation at 135 MHz. It consumes approximately 70 mA while operating at 67.5 MHz.

A second technique for reducing power consumption is bypassing the internal 1.8-V linear regulators. This is accomplished by powering down the regulators and providing an external 1.8-V supply. The TAS3204 utilizes linear 1.8-V regulators to derive the digital supply voltages from the single required 3.3-V input power supply. This linear drop results in nearly half of the power consumed by the digital circuitry being dissipated in the 1.8-V regulators. Utilizing a more efficient external 1.8-V switching power supply, such as the Texas Instruments TPS6220x family of step down converters, can significantly reduce this loss. The procedure for using an external supply is to first power down the internal 1.8-V regulators by pulling the VREG_EN (active low) pin high, then to apply the external 1.8-V source to pins VR_DIG, VR_ANA, VR_PLL. The TAS3204 must either be held in reset during this sequence or be reset after it is complete.

During normal operation using the internal 1.8-V regulators, the digital core of the TAS3204 dissipates approximately 430 mW of power. When powering down the regulators and using an external 1.8-V switching supply, the digital core dissipates approximately 215 mW of power.

The power numbers quoted above reflect only the power consumed by the digital core of the TAS3204. Table 1 summarizes the total power consumption (discrepancy is due to analog power consumption) of the TAS3204, under nominal operation, for the described techniques.

Table 1. Summary of Power Consumption

Operating Mode	Total Power Consumption	
	mA	mW
135 MHz, internal regulators on (default operation)	190	627
67.5 MHz, internal regulators on	130	429
135 MHz, bypassing internal regulators	175	405 (1)
67.5 MHz, bypassing internal regulators	115	297 (1)

(1) Due to digital core voltage supply of 1.8 V instead of 3.3 V

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