Wired-Logic Signaling With M-LVDS

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ABSTRACT

M-LVDS devices provide true multipoint functionality. M-LVDS standard contention provisions and Type-2 M-LVDS receivers allow use of these devices in wired-logic signaling designs. This application report discusses M-LVDS features that support wired-logic signaling, compares this to LVDS features, and demonstrates wired-OR signaling with Texas Instruments M-LVDS compliant transceivers.

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1 Introduction

The ratification and publication of TIA/EIA-899 in early 2002 introduced multipoint-low-voltage-differential signaling or M-LVDS. It specifies the electrical characteristics of a shared differential data bus with up to 32 connections and signaling rates up to 500 Mbps. It also specifies a Type-2 receiver with a nominal 100-mV differential input voltage threshold offset and suggests interface designers use it for failsafe provisions or wired-logic signaling at lower signaling rates (than Type-1 receivers). The standard offers no guidance on the maximum wired-logic signaling rate other than recommending reflected-wave switching.

Wired-logic signaling is a common technique used on multipoint bus interface standards. Examples include the controller area network (CAN), small-computer systems interface (SCSI), IEEE-488 (GPIB), IEEE-896 (BTL), and others. Often called wired-OR signaling, it provides the equivalent OR gating of all the outputs on the signal line(s) and collision detection. Multipoint protocols most often use wired-logic signaling during bus arbitration, but some also use it during data transfer phases.

Wired logic provides a simple means of sharing a bit of information among physically separated nodes without the need (and cost) of a sophisticated protocol. In the simplified schematic diagram of Figure 1, switches A through N represent the nodes connected to a common signal X. When one switch is closed, the division of V by R and R_T determines the voltage on X. If the voltage at X with one switch closed exceeds the logic threshold, closing one or more switches just brings the voltage at X closer to V. However, the logic state remains the same until all switches are opened, returning X to zero volts and changing the logic state. Logically this is an OR gate.

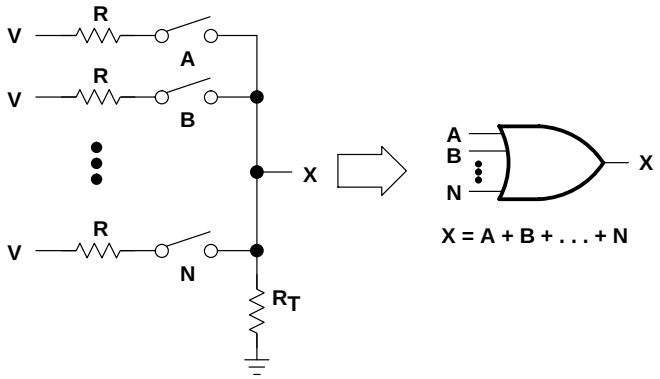

Figure 1. Wired-OR Gate

The circuit in Figure 1 uses positive logic, a single-ended signal, and switches. In actual practice, you replace the switches with transistors in line circuits. You can implement negative logic or other logic gate functions with some well-placed inverters. Also, you can apply the same concept using differential line drivers and receivers, but all applications drive the load actively in one state only, and passively in the other.

Using the configuration in Figure 2, and an R_L of 50 Ω, parallel operation of multiple wired-OR M-LVDS drivers should provide differential bus voltage of zero volts with all drivers transmitting a low. With one or more drivers transmitting a high to the bus, the bus voltage should be about 500 mV or above.

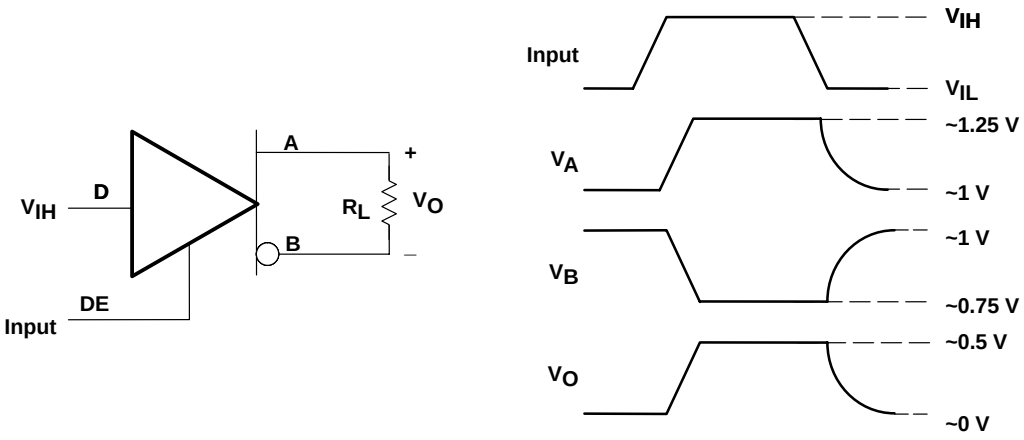

Figure 2. Wired-OR Operation of M-LVDS Driver

As stated earlier and illustrated in Figure 3, the input thresholds of Type-2 M-LVDS receivers are offset from zero to provide some differential noise margin and receive this signal when no drivers are active. With a differential input voltage threshold of 50 mV to 150 mV, the worst-case differential noise margin is 50 mV in the low state. Whether this margin is sufficient depends greatly on the system design and signaling rate.

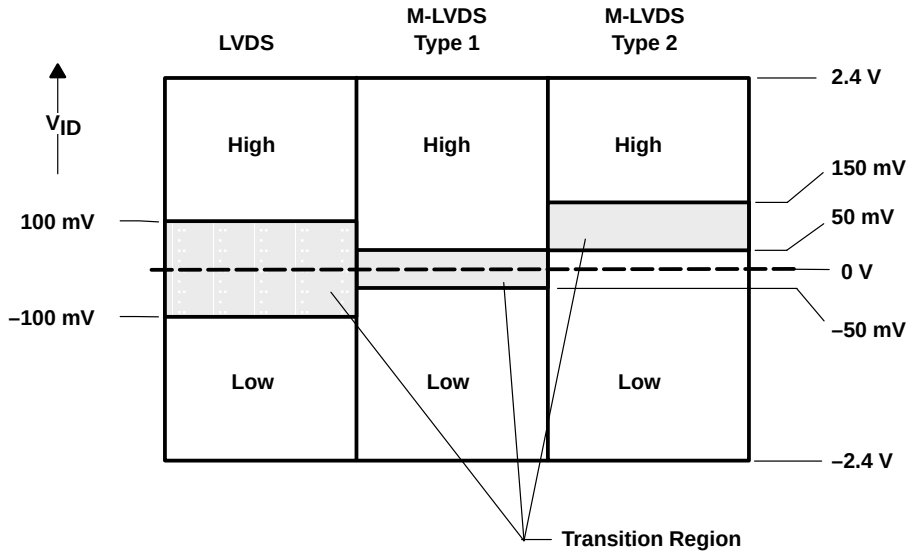

Figure 3. Differential Input Voltage Threshold Comparison

The objective of this investigation is to implement a wired-OR bus using M-LVDS with Type-2 receivers, examine the signals and quality, and draw some general conclusions as to its applicability. Specifically, we determine the maximum signaling rate for wired-OR operation of Texas Instruments' SN65MLVD204 M-LVDS Transceiver in a four-node multipoint connection of M-LVDS evaluation modules (EVMs).

In an effort to keep lab time manageable, we base signal quality upon eye-pattern measurements, include only typical operating conditions, and limit the number of line circuit samples and bus loading combinations. Additionally, and due to the many variables involved, we leave crosstalk and live insertion with wired-OR M-LVDS, to future investigation.

2 Materials

- (4) M-LVDS evaluation module (EVM), MLVD20XEVM
- HFS9003 stimulus system
- TDS784 digital oscilloscope
- FET probes
- Power supply
- CAT5 unshielded twisted-pair cable (as required)

3 Methods

Four M-LVDS EVMs are populated with the SN65MLVD204 100-Mbps M-LVDS transceivers and are bused together using 0.5 m of CAT5 unshielded twisted-pair cable without a jacket. 100-Ω resistors terminate the bus at each end and all EVMs are powered from the same power supply set to 3.3 V. Figure 4 schematically illustrates the test setup.

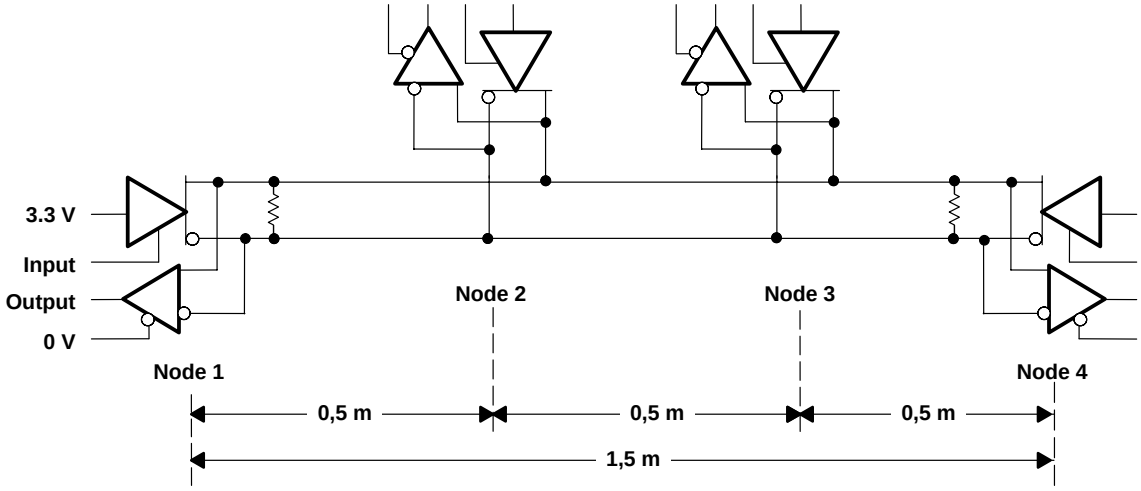

Figure 4. Test Bus Schematic Diagram

The peak-to-peak differential bus signal is measured before applying power to the system and any input signals. The driver at node 1 is enabled (3.3 V) and the steady-state differential bus signal measured. This is repeated after enabling the drivers at nodes 2, 3, and then 4, such that all nodes are on.

After returning all nodes to the off or disabled state, the HFS9003 is set to output a 100-Mbps pseudo-random bit sequence (PRBS) with a run length of 2^{23}–1. The input levels are set to swing from 0.8 V to 2.2 V and applied to the driver enable at node 1. Eye-pattern images are captured for the differential receiver input and single-ended receiver output at each of the four nodes. The input signaling rate is increased to 200 Mbps and the measurements are repeated.

The signaling rate is reduced to 100 Mbps and the input moved to the driver at node 3. The eye-pattern images are again captured for all nodes.

An additional input signal is set up and applied to the driver at node 1. Again, with an input voltage swing from 0.8 V to 2.2 V, the signal is set to a 50% duty cycle pulse output. Eye–patterns are captured at each node.

4 Results

The differential noise floor is measured at approximately 10 mVpp with or without system power applied.

The steady-state bus differential voltage with one driver enabled is 520 mV. This increases to 1,000 mV with two drivers active, with no perceptible change in this level by turning on nodes 3 and 4.

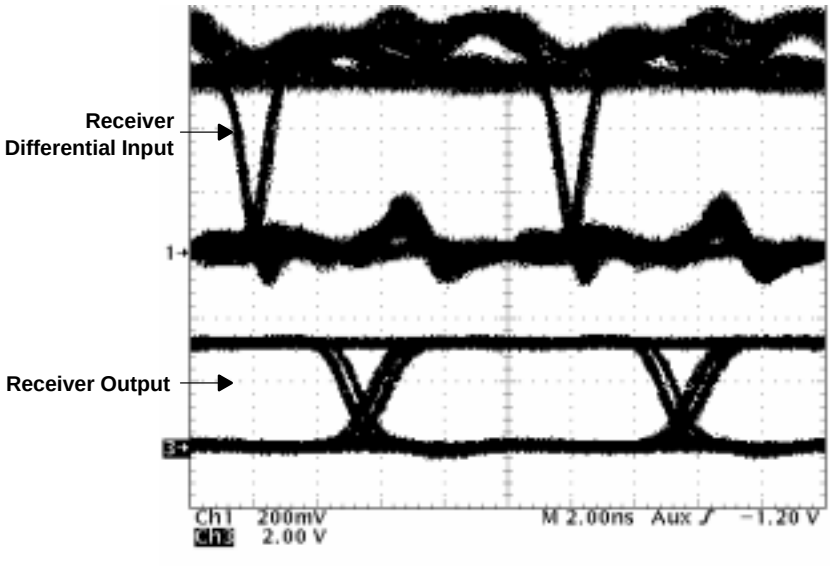

Figure 5. Eye Patterns at Node 1 With 100-Mbps PRBS Into Node 1

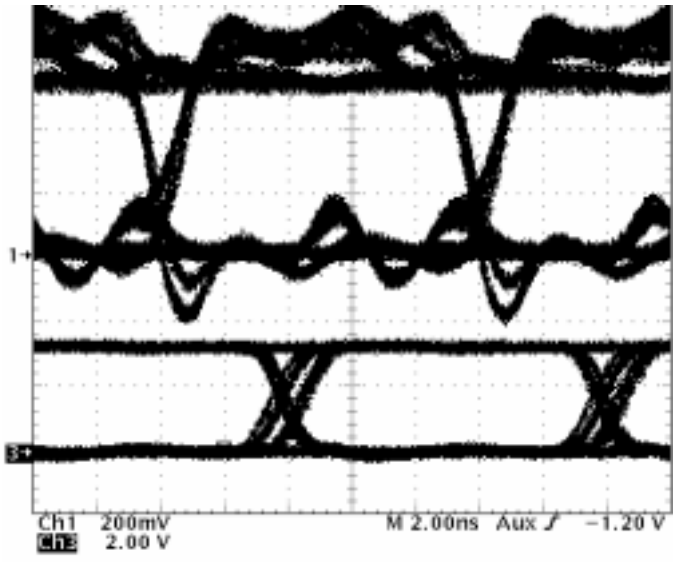

Figure 6. Eye Patterns at Node 2 With 100-Mbps PRBS Into Node 1

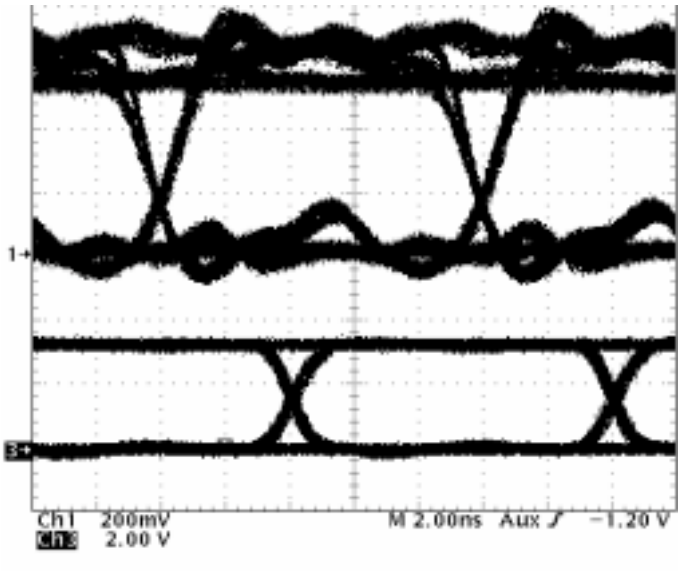

Figure 7. Eye Patterns at Node 3 With 100-Mbps PRBS Into Node 1

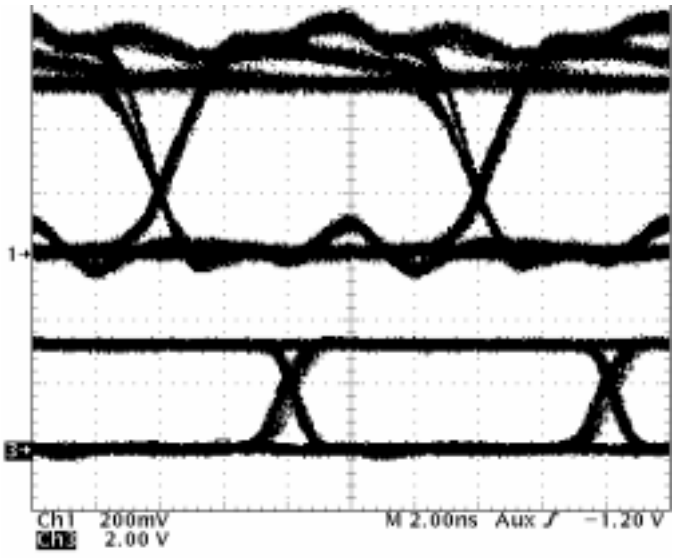

Figure 8. Eye Patterns at Node 4 With 100-Mbps PRBS Into Node 1

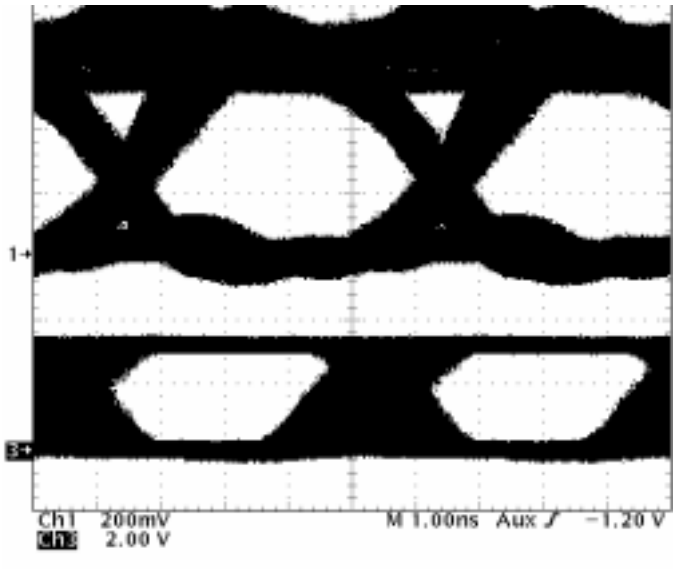

Figure 9. Eye Patterns at Node 4 With 200-Mbps PRBS Into Node 1

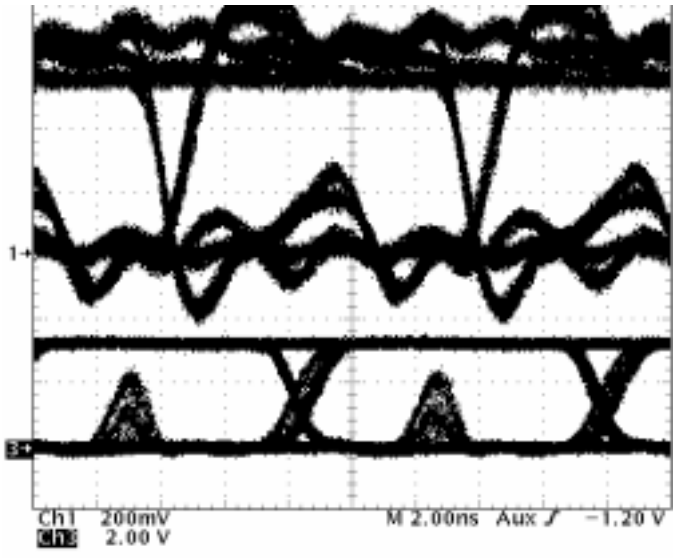

Figure 10. Eye Patterns at Node 2 With 100-Mbps PRBS Into Node 3

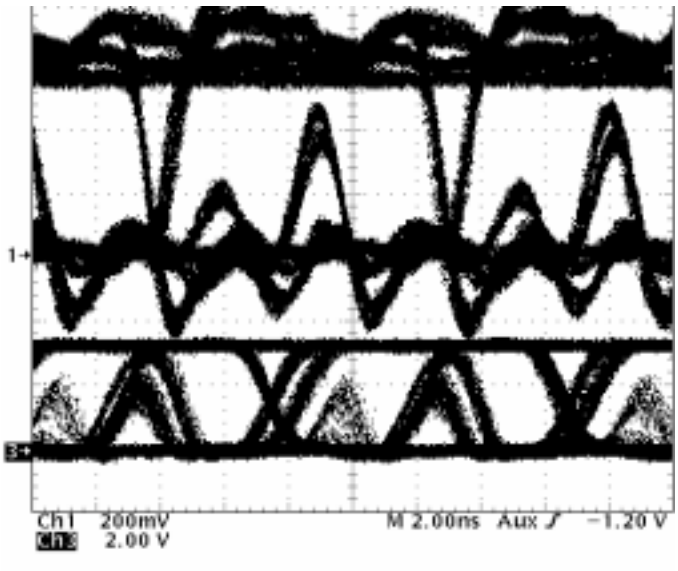

Figure 11. Eye Patterns at Node 3 With 100-Mbps PRBS Into Node 3

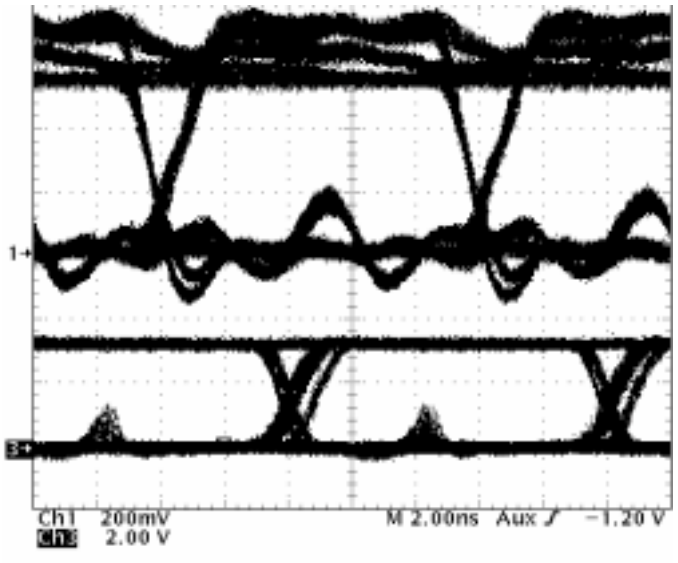

Figure 12. Eye Patterns at Node 4 With 100-Mbps PRBS Into Node 3

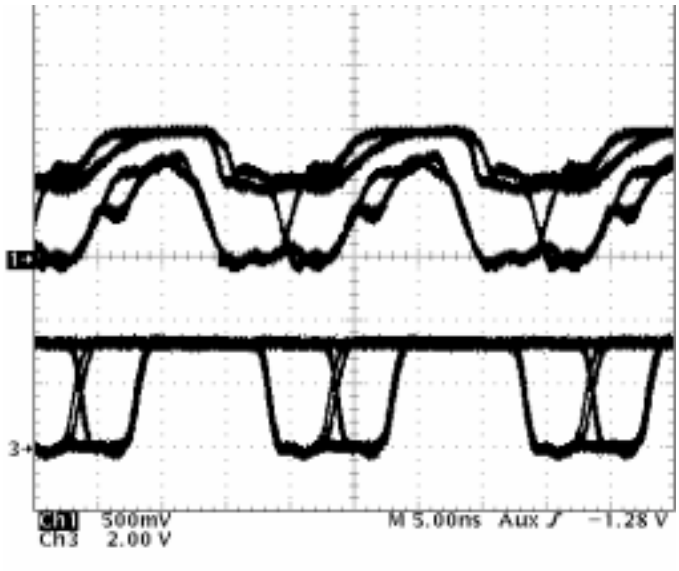

Figure 13. Eye Patterns at Node 4 With PRBS Into Node 3 and Pulse Into Node 1

5 Discussion

5.1 Steady-State Differential Bus Voltages

We find the steady-state output voltage with one driver to be 520 mV, and within the specified range in the data sheet of 480 mV to 680 mV. Enabling one additional driver approximately doubles the output to 1000 mV, indicating relatively high driver output impedance with respect to the 50-Ω load. High driver output impedance relative to the load makes the driver appear more like an ideal current source than an ideal voltage source. If so, the bus differential voltage would increment by about 500 mV when enabling each additional driver.

This is not the case, as enabling the third and fourth driver causes no perceptible change in the steady-state differential bus voltage. The limitation of the differential bus voltage to 1 V is due to the design of the SN65MLVD204, where current sources in the driver output circuit begin to shut off as the ground-referenced output voltage approaches supply rails. This limitation is well within the maximum allowed by the TIA/EIA-899 standard and leaves more of the bus voltage range to for allocation to common-mode noise. A lower differential bus voltage is also a benefit in incident-wave wired-OR signaling, as jitter from intersymbol interference is lower than it would be with higher signal levels.

In any case, one enabled driver exceeds the maximum Type-2 receiver differential input voltage threshold of 150 mV. Additional enabling of drivers only increases the differential noise margin when the bus is at a high-level. The steady-state differential voltage for the low state (all drivers disabled) in this system is 0 V. The worst-case noise margin would occur with the lowest possible receiver input voltage threshold of 50 mV. Of this 50 mV, 5 mV is allocated to random differential noise as we found a 10 mV peak-to-peak, or 5 mV differential noise floor in this system. This leaves 45 mV in the worst-case for other differential noise.

5.2 Eye-Pattern Anomalies and Causes

Referring to Figure 5, we see that the receiver output eye is about 84% open at 100 Mbps using 50% of the amplitude as the threshold. This is considered recoverable in most systems. We also observe that using a threshold of 0.8 V would open the eye to about 92%. This asymmetry matches that at the input and is due to a difference between the high-level-to-high-impedance and high-impedance-to-high-level output delay times of the driver.

We also observe an area of concern in the receiver differential input eye pattern with a nearly 200-mV *bump* mid-pulse in the low state. It is most likely a result of reflections from the other nodes located 2.5 ns, 5 ns, and 7.5 ns away from node 1 and our observation point. If so, it takes a round-trip delay of 5 ns, 10 ns, or 15 ns for the wave to travel down the bus, impinge on the impedance mismatch between the cable and stub, and for the reflected wave to return to our observation point. Since a wave is launched from node 1 every 10 ns, it is probable that the anomaly is the superposition of reflected waves from node 2 and the last transition and from node 4 and two transitions prior. It is obvious from the receiver output eye pattern that the *bump* is either too short in duration or of insufficient amplitude to cause the receiver output to change.

Moving the observation points to the other nodes (Figure 6, Figure 7, and Figure 8) reveals little significant change in the eye opening at the receiver outputs. We do observe some variation in the amplitude and duration of reflected voltage at the receiver input as they combine or subtract at different times.

Doubling the signaling rate to 200 Mbps in Figure 9 gives a receiver output eye that is 56% open. The reflections, which are obvious in the previous figures, are now indistinguishable because bus transitions are occurring at the 5 ns multiples of the round-trip delays and masking their presence. This most likely contributes to closing the eye to 56%, however.

Figure 10 shows that the impedance mismatches created by our connections to the cable have now created sufficient voltage the receiver input to cause the output to change. This is more pronounced in Figure 11 where multiple reflections are being seen at the receiver output. The cause is that we are now launching a wave at node 3 in the middle of the bus and getting a combination of reflections from both nodes 2 and 4 from the same bus transition and rendering the system unusable at this signaling rate.

Examination of our EVMs reveals a good deal of test points and other components that are adding parasitic capacitance to the stub. Figure 14 shows our worst-case condition of driving and monitoring at node 3 steadily improve as extraneous capacitance is removed from the EVM and bus connection until, ultimately, the receiver output eye opens and the system becomes usable.

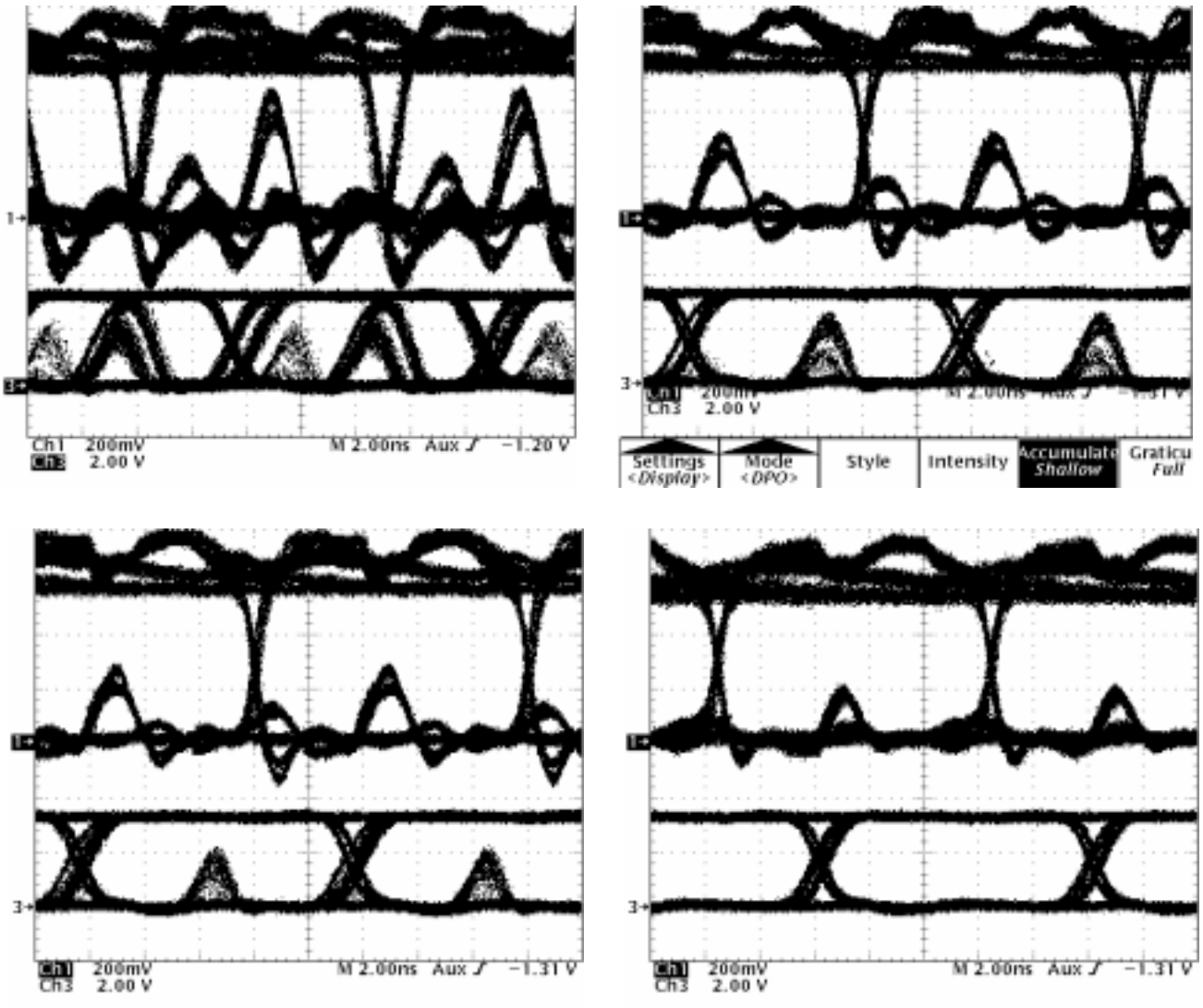

Figure 14. Eye Patterns Into and Measured at Node 3 as Capacitance Decreased

Removing the source of reflected waves is not always an option. One method of adding differential noise margin is by adding a steady-state differential bias to the bus signal. Since there is more than enough high-level margin, this technique takes some of the positive margin and adds it to the low-level margin. This is done by modifying our test bus terminations to that shown in Figure 15.

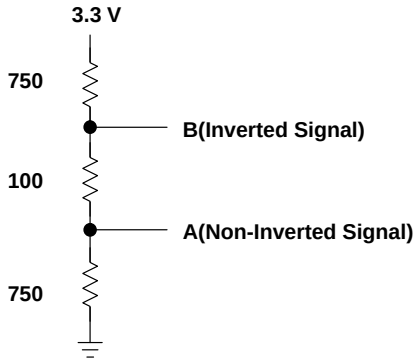

Figure 15. Termination Modification for Increasing Noise Margin

The eye patterns with the modified termination in Figure 16 show that the differential signal now swings between –200 mV and 300 mV. Based upon a 100-mV threshold, the low-level margin is now 100 mV above our reflected noise bump and the high-level margin is 200 mV.

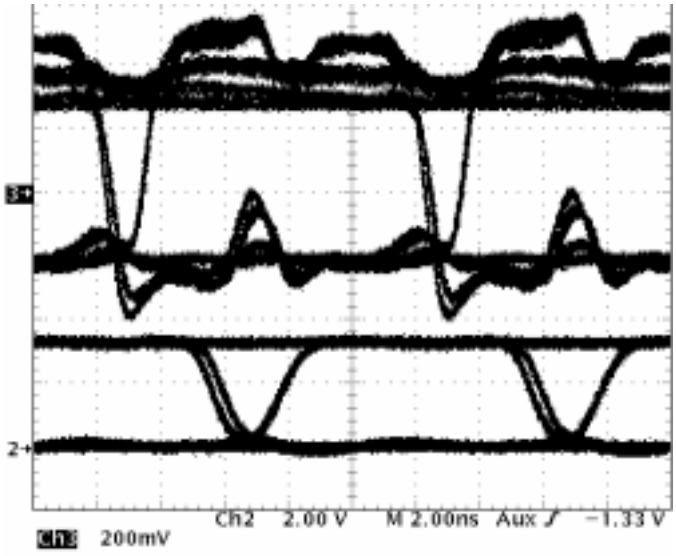

Figure 16. Eye Patterns at Node 3 With 100-Mbps PRBS Into Node 3 With Modified Terminations

In our final examination, Figure 13 shows the results of driving nodes 1 and 3 simultaneously with different data patterns. Node 3 is transmitting the PRBS, while node 1 transmits a 50% duty-cycle pulse train at the same signaling rate. The terminations are returned to the original 100Ω resistors only and the signaling rate is lowered to 50 Mbps for display purposes. In the eye pattern of the receiver output at node 4, we see the pulsed signal from node 1 imbedded in the middle of, what up to now has been, a normal eye pattern. While the signal from node 3 is randomly driving the bus high or low, the predictable high level from node 1 forces the bus to a high, regardless of the output from node 3. This gives the effective OR-gate output on the bus and is repeated at the receiver output at node 4.

6 Summary and Conclusions

The eye patterns measured on a test bus consisting of four SN65MLVD204 M-LVDS EVMs separated by 0,5 m of twisted-pair cable show the capability of incident-wave wired-OR signaling at rates exceeding 100 Mbps. Due to reflections, it is necessary to reduce the stub capacitance presented by the EVMs to achieve these rates when transmitting from nodes located in the middle of the bus.

The worst-case noise margin of 50 mV provides little room for reflections from impedance discontinuities along the bus and likely does not provide sufficient noise margin for incident-wave switching for all but pristine multipoint buses. The framers of TIA/EIA-899 are correct in recommending reflected-wave switching for wired-OR signaling with M-LVDS and Type-2 receivers. Reflected-wave switching would require sampling of the bus state after a round-trip delay of the bus. For the test bus, this would be 15 ns and a maximum signaling rate of 66.7 Mbps (not including setup and hold times for sampling). Centering the differential signal swing about the threshold by adding a steady-state differential bias through termination resistors may provide sufficient noise margin for incident-wave switching and higher signaling rates for the less than pristine multipoint buses.

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