

Accurate PWM Duty Cycle Clamp

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ABSTRACT

Power supply applications using current sense transformers require a duty cycle clamp on the pulse width modulator (PWM) to ensure transformer reset. Not all PWMs come with a duty cycle clamp, presenting a problem for the power supply designer. This application note shows how to implement a duty cycle clamp by using a simple delay circuit.

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1 Duty Cycle Clamp Circuit

The circuit in Figure 1 can be used affectively to clamp the maximum duty cycle of PWM controller. It is a simple delay circuit that consists of ten passive components, a diode, LM311 comparator and a MOSFET driver. Note there are two holdup/bypass capacitors for the UC3705 and the LM311 that are not shown in Figure 1.

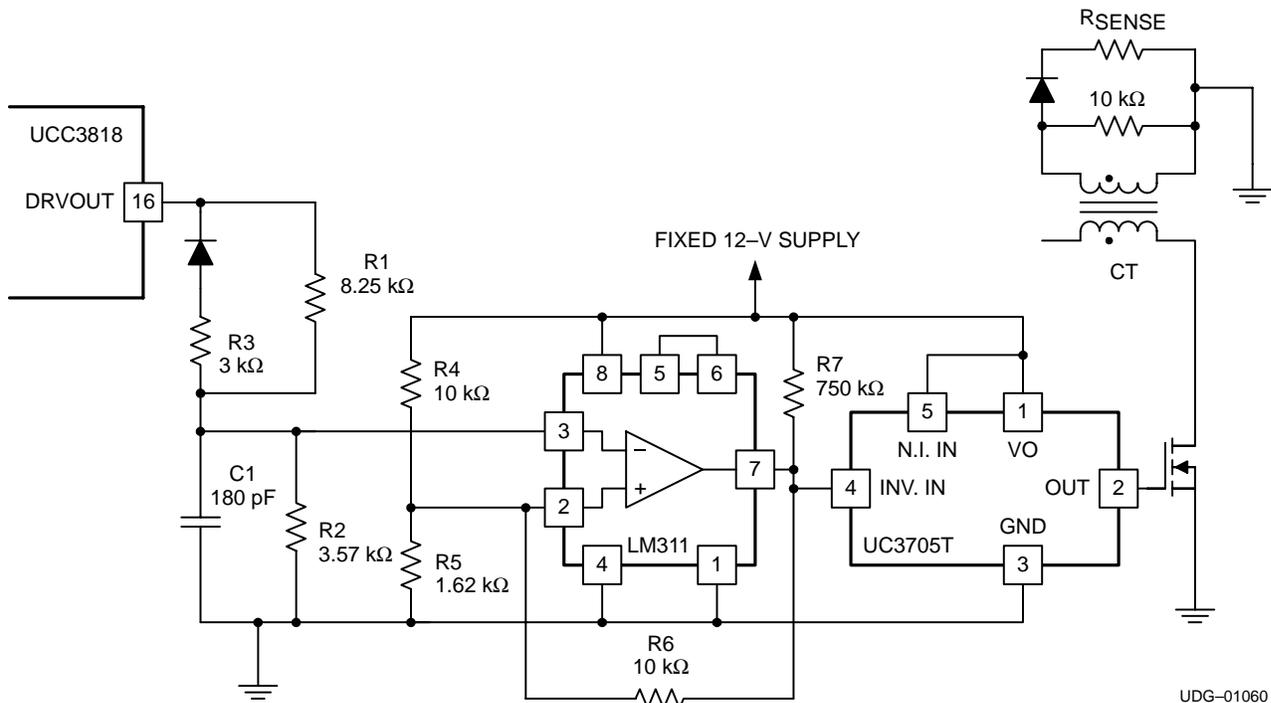


Figure 1. Maximum Duty Cycle Clamp Application

2 Theory of Operation

When the gate drive of the UCC3818 transitions from low to high resistors R1, R2 and capacitor C1 form a timing delay to the LM311 comparator. When the threshold voltage of the comparator is reached, it activates the UC3705 MOSFET driver. Resistors R4, R5, R6 and R7 along with the LM311 form a hysteretic comparator that is required for circuit stability. Resistor R3 and diode D1 provide a fast discharge path for C1 during circuit reset, which occurs when the gate drive goes low.

2.1 Design Example

Resistors R1 and R2 attenuate the gate drive signal. Diode D1 and resistor R3 speed up the turn off of the comparator. The following equations can be used to calculate the size of R2 and R3. V_{RPEAK} is the peak ramp voltage, which is selected to be 3.6 V. V_{GATE} is the maximum gate drive voltage of the UCC3818, which is approximately 12 V for this design. V_D is the forward diode drop of D1 and $I_{GATE(max)}$ is the maximum gate drive current that the PWM controller can sink. For this design the $I_{GATE(max)}$ is 1.2 A and the diode used is a 1N4148, which has a forward voltage drop of 0.7 V. R1 is selected to be a standard 8.25 k Ω resistor, giving R2 a value of roughly 3.57 k Ω .

$$R2 = R1 \times \frac{V_{RPEAK}}{V_{GATE} - V_{RPEAK}} \approx 3.57 \text{ k}\Omega, R3 = \frac{V_{RPEAK} - V_D}{I_{GATE(max)}} \approx 3\Omega \quad (1)$$

Equation (2) is used to set up the LM311 comparator, where V_{FIXED_SUPPLY} is the supply voltage to the comparator and V_{TRIP} is the comparator trip voltage. For this design example V_{TRIP} was selected to be 3 V and R6 was selected to be 10 k Ω . Note for this equation to hold true R4 must be set to the same value as R6.

$$R5 = \frac{1}{2} \times V_{TRIP} \times \frac{R6}{V_{FIXED_SUPPLY} - V_{TRIP}} \approx 1.62 \text{ k}\Omega \quad (2)$$

After the components are selected, it is a good idea to check the hysteresis level to ensure the comparator will turn on and off correctly. Equation (3) can be used to calculate the hysteresis (V_{HYST}) of this design example. For this design example, the hysteresis is approximately 1.5 V.

$$V_{HYST} = \frac{V_{FIXED_SUPPLY} \times \left(\frac{R5 \times R6}{R5 + R6} \right)}{R4 + \left(\frac{R5 \times R6}{R5 + R6} \right)} \approx 1.5 \text{ V} \quad (3)$$

After the comparator has been set up, component C1 can be selected using equations (4) and (5), where t_{DELAY} is the turn on delays of the LM311 and UC3705 less the turn off delays of the comparator and MOSFET driver, t_{DELAY} is roughly 100 ns. Variable D_{MAX} is the maximum duty cycle and f_s is the PWM's switching frequency. For this design example D_{MAX} is set to 0.9 and the switching frequency was selected to be 100 kHz.

$$t = (1 - D_{\text{MAX}}) \times f_s - t_{\text{DELAY}} = 900 \text{ ns}, \quad (4)$$

$$C1 = \frac{\ln \left[1 - \frac{V_{\text{TRIP}}}{V_{\text{GATE}} \times \left(\frac{R2}{R1 + R2} \right)} \right]}{\frac{R1 \times R2}{R1 + R2}} \approx 220 \text{ pF} \quad (5)$$

Figure 2 shows that the duty cycle was clamped to roughly 90%. Channel 2 is the gate drive of the UCC3818. Channel 1 is the output of the UC3705 gate driver. Channel 3 is the voltage at the inverting input of the LM311 comparator and Channel 4 is the voltage at the non-inverting input of the comparator.

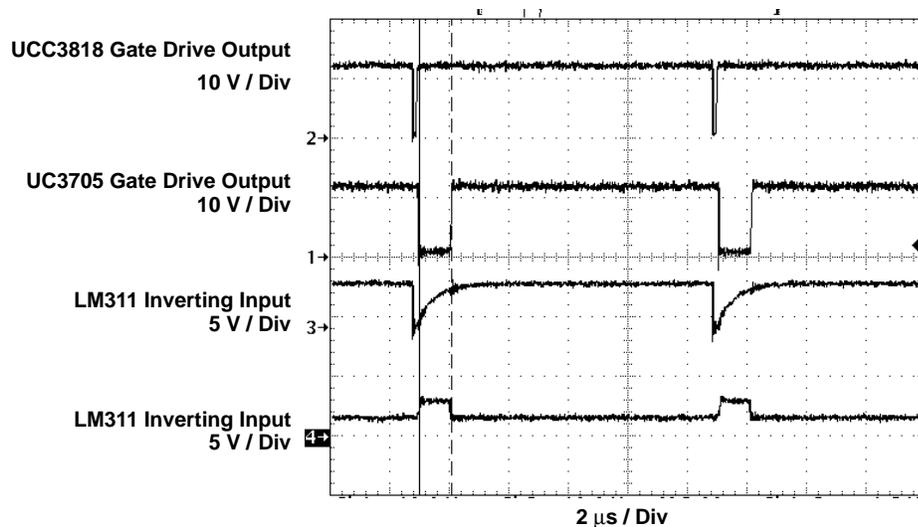


Figure 2. Clamping Waveforms

A duty cycle clamp on the PWM is required to reset a current transformer used in power supply applications. If the PWM used in the design does not have a duty cycle clamp, such as the UCC3818, additional circuitry will be required. This design example shows the duty clamp being implemented with delay circuit and MOSFET driver.

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