10-Watt Flyback Converter Using the UCC3809

Power Supply Control Products

Contents

1 Introduction

1.1 Design Procedure

The UCC3809EVM evaluation module is an isolated 10-W, 3.3-V converter designed for telecom input voltages, nominally –48 Vdc but ranging from –32 Vdc to –75 Vdc. The UCC3809 economy primary-side controller is used as the pulse-width modulator (PWM), combined with a TLV431 low-voltage adjustable-precision shunt regulator on the secondary side. The nominal switching frequency for this converter is approximately 400 kHz. The UCC3809 is configured with a 50% duty-cycle clamp.

1.2 Operating Specifications

SPECIFICATION	MIN	TYP	MAX	UNITS
Input voltage range	32	48	75	V
Output voltage range	3.218	3.3	3.383	V
Output current range	0		3.3	A
Operating frequency	344	380	420	kHz
Output ripple			100	mV
Efficiency (V_{IN} = 48 V, I_{OUT} = 3 A)		75		%

The circuit, shown in Figure 1, is a discontinuous fixed-frequency current-mode controlled flyback converter. This converter contains features such as external shut down, optocoupler isolation, programmable maximum duty cycle, and a summing node for voltage feedback, current sense, and slope compensation.

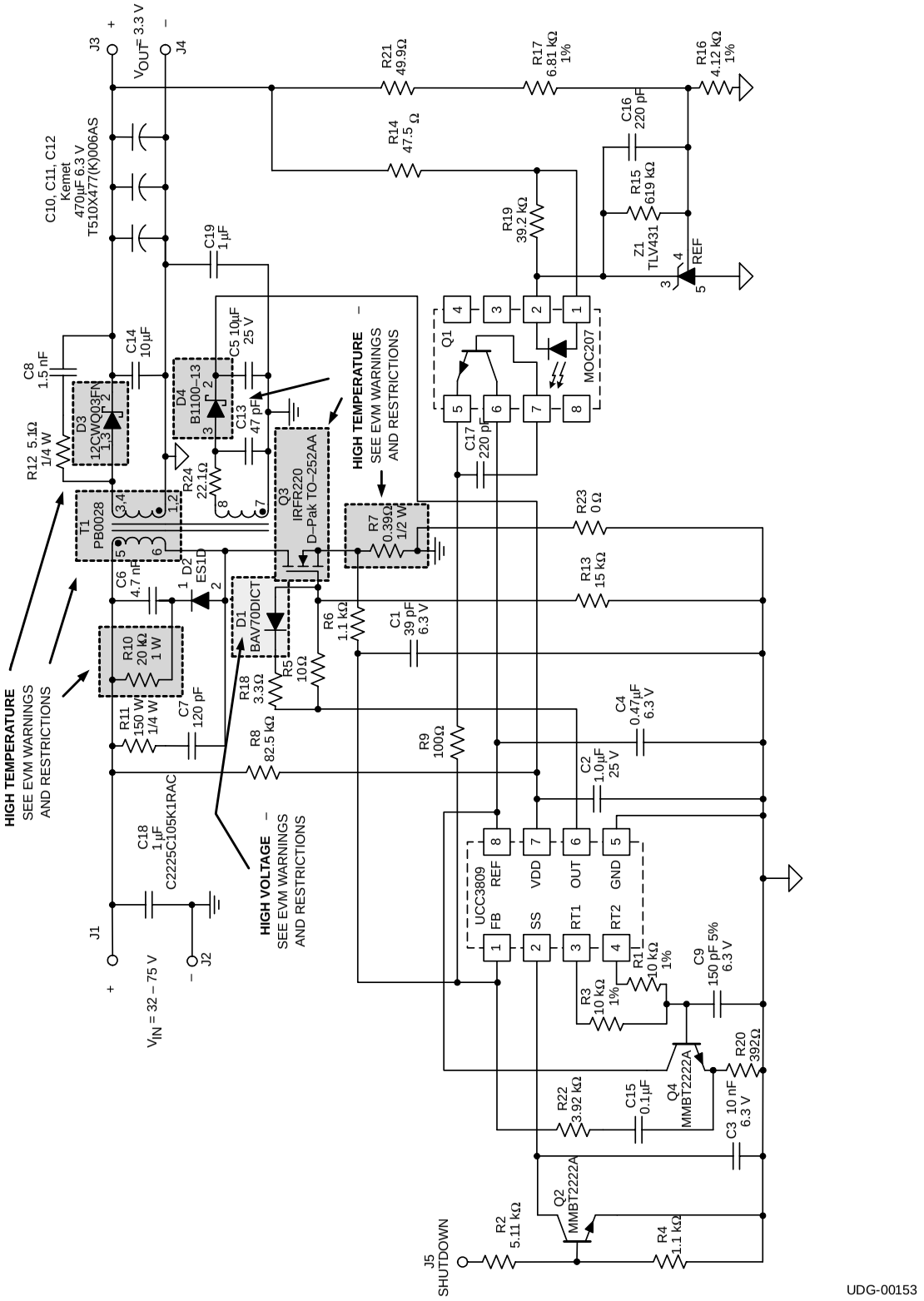
Table 1. UCC3809 10-W Flyback Converter Bill of Materials

	Reference	QTY	Description	Manufacturer	Part Number
Capacitor	C1	1	Ceramic, 39 pF, ±5%, 50 V, NPO, 0603	Panasonic	ECJ–1VC1H390J
	C2	1	Ceramic, 1.0 µF, +80%/–20%, 50 V, Y5V, 0805	Taiyo Yuden	UMK212F105ZG
	C3	1	Ceramic, 10 nF, ±10%, 50 V, X7R, 0603	Panasonic	ECU–V1H103KBV
	C4	1	Ceramic, 0.47 µF, +80%/–20%, 16 V, Y5V, 0603	Panasonic	ECJ–1VF1C474Z
	C5	1	Ceramic, 10 µF, ±10%, 35 V, Y5V, 1210	Taiyo Yuden	GMK325F106ZH
	C6	1	Ceramic, 4.7 nF, ±10%, 50 V, X7R, 0603	Panasonic	ECU–V1H472KBV
	C7	1	Ceramic, 120 pF, ±5%, 50 V, NPO, 0603	Panasonic	ECJ–1VC1H121J
	C8	1	Ceramic, 1.5 nF, ±10%, 50 V, X7R, 0603	Panasonic	ECU–V1H152KBV
	C9	1	Ceramic, 150 pF, ±5%, 50 V, NPO, 0603	Panasonic	ECU–V1H151JCV
	C10, C11, C12	3	Tantalum, 470 µF, ±10%, 6.3 V, 7343H	Kemet	T510X477K006AS *
	C13	1	Ceramic, 47 pF, ±5%, 50 V, NPO, 0603	Panasonic	ECJ–1VC1H470J
	C14	1	Ceramic, 10 µF, ±10%, 6.3 V, X5R, 1206	Taiyo Yuden	JMK316BJ106ML
	C15	1	Ceramic, 0.1 µF, +80%/–20%, 16V, Y5V, 0603	Panasonic	ECJ–1VF1C104Z
	C16, C17	2	Ceramic, 220 pF, ±5%, 50 V, NPO, 0603	Panasonic	ECU–V1H221JCV
	C18	1	Ceramic, 1 µF, ±10%, 100 V, X7R, 2225	Kemet	C2225C105K1RAC *
	C19	1	Ceramic, 1 µF, ±10%, 16 V, X7R, 1206	Panasonic	ECJ–3YB1C105K

NOTE: * Equivalent substitution not recommended

	Reference	QTY	Description	Manufacturer	Part Number
Diode	D1	1	Fast Switching, 70 V, 10 mA, SOT–23	Vishay/LiteOn Power Semiconductor (Diodes Inc.)	BAV70DI
	D2	1	Ultra-Fast, 200 V, 1 A, SMA/DO–214AC	Vishay/LiteOn Power Semiconductor (Diodes Inc.)	ES1DT
	D3	1	SCHOTTKY, 30 V, 12 A, TO–252AA	International Rectifier	12CWQ03FN
	D4	1	SCHOTTKY, 100 V, 1 A, SMA/DO–214AC	Diodes, Inc.	B1100–13
Optoisolator	Q1	1	846–01, STYLE 1	Motorola	MOC207
Transistor	Q2, Q4	2	NPN, 40 V, 350 mW, SOT–23	Vishay/LiteOn Power Semiconductor (Diodes Inc.)	MMBT2222A
MOSFET	Q3	1	N–Channel, 200 V, 4.8 A, 0.8 Ω, TO–252AA	International Rectifier	IRFR220
Resistor	R1, R3	2	Thick Film, 10.0 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF1002V
	R2	1	Thick Film, 5.11 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF5111V
	R4, R6	2	Thick Film, 1.1 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF1101V
	R5	1	Thick Film, 10.0 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF10R0V
	R7	1	Thick Film, 0.39 Ω, ±5%, 1/2 W, 2010	Panasonic	ERJ–12ZQJR39U
	R8	1	Thick Film, 82.5 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF8252V
	R9	1	Thick Film, 100 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF1000V
	R10	1	Thick Film, 20 kΩ, ±5%, 1 W, 2512	Panasonic	ERJ–1WYJ203U
	R11	1	Thick Film, 150 Ω, ±1%, 1/4 W, 1210	Panasonic	ERJ–14NF1500U
	R12	1	Thick Film, 5.1 Ω, ±5%, 1/4 W, 1210	Panasonic	ERJ–14YJ5R1U
	R13	1	Thick Film, 15 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF1502V
	R14	1	Thick Film, 47.5 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF47R5V
	R15	1	Thick Film, 619 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF6193V
	R16	1	Thick Film, 4.12 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF4121V
	R17	1	Thick Film, 6.81 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF6811V
	R18	1	Thick Film, 3.3 Ω, ±5%, 1/16 W, 0603	Panasonic	ERJ–3GSYJ3R3V
	R19	1	Thick Film, 39.2 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF3922V
	R20	1	Thick Film, 392 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF3920V
	R21	1	Thick Film, 49.9 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF49R9V
	R22	1	Thick Film, 3.92 kΩ, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF3921V
	R23	1	Thick Film, 0 Ω, ±5%, 1/16 W, 0603	Panasonic	ERJ–3GSY0R00V
	R24	1	Thick Film, 22.1 Ω, ±1%, 1/16 W, 0603	Panasonic	ERJ–3EKF22R1V
Transformer	T1	1	15 μH, RM5, 3F3	Pulse	PB0028
Integrated Circuit	U1	1	Economy primary side controller, MSOP–8	Texas Instruments	UCC3809P–2*
	Z1	1	Low voltage adjustable precision shunt regulator, 1.25 V, SOT–23–5	Texas Instruments	TLV431ACDBVR*
Terminal pin	J1, J2, J3, J4, J5	5	Terminal pin	Mill–Max	3156–2–00–01–00–00–08–0
	–	1	PCB, FR4, 4-Layer, 1 oz, 2.75””(L) x 1.00””(W) x 0.063””(T)”		SLUP052

NOTE: * Equivalent substitution not recommended



NOTE: High-Voltage component. See EVM Warning and Restrictions at the back of this document.
NOTE: High-Temperature component. See EVM Warning and Restrictions at the back of this document.

Figure 1. Flyback Converter Utilizing the UCC3809 Economy Primary-Side Controller.

2 Description

A brief description of the circuit elements follows:

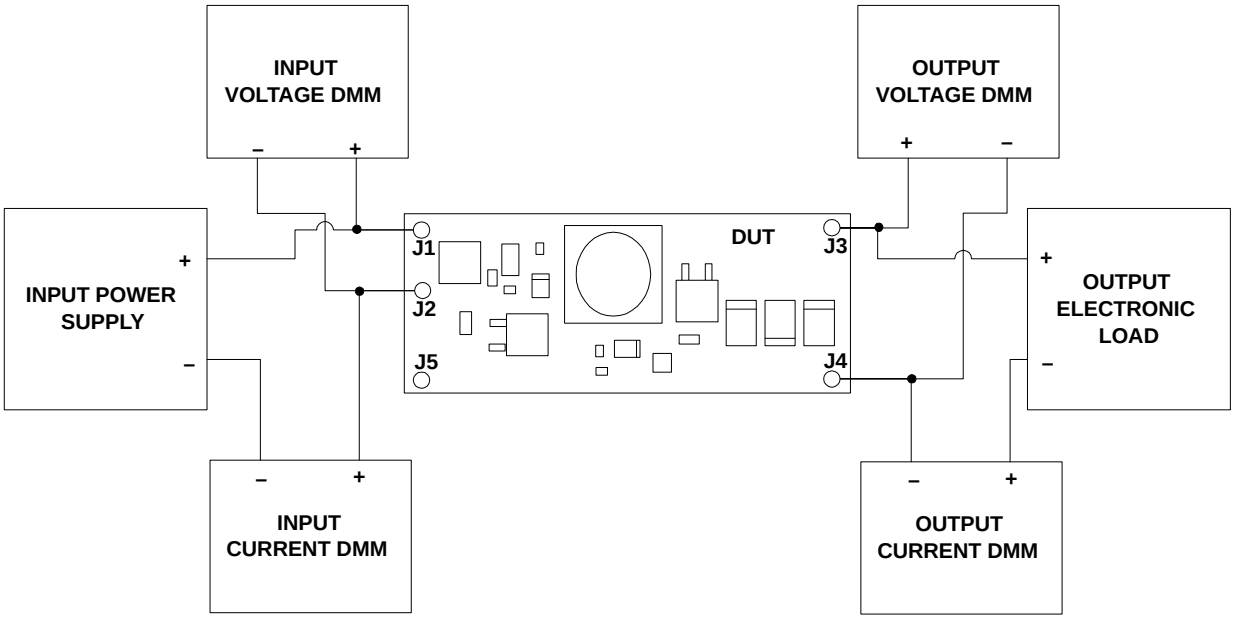
- Transformer (a.k.a. flyback inductor) T1, transistor Q3, Schottky diode D3, input capacitor C18, and output capacitors C10 through C12 form the power stage of the converter. Power resistor R7 senses the primary-switch current and converts this current into a voltage to be sensed by the primary-side controller feed-back comparator.
- Capacitor C14 filters out high-frequency noise on the output bus directly at the output diode.
- Resistor R11 and capacitor C7, along with resistor R10, capacitor C6, and diode D2 make up the voltage snubber and clamp, respectively, for the primary side; likewise, resistor R12 and capacitor C8 provide secondary-side snubbing.
- Resistor R8 supplies the start-up current to the primary-side controller, UCC3809. Operating current is provided through the self-biasing (sometimes referred to as bootstrap) components D4 and C5.
- Resistor R6 and capacitor C1 filter out leading-edge current spikes which are caused by the reverse recovery of the rectifier, equivalent capacitive loading on the secondary, and parasitic circuit inductances. C1 should be returned directly to the IC ground.
- Resistor R24 and capacitor C13 provide leading-edge blanking to the voltage spike resulting from the leakage inductance of the transformer. Failure to add these components would result in D4 and C5 peak rectifying to this spike voltage.
- The primary-side controller functions are supported by external circuitry such as resistors R3 and R1, combined with C9, which provide a charge and discharge path for the internal oscillator, setting the switching frequency for the converter.
- Transistor Q4, resistors R20, and R22, along with dc voltage-blocking capacitor C15 provide slope compensation.
- Capacitor C3 programs the soft-start time and transistor Q2, biased from the resistor divider R2 and R4, is used to form an external shutdown.
- Capacitors C2 and C4 are decoupling capacitors which should always be good quality low ESR/ESL type capacitors placed as close to the IC pins as possible and returned directly to the IC ground reference.
- The gate-drive circuitry is composed of gate-drive resistor R5 (necessary for damping any oscillations resulting from the input capacitance of Q3 and any parasitic stray inductance) and pull-down resistor R13 (this resistor assures Q3 stays off in the event that U1 is removed from the circuit for any reason). Resistor R18 and diode D1 are used to accelerate the turnoff time of Q3, while still limiting the gate current during switch turnoff, thereby protecting the output stage of U1.
- The voltage-sense feedback loop is comprised of resistor-divider network R21, R17, and R16 (actually R21 provides a series 50-Ω injection point for small-signal control-loop analysis). Feedback components R15 and C16 provide the necessary gain and pole to stabilize the control loop, while R14 and R19 provide bias current to optocoupler Q1, and secondary-side error amplifier and voltage reference Z1. Capacitor C17 helps to filter noise that may corrupt the exposed base terminal of the optocoupler while R9 provides the proper offset for the voltage-feedback signal to be summed with the current-sense signal and the slope compensation at the FB pin of the UCC3809.

3 Theory of Operation

When Q3 is turned on, T1 primary current increases linearly from zero. During this time, energy is stored in the gap of the transformer while the load current is supplied by the output-capacitor bank, C10 through C12, as well as C14. When this primary current has increased to a value at which the voltage across R7, summed with the voltage sense and slope compensation, exceeds the FB threshold voltage of one volt, Q3 is turned off. The stored energy in T1 is now transferred to the secondary side, forward biasing D3, and also replenishing the charge on the output-capacitor bank.

Peak current mode control responds immediately to line voltage changes and also provides over current protection to the switching device. A discontinuous current-mode controlled flyback converter does not have a right half plane zero and does not have the subharmonic-loop instability problems usually seen in the large duty–ratio continuous–inductor current topologies. Although this converter does have peak-current limit, and survives a momentary short circuit on the output, an extended short circuit results in power supply failure.

4 UCC3809EVM–052 Operating Instructions



NOTES: 1. Source power should be able to supply a minimum of 0.5 A at 75 V.
NOTES: 2 Load should be able to sink up to 3 A with adequate power rating. Resistive loads with adequate ratings may be used.

Figure 2. Connection Diagram for the UCC3809EVM–052

1. Connect a dc power supply, capable of supplying up to 75 V at 0.5 A, to terminals J1 and J2. Note that the positive terminal is connected to J1, the negative terminal is connected to J2. The power supply should be set to its minimum-output voltage level and current limited to 0.5 A.
2. Connect the load to J3 and J4. This load should be capable of handling 3 A at 3.3 V. The positive terminal is connected to J3, the negative terminal is connected to J4.

   The output load should never exceed 3 A.

   Do not short the output terminals, power converter failure results.
3. Turn on the electronic load.
4. Turn on the input power supply. Starting with the input dc power supply at its minimum setting, slowly increase the voltage to the EVM operating range, 32 V to 75 V. The converter actually begins regulating when the dc supply is at approximately 24 V.

   The input voltage to the EVM should be no greater than 75 V at any time.

5 Determine the Maximum on Time (D_{MAX}) for the Primary Switch

Maximum duty cycle occurs at minimum input voltage and maximum load. Programming D_{MAX} clamps the maximum on–time of the switch. This maximum on–time should incorporate enough of a margin so that control is well maintained at minimum input voltage. The UCC3809 has a programmable maximum duty-cycle clamp up to 70%. Core saturation is prevented and discontinuous mode is ensured by establishing a dead time, usually approximately 20% of the switching period. For this converter it is assumed D_{MAX} is 40% and the clamp is set at 50% Setting a maximum duty cycle protects the magnetics from saturating during startup and brown outs. Selecting RT1 equal to RT2 results in 50% duty cycle, the value of CT is selected to satisfy the following equation:

$$\frac{1}{f_{SW} \times 0.74 \times (RT1 + RT2)} - 27\ pF = 141.919\ pF$$

where f_{SW} is the desired switching frequency of the converter. A standard value of 150 pF results in a measured switching frequency of 380 kHz.

6 Determine the Turns Ratio of the Flyback Inductor

By equating the volt–second on product, which is equal to the minimum input voltage, $V_{IN(min)}$, minus the drain to source forward voltage drop, V_{DS}, multiplied by the maximum on–time, $t_{ON(max)} = D_{MAX}T$, to the reset volt-second product, equal to the output voltage, V_{OUT}, added to the forward voltage drop of the output diode, V_F, multiplied by the reset time, $t_{RESET} = (0.8–D_{MAX})T$, the core is prevented from drifting up or down its hysteresis loop. The turns ratio of the transformer can be calculated by using this steady state volt–second approach:

$$n = \frac{\left(V_{IN(min)} - V_{DS}\right) \times D_{MAX} \times T}{\left(V_{OUT} + V_F\right) \times \left(0.8 - D_{MAX}\right) \times T}$$

This application utilizes a turns ratio of 7, the primary consists of 14 turns while the secondary has 2 turns.

7 Primary Inductance

Magnetic design is a major part of any switch-mode power supply. The flyback transformer is actually a coupled inductor, acting as an energy storage unit as well as performing the usual transformer functions. Crucial considerations include primary inductance, working flux density swing, gap length, winding scheme and wire diameter. The primary inductance, L_P, for a discontinuous mode flyback converter can be calculated according to the following relationship:

$$L_P = \frac{n \times \left[\left(V_{IN(min)} - V_{DS}\right) \times t_{ON(max)}\right]^2}{2 \times T \times V_{OUT} \times I_{OUT}}$$

where n is the assumed efficiency of the converter and I_{OUT} is the output current. This converter design requires a primary inductance of approximately 15 μH, typical. With a required output power of 10W and assuming 70% efficiency, the core should be sized to safely handle at least 14 W. The ferrite core should have high saturation, low residual flux density, and low losses. An RM5 core of 3F3 material proved to be suitable for this application. Hysteresis loss is minimized in this design by restricting the flux density to 800 gauss. Selecting a core material with high permeability is not crucial because the energy stored in the flyback transformer is actually stored in the air gap. Gapping the core also reduces the residual flux density. The size of the air gap is calculated by applying the following equation:

$$GAP = \frac{\mu_O \times \mu_R \times N_P{}^2 \times A_E \times 10^{-2}}{L_P}$$

where μ_0 is the permeability of free space equal to $4\pi \times 10^{-7}$ H/m and μ_R is the relative permeability of free space, which is air, equal to 1. A_E is the effective core area measured in cm^2 .

8 Soft Start

Soft start is used to reduce transformer and output capacitor stress and to reduce the surge on the input circuits when the converter action starts. The considerable capacitance on the output lines should be charged slowly so as not to reflect an excessive transient. Also, a wide initial pulse could result in saturation of the core, and voltage overshoot on the output results if the inductor current is allowed to rise to a high value during start-up. To program this rise time, referred to as t_{SS}, a 10-nF capacitor is chosen so that the 9.1-μA of maximum internal-charging current from the SS pin of the UCC3809 delays complete start-up for approximately 2 ms (800 cycles). When the voltage on this capacitor charges from 1 to 2 volts, the duty cycle is gradually increased from narrow pulses to normal operating conditions. If pulled below 0.5 V the output driver is inhibited and the IC reference is pulled low. The controller goes into its low start-up current of less than 100 μA. A simple NPN transistor and two resistors allow the user to externally control this feature by application of a 5-V signal to J5 as shown in Figure 1.

9 Self-Biasing Winding

At first power up, the UCC3809 has a very low start-up current of approximately 100-μA. This current can be supplied by a start-up resistor from the converter input line. But constant IC operating current, as high as 1.25 mA at 400 kHz at 25°C, no load, in addition to the average gate-drive current from this source would be impractical for efficiency reasons. Therefore, a bias winding is added to the Flyback inductor. This winding is essentially another secondary output but its return is common to the primary side. This winding must maintain voltage above the undervoltage lockout (UVLO) threshold of the UCC3809 while supplying the IC with its operating current as well as the average gate-drive current, as mentioned above. The turns ratio for the bias winding is determined using the same procedure as the main secondary, explained previously, except that V_{OUT} is replaced with VDD. A small leading edge blanking RC circuit is placed at the output of the transformer to filter out the voltage spike due to leakage inductance of the transformer. A 100-V Schottky is used because the device's working peak reverse voltage rating must be able to handle the reflected primary voltage added to the reflected main output voltage along with the VDD voltage that it is supplying. The bias winding capacitor must be able to maintain the IC input voltage above the UVLO threshold, V_{UVLO}, while supplying both the operating current for the UCC3809, I_{VDD}, and the average gate-drive current, $I_{GATE(avg)}$. A minimum value for C_{BOOT} can be calculated as:

$$C_{BOOT} = \frac{\left(I_{GATE(avg)} + I_{VDD}\right) \times t_{SS}}{\left(VDD - V_{UVLO}\right)}$$

10 Selection of the Switching Element

The MOSFET switch is selected to meet the drain to source voltage stress resulting from the maximum input voltage, $V_{IN(max)}$, the reflected secondary voltages, equal to the output voltage, V_{OUT}, plus the output diode forward voltage drop, V_F, and the voltage spike due to the leakage inductance, assumed to be 30% of the input voltage:

$$V_{DS(stress)} = \left[\left(V_{IN(max)}\right) + N \times \left(V_{OUT} + V_F\right)\right] + 0.3 \times V_{IN(max)}$$

The switch must be able to conduct the repetitive peak-primary current as determined by:

$$I_{PEAK(primary)} = \frac{\left(V_{IN(min)} - V_{DS}\right) \times t_{ON(max)}}{L_P}$$

The primary-current waveform of a discontinuous mode flyback converter is triangular in shape, therefore, its root mean square (rms) current is calculated by:

$$I_{PRMS} = \frac{I_{PEAK(primary)}}{\sqrt{3}} \times \sqrt{\frac{t_{ON(max)}}{T}}$$

The chosen device should also have a low $R_{DS(on)}$ value because the conduction losses of the device are proportional to the square of the primary rms current through the device. Selection of a device that has a peak current rating of at least three times the peak-primary current usually ensures acceptably low conduction losses.

$$P_{CONDUCTION} = I_{PRMS}^{2} \times R_{DS(on)}$$

Switching losses are the result of overlapping drain current and source voltage at turn off. The drain voltage begins to rise only after the *Miller* capacitor of the device begins to discharge. This discharging time is a function of the external gate resistance, R_{GATE}, and the gate to drain *Miller* charge, Q_{GD}, as shown in the following equation:

$$t_{MILLER} = \frac{Q_{GD} \times R_{GATE}}{VDD - V_{TH}}$$

where V_{TH} is the turn on threshold voltage of the gate.

The power loss due to the external capacitance of the MOSFET also contributes to the total switching losses, which can be calculated as shown:

$$P_{SWITCHING} = f_{SW} \times \left[\frac{C_{OSS} \times V_{DS(stress)}^{2}}{2} + V_{DS(stress)} \times I_{PEAK(primary)} \times t_{MILLER}\right]$$

During turn on there is no overlap of drain voltage and current because there is no current in a discontinuous current-mode converter at turn on. Minimal losses also occur during the off-time of the FET due to the leakage current:

$$P_{OFF(time)} = \left(1 - D_{MAX}\right) \times I_{LEAK} \times V_{DS(stress)}$$

11 Current Sense

The ground referenced sense resistor is selected such that the maximum peak-primary current trips the 1-V FB pin threshold when this current is 10% higher than its normal operating peak value at the minimum input voltage. This limits the peak-primary current in the event of an output short circuit. This resistor must have a power rating to meet the $I_{RMS}^{2}R$ requirement, where I_{RMS} is the root mean square (rms) primary current. Because this resistor defines the maximum peak-primary current, the input energy to the transformer is defined and equal to $(1/2)L_P I_{PEAK}^{2}$. This defined energy in a fixed frequency discontinuous-mode flyback results in a fixed output power. The advantage of current-mode control is that the output voltage is held constant despite changes in the input voltage because the peak-primary current remains constant; the slope of this inductor current and its pulse width are adjusted. Leading edge spikes or noise are caused by the reverse recovery of the rectifier, equivalent capacitive loading on the secondary, and parasitic circuit inductances. A small low pass RC filter is added to the current-sense signal to filter out these spikes so the comparator does not assume an overload condition is present during switch turn on. To avoid excessive phase lag on the current-sense signal, the low pass filter corner frequency is selected to be at least a decade above the switching frequency.

12 Gate Drive

At 15 volts gate to source voltage the IRFR220 has a total gate charge of approximately 14 nC. The UCC3809 is capable of sourcing 400-mA of peak-drive current which would result in a turn-on time of 35 ns. To limit the peak current through the IC, an external resistor is placed between the totem-pole output of the IC and the gate of the MOSFET. The minimum value of this resistor is determined by:

$$R_{GATE} = \frac{VDD(min) - V_{SAT}}{I_{GATE(peak)}}$$

This small-series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance. A pulldown resistor is added to the gate drive to insure the MOSFET gate does not get charged to its turnon threshold during device start up. Adding a fast-switching diode and smaller value resistor in parallel with the gate resistor helps to control the current the IC needs to sink during turnoff and protects the output stage of the device. These components also help to reduce turnoff losses which tend to dominate the switching losses in discontinuous current-mode (DCM) converters.

13 Output Diode

The output diode in a flyback converter is subject to large peak and rms current stresses. The 10-W flyback converter described here has measured peak-secondary currents as high as 18 A with an rms value of approximately 7 A. Schottky diodes are recommended because of their low-forward voltage drop and the virtual absence of minority carrier reverse recovery. The secondary-side Schottky rectifier was selected to meet the working peak-reverse voltage, the peak repetitive-forward current, and the average forward current of the application. The working peak-reverse voltage, V_{REV}, or blocking voltage, is calculated according to the following equation:

$$V_{REV} = \left(V_{IN(max)} + V_{RDS(on)}\right) \times \frac{1}{N} + \left(V_{OUT}\right)$$

The reflected peak-primary current constitutes the peak repetitive-forward current through the diode. Because all current to the output capacitor and load must flow through the diode, the average-forward diode current is equal to the steady-state load current. Power loss in the Schottky is the summation of the conduction losses and reverse leakage losses. Conduction losses are calculated using the forward voltage drop across the diode and the average-forward current. Reverse leakage losses are dependent upon the reverse-leakage current, the blocking voltage, and the on time of the FET.

14 Output and Input Capacitors

Output capacitors are selected based upon their capacitance value, equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitor ripple current rating. The capacitance value controls the peak to peak output ripple voltage at the switching frequency. Assuming a linear decay of the capacitor voltage during the off time, during which the capacitor must supply the load current, the minimum value of the output capacitor may be calculated as follows:

$$C_{OUT} = \frac{\left(T - t_{ON(max)}\right) \times I_{OUT}}{V_{RIPPLE}}$$

where V_{RIPPLE} is the acceptable peak-to-peak output-voltage ripple. Unfortunately there are practical limitations to how low a single stage output filter can reduce the ripple voltage and sometimes an extra LC filter stage is necessary. This second-stage filter would also reduce the output high-frequency noise. Parasitic resistance and inductance in the output capacitors tends to make the ripple voltage much greater than expected based upon the above equation. Using capacitors with the lowest possible ESR and ESL helps reduce the high-frequency ripple. The rms ripple current that the output capacitors experience is not the same as the secondary-side rms output current; it is the ac portion of it. The secondary-side rms current is in the shape of a clipped sawtooth, or trapezoid, where as the output capacitor's current waveform is in the shape of right triangle. Therefore, the typical capacitor ripple current rating the output capacitors must meet is equal to:

$$I_{RMS(cout)} = I_{PEAK(sec)} \times \sqrt{\left(\frac{t_{RESET}}{T}\right)\left[\frac{4 - 3 \times \left(\frac{t_{RESET}}{T}\right)}{12}\right]}$$

where $I_{PEAK(sec)}$ is the peak-secondary current, and t_{RESET} is equal to the off time of the switch. The same selection criteria is used for the input capacitor, keeping in mind these capacitors must also be rated to handle the maximum-input voltage.

15 Loop Compensation

The UCC3809 is a primary-side controller for use in isolated converters; therefore it does not contain an internal error amplifier. The TLV431, a low-voltage adjustable-precision shunt regulator, is used on the secondary side for the feedback control loop. This regulator is ideal for low voltage supplies because the output voltage can be set to any value between its reference of 1.24 V and 6 V while operating from a lower voltage than the standard TL431.

The output voltage is resistively divided and compared to the TLV431's 1.24V reference voltage. When the resistively divided-converter output voltage rises above this threshold, the TLV431 drives the optocoupler diode on which, in turn, drives the FB pin on the UCC3809 to its 1-V threshold, turning off the output driver. The reverse happens when the resistively divided-output voltage falls below the 1.24-V TLV431 reference voltage.

The feedback loop needs to be closed around the error amplifier by adding a compensation network. The network components are selected so as to give the converter good dynamic response, acceptable line and load regulation, and stability resulting from optimum closed-loop bandwidth. Before calculating the error-amplifier compensation, the control to output gain, or transfer characteristic, along with the power-stage poles and zeros must be determined. This is easily done using Lloyd Dixon's *Closing the Feedback Loop* available in the Unitrode Power Supply Design Seminar SEM–700. The output capacitor, because of its parasitic ESR, contributes a zero in the frequency response at:

$$F_{ESR(zero)} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

where C_{OUT} is the total capacitance of the output capacitor bank and ESR is the parallel combination of the output capacitor's equivalent series resistance. The power stage contributes a pole located at:

$$F_{PWRstg(pole)} = \frac{2}{2 \times \pi \times R_{OUT} \times C_{OUT}}$$

Note that this pole is load dependent. The control to output gain is calculated by the following equation:

$$G = K \times \sqrt{\frac{R_{OUT} \times \left(L_{SEC} \times f_{SW}\right)}{2}}$$

$$I_P = \frac{2 \times I_{SC(sec)}}{1 - D_{MAX}}$$

$$K = \frac{I_P}{V_C}$$

where R_{OUT} is the load, L_{SEC} is the primary inductance reflected to the secondary side, and $I_{SC(sec)}$ is the secondary-side short-circuit current, V_C is the reference voltage of the TLV431, or 1.24 V.

Once the gain and corner frequencies have been determined, a bode plot can be constructed of the pre-compensated converter. Sampling theory limits the maximum-crossover frequency to one half the switching frequency. Practicality limits it even further; the system is unstable if the crossover frequency is more than $f_{SW}/2\pi D_{MAX}$. For this design, the crossover frequency was set at approximately 1 kHz. The error amplifier requires 38-dB of gain at this frequency. A pole is also needed to cancel the ESR zero. This pole is added a decade below the corner frequency of the ESR zero, resulting in an increase in low-frequency gain and adding 45 degrees of phase margin. The error-amplifier compensation is determined using the following equation:

$$EA_{GAIN} = 20 \times \log\left(\frac{R_F}{R_I}\right)$$

where R_I is equal to R21 + R17, referring to Figure 1, the feedback resistor, R_F, shown as R15 in Figure 1, is easily determined. The feedback capacitor (shown as C16 on the schematic), which, when combined with the feedback resistor adds the ESR canceling pole, is calculated using:

$$C_F = \frac{1}{2 \times \pi \times F_P \times R_F}$$

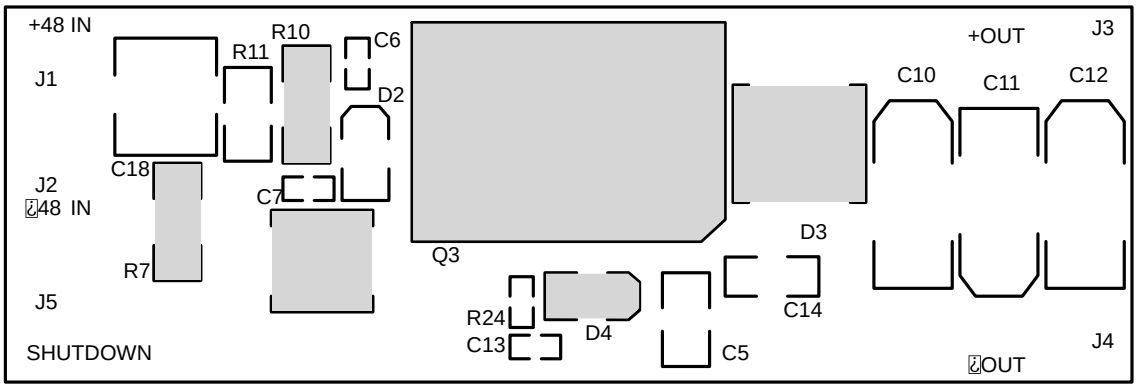
where F_P is set at one-tenth $F_{ESR\ (zero)}$.

The resultant phase margin is approximately 100 degrees.

16 Slope Compensation

All peak current-mode converters benefit from slope compensation, which is added to the current-sense signal, to cancel the error introduced by sensing peak current instead of average current. The amount of inductor down slope added to the FB pin was designed to be approximately 0.5 and the emitter follower configuration was used. The step-by-step calculations are beyond the scope of this design note. Application Note U–111 *(TI Literature Number SLUA111)* is an excellent reference for slope compensation design techniques.

17 Silkscreen



NOTE: High–temperature component. See EVM Warnings and Restrictions at the back of this document.

18 Conclusion

This design procedure addresses the major considerations and calculations used in the design of a 10-W discontinuous-mode flyback converter. These include maximum duty cycle, inductor turns ratio, core selection, primary inductance, gate drive, and current sensing. Major component selections such as switching element, output diode, and output capacitors were also discussed as well as control loop compensation. This converter is available as an evaluation module from Texas Instruments.

19 References

Bill Andreycak, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, Unitrode Application Note U–137, *(TI Literature Number SLUA156),* Unitrode Applications Handbook IC#1051, 1997.

Bill Andreycak, *Practical Considerations in Current Mode Power Supplies*, Unitrode Application Note U–111, *(TI Literature Number SLUA111),* Unitrode Applications Handbook IC#1051, 1997.

Keith Billings, *Switchmode Power Supply Handbook*, McGraw–Hill, Inc.,1989.

Lloyd Dixon, Jr., *Closing the Feedback Loop*, Unitrode Power Supply Design Seminar Manual SEM–1100, 1996.

DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 32.0 V to 75.0 V, and the output voltage range of 3.218 V to 3.383 V, and the load current range of 0.0 A to 3.0 A.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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