Application Report
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Design for Integrated Photo Flash Charger and IGBT Driver

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ABSTRACT

The Texas Instruments TPS65552A offers a complete solution for charging photo flash capacitors. It has an integrated power switch, an IGBT driver, and control logic block for photo flash applications. The TPS65552A controller requires only a few external components and gives fast charging times with high efficiency.

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1 Introduction

The TPS65552A series offers a complete solution for charging a photo flash capacitor from battery input and subsequently discharging the capacitor into a xenon flash tube. This device has an integrated power switch, an IGBT driver, and control logic blocks for charging applications. Compared with discrete solutions, this device significantly reduces the component count, shrinks the solution size, and eases design complexity. Additional advantages are fast charging time and high efficiency due to the optimized PWM control algorithm. The typical application circuit is shown in Figure 1.

Among the salient features of the TPS65552A are programmable peak primary current, adjustable output voltage, and a charge-complete status output.

- Programming the peak primary current is easy. The peak current can be set from 0.9 A to 1.8 A by using the I_PEAK pin of the TPS65552A. Setting the I_PEAK pin low sets the peak primary current to the minimum. Setting the I_PEAK pin to a logic high sets the primary current to the maximum. The peak primary current can be set to any value between the minimum and maximum by applying an analog voltage to the I_PEAK pin. Section 2 discusses programming the peak current in more detail.
- The target output voltage is set by the turn ratio of the transformer. The TPS65552A decides the target voltage by sensing the primary-side voltage ($V_{(SW)}$). It compares $V_{(SW)}$ to a threshold voltage (V_FULL) with an internal comparator U1 shown in Figure 1 and Figure 2.
- The XFULL pin goes low when the capacitor charging is completed. A designer can connect an LED or controller to this pin to signal when this charging is complete.

The TPS65552A offers three forms of protection. The TPS65552A uses MAX ON TIME, OVER VDS, and THERMAL shutdown. For example, the MAX ON TIME protection prevents the controller from trying to pull too much current from a low battery that cannot supply enough current and thus never reaches the target peak current. All three protection functions are covered in detail in Section 2.

The target application of TPS65552A is particularly well-suited for portable device applications like digital still cameras (DSC), digital video cameras (DVC), optical film cameras, mobile phones with camera, and PDAs with cameras.

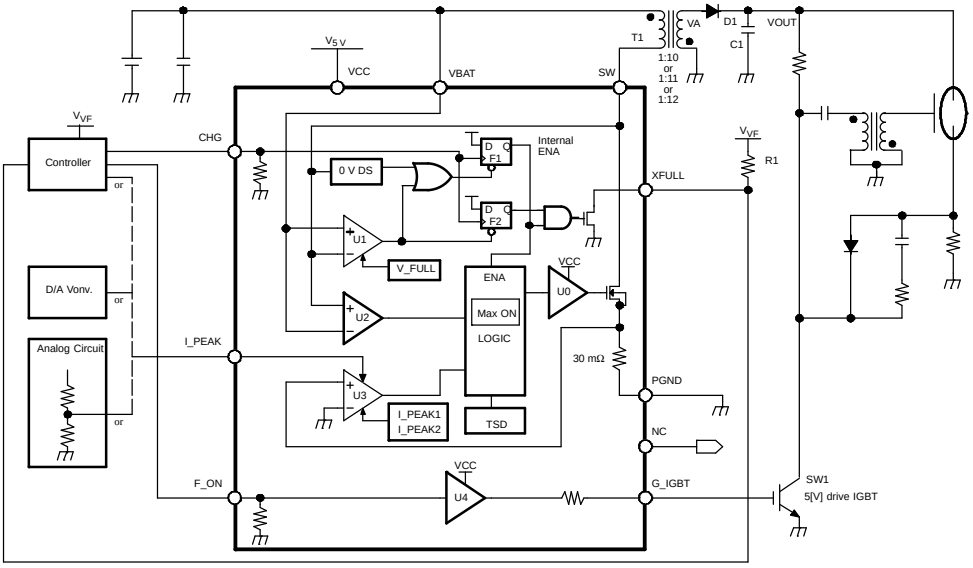

Figure 1. Typical Application Circuit

2 Operation

2.1 Basic Function

2.1.1 How to Start and Stop Charging

The TPS65552A has one internal enable-latch, F1, that holds the charge ON/OFF status of the device (see Figure 2). A rising edge on the CHG pin latches the internal latch on the ON state. Charging continues until one of the three following events occurs.

1. Forcing a STOP by setting the CHG pin to a logic low.
   - This manually stops the charging. By setting the CHG pin to low, the internal ENA function (see Figure 2) goes low and the internal FET switch turns off.
2. Automatic STOP by detecting the output voltage, VOUT, has reached the target value.
   - This is the standard stop function. U1 (see Figure 2) compares (VSW – VBAT) to V_FULL, which decides maximum primary-side voltage. The TPS65552A automatically stops charging when (VSW – VBAT) exceeds VFULL.
3. Protecting STOP due to OVDS protection.
   - This function protects TPS65552A from overvoltage at the SW pin when the internal FET switch is on. The internal FET is turned off if the voltage between the drain and the source of the FET exceeds the specified OVDS voltage of 1.2 V. Internally, exceeding OVDS makes F1 reset, forcing ENA to go low and switching the internal FET off.

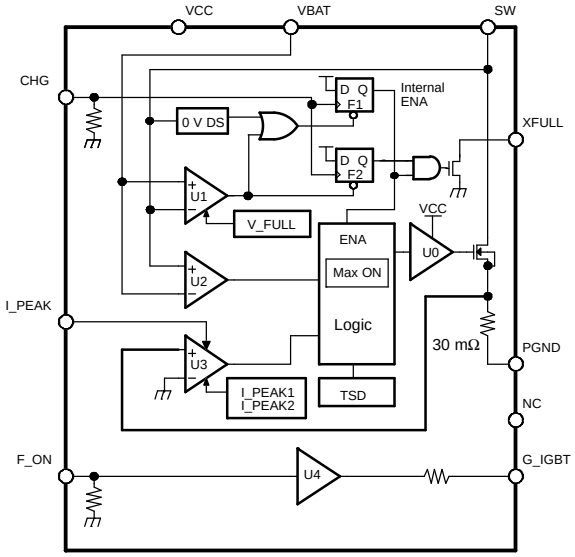

Figure 2. Block Diagram

2.1.2 Principles of Charging

The TPS65552A application circuit is based on a flyback transformer. The internal FET switch turns on, allowing current to flow into the primary of the transformer and thus store energy. The energy stored in the primary is transferred to the secondary when the switch turns off. Current flows in the secondary to the output capacitor (C1 in Figure 1) via the diode, D1.

The TPS65552A uses three comparators, U1, U2, and U3 in Figure 2 to determine the state of the internal FET switch. The descriptions of these comparators' functions follow.

- U1: Detects charge completion
- U2: Detects when zero energy remains in the transformer for the SW-ON timing. This is used to determine the timing when to switch the internal FET ON. U2 senses the kickback voltage at the SW pin. The internal switch is turned on when $V_{(SW)}$ is less than VBAT (Time 5 in Figure 3).
- U3: Detects the peak current for SW-OFF timing. U3 senses the primary-side current ($I_{(SW)}$) flowing through the internal FET switch from SW to PGND. SW turns OFF when $I_{(SW)}$ exceeds the target current set by the I_PEAK pin. (Time 2 in Figure 3)

A charge cycle starts when the CHG pin transitions from a logic low to high. The SW turns ON and $I_{(SW)}$ increases linearly through the primary of the flyback transformer (Time 1 to Time 2 in Figure 3). SW is turned off once $I_{(SW)}$ exceeds the target current (I_PEAK, Time 2 in Figure 3).

When SW turns OFF, the magnetic energy in the transformer starts discharging and the output voltage increases forward biases the output diode. As a result, the kickback voltage, now present at the SW pin, increases (Time 2 to Time 3 in Figure 3). When almost all the energy in the transformer is discharged, the transformer cannot maintain the secondary current; so, the secondary voltage and the kickback voltage both start to collapse (Time 3 in Figure 3). After rectification stops, the small energy left in the transformer is released via parasitic paths, and the kickback voltage reaches zero (Time 3 to Time 4 in Figure 4). During this period, comparator U2 senses when (VSW – VBAT) dips from VZERO (Time 5 in Figure 4) and makes SW turn ON for the next cycle.

The ON time on SW depends on I_PEAK. The ON time is calculated by Equation 1. This equation does not depend on output voltage.

$$T_{ON} = L_P \frac{I_{PEAK}}{V_{BAT}} \quad (1)$$

T_{ON}: ON time
L_P: Primary inductance
I_{PEAK}: Peak current
V_{BAT}: Battery voltage

On the other hand, the OFF time depends on output voltage for each cycle. This is because the current that flows on the secondary side depends on output voltage for each cycle . The OFF time is calculated by Equation 2.

$$T_{OFF} = N \times L_P \frac{I_{PEAK}}{V_{OUT}} \quad (2)$$

N: Turn ratio of transformer
V_{OUT}: Output voltage

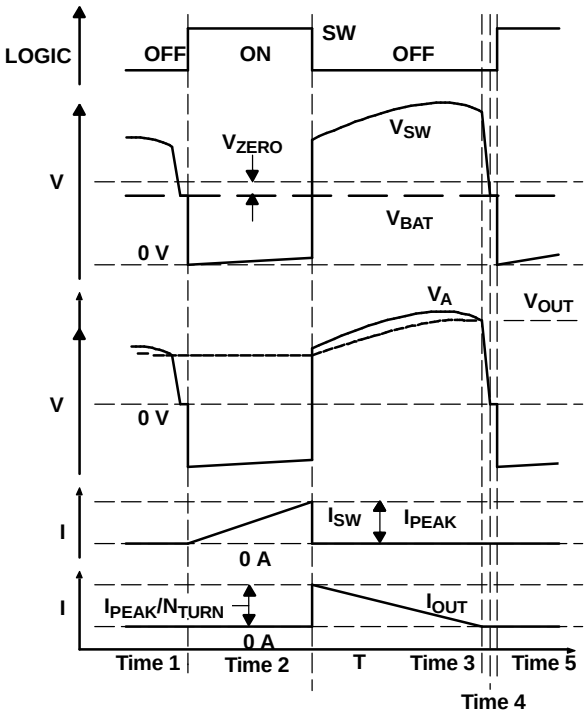

Figure 3. Timing Diagram for One Switch Cycle

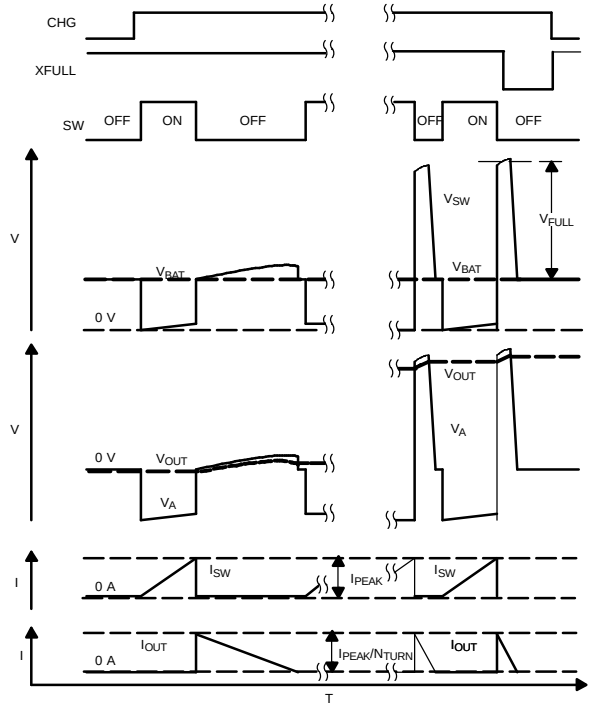

Figure 4. Timing Diagram for Beginning/Ending Cycles

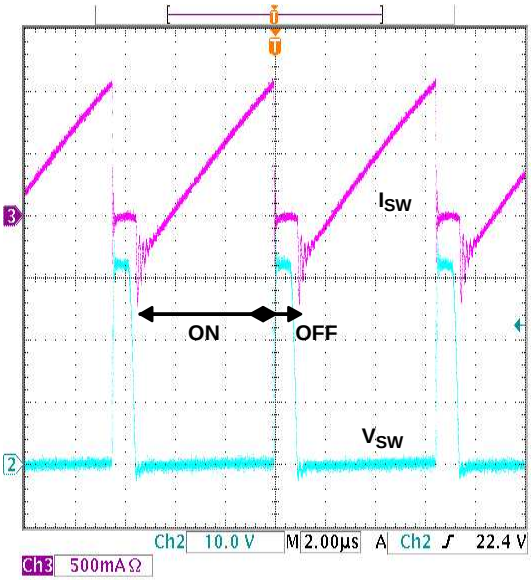

Figure 5. Waveform of Primary Side

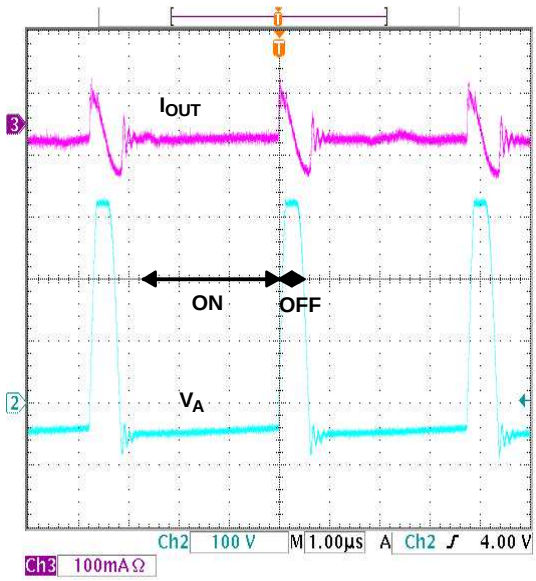

Figure 6. Waveform of Secondary Side

2.1.3 Programming Peak Current

The I_PEAK pin of the TPS65552A is used to program the peak primary current from 0.9 A to 1.8 A. The I_PEAK input is treated as a logic input when its voltage is below $V_{(PKL)}$ (0.6 V) and above $V_{(PKH)}$ (2.4 V). If the input is less than $V_{(PKL)}$ or more than $V_{(PKH)}$, the value of the peak current is equal to $I_{(PEAK1)}$ or $I_{(PEAK2)}$ as shown in Figure 2. $I_{(PEAK1)}$ and $I_{(PEAK2)}$ are specified in the data sheet. For voltages between $V_{(PKL)}$ and $V_{(PKH)}$, I_PEAK input is treated as analog input.

Equation 3 shows the relationship between peak current, I_PEAK , and I_PEAK pin voltage, V_PEAK.

$$I_{PEAK} = 0.472 \times V_{PEAK} + 0.668 \ (0.6\ V < Vpk < 2.4\ V) \quad (3)$$

Typical usages of the variable primary current follow.

- Changing I_PEAK depending on the battery capacity. For example, I_PEAK can be set high when the battery is fully charged and can supply the most current. As the battery discharges, I_PEAK can be decreased to reduce the amount of peak current the battery needs to supply.
- I_PEAK can be used for active power management. For example, I_PEAK can be reduced when the lens zoom motor is operating to avoid excessive current draw on the battery.

The voltage on the I_PEAK pin (V_PEAK) can be controlled in three ways as shown in Figure 1.

1. Use an external controller, and treat I_PEAK as the logic input pin. This method produces only the two values of peak current, $I_{(PEAK1)}$ and $I_{(PEAK2)}$, as shown in Figure 3
2. Use an external controller with a D/A converter to force V_PEAK to follow analog information such as battery voltage. The D/A converter can set the voltage on the I_PEAK pin between $V_{(PKL)}$ and $V_{(PKH)}$.
3. Use an analog circuit. The function is the same as using a D/A converter. The voltage on I_PEAK can be set using an analog circuit as shown in Figure 1.

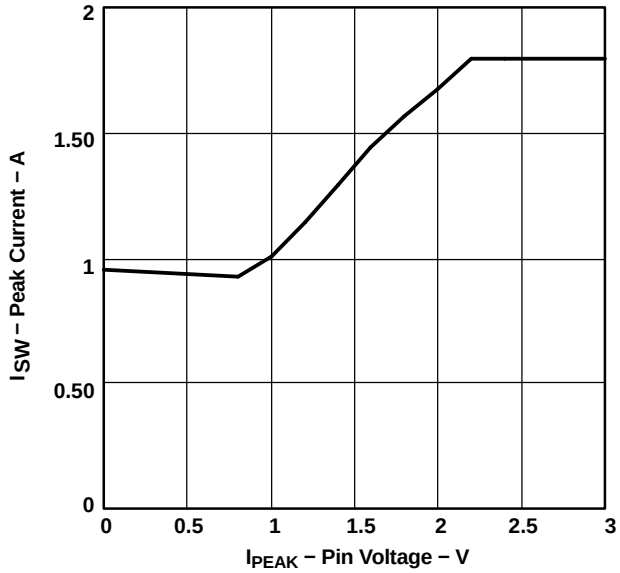

Figure 7. I_PEAK Pin Voltage Versus Peak Current

2.1.4 Propagation I_PEAK Delay

A 200-ns delay occurs between the detection of $I_{(SW)}$ exceeding the I_PEAK value to the turn off of SW. Therefore, there is a difference between the peak current detection value and the actual peak current value as shown in Figure 8. The difference depends on the primary-side inductance and the battery voltage (see Equation 4).

$$I\_PEAK = \frac{V_{BAT}}{L_P} T_{ON} \quad (4)$$

T_{ON}: ON time
L_P: Primary inductance
I_PEAK: Peak current on the primary side
V_{BAT}: Battery voltage

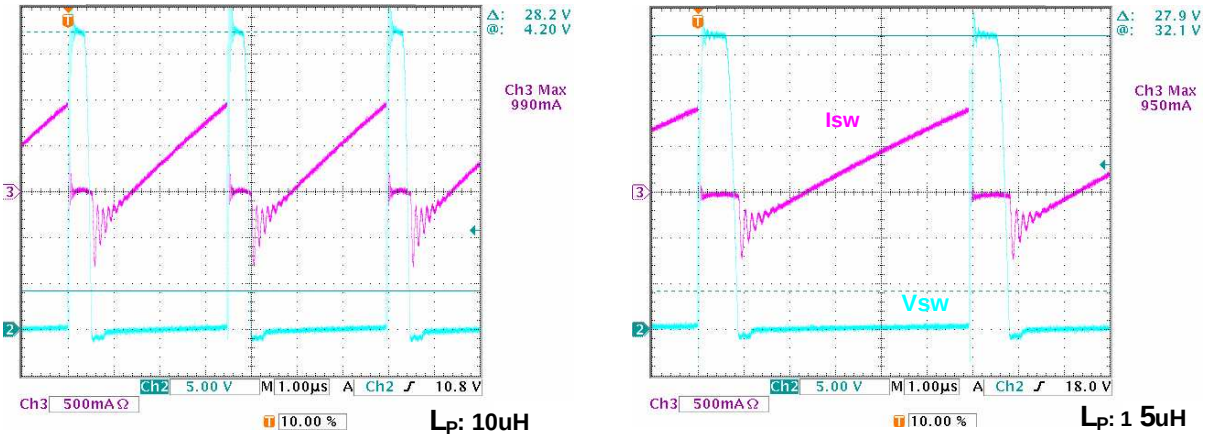

Figure 8. I_PEAK Delay Depends on Primary-Side Inductance

2.1.5 I_PEAK Temperature Characteristic

The TPS65552A has an I_PEAK temperature characteristic of approximately –3500 ppm/°C as shown in Figure 9.

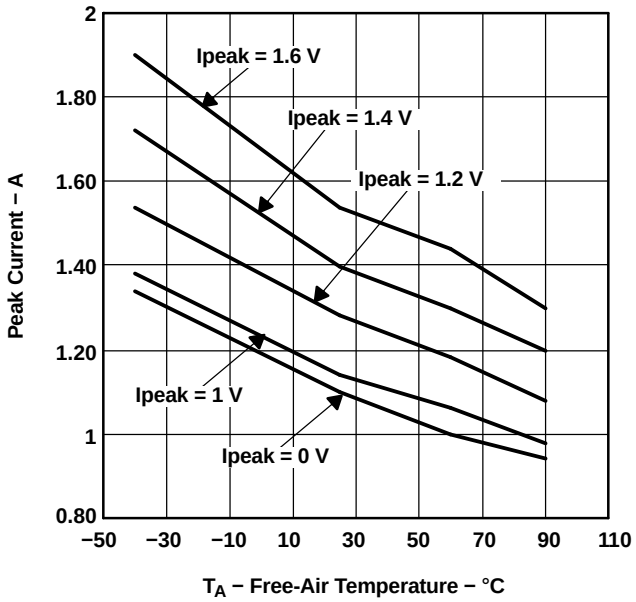

Figure 9. I_PEAK Temperature Characteristic

2.1.6 Charge Status Indicator

When the charging operation is complete, TPS65552A drives its charge-complete indicator, XFULL, low. To communicate to a controller that the charging is complete, connect the XFULL pin to the controller with a pullup resistor (see Figure 10). It is strongly recommended that the CHG pin be set to low immediately after the charging is complete. The XFULL output can also be used to drive an LED to provide visual indication of charging status. Simply connect the anode to the VCC and the cathode to XFULL (see Figure 11).

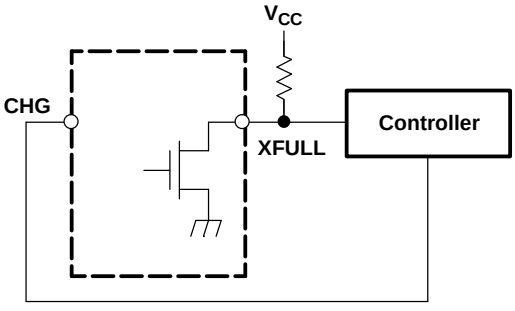

Figure 10. Connect Controller to XFULL

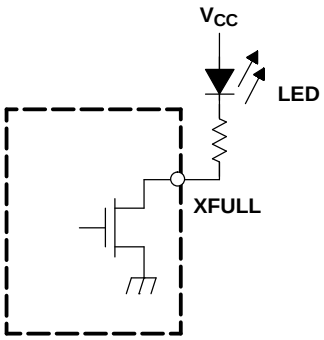

Figure 11. Connect LED to XFULL

The XFULL output is configured as an open-drain MOSFET as shown in Figure 2. The MOSFET has a low current sink capability. The current sink capacity of XFULL is shown in Figure 12 and Figure 13.

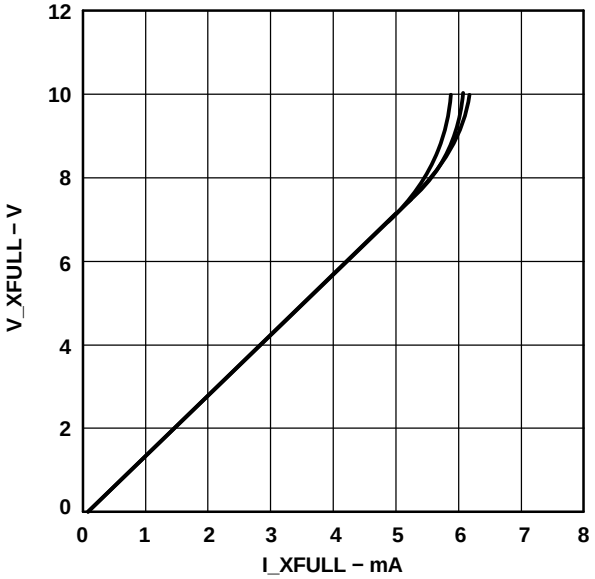

Figure 12. I_XFULL Versus V_FULL

2.1.7 Protections

The TPS65552A has three device protections, MAX ON TIME, OVER VDS SHUTDOWN, and THERMAL DISABLE.

1. MAX ON TIME
   - The MAX ON TIME protection guards against pulling current from an almost empty battery and never reaching the desired peak current. If the ON time of SW exceeds TMAX, then the TPS65552A turns OFF, regardless of the I_PEAK state. TMAX is designed to be typically 80 µs.
2. OVER VDS SHUTDOWN
   - This function protects against damage from large current on the primary side. The TPS65552A monitors the voltage across the internal FET and stops charging when the voltage exceeds the OVDS limit. The typical OVDS limit is 1.2 V.
3. THERMAL DISABLE
   - If the junction temperature of the TPS65552A exceeds 150°C, all functions stop as shown in Figure 13. If the level of the CHG pin is high, the device automatically restarts when its temperature has dropped below the threshold as shown in Figure 14.

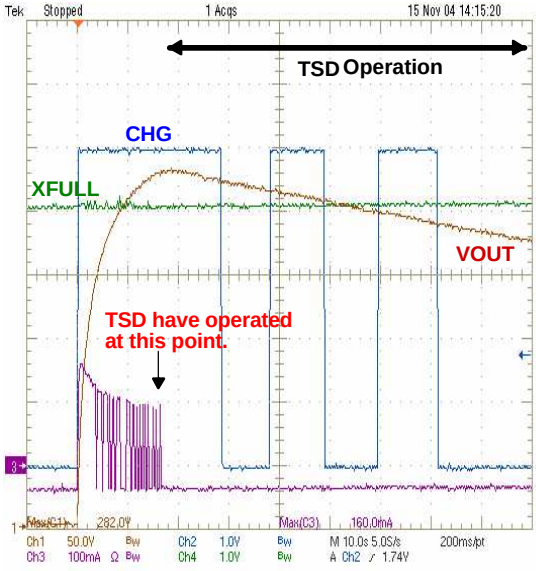

Figure 13. TSD Operation

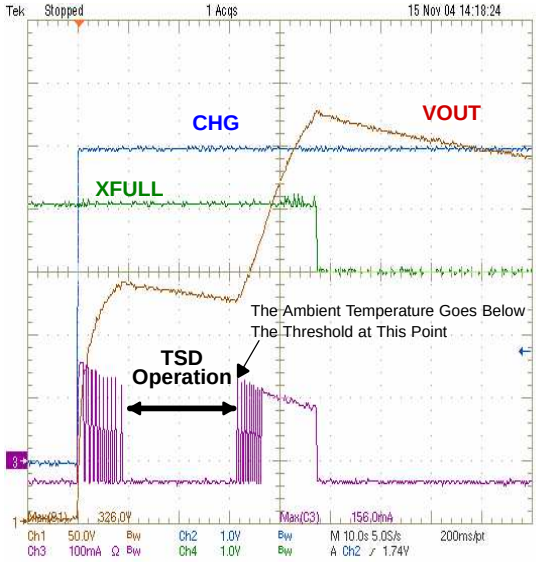

Figure 14. Charging Automatically Restarts When Ambient Temperature Reaches Threshold

2.1.8 IGBT Driver

TheTPS65552A has an integrated IGBT driver to drive the gate of an IGBT for a lamp trigger circuit. Once the photo flash capacitor is charged, the F_ON pin is switched from low to high to activate the lamp trigger. When the F_ON pin is switched to high to fire the photo flash, the CHG pin must remain at GND level. The TPS65552A may be damaged by an overvoltage on the SW pin if the CHG pin remains high during a flash (see Figure 15).

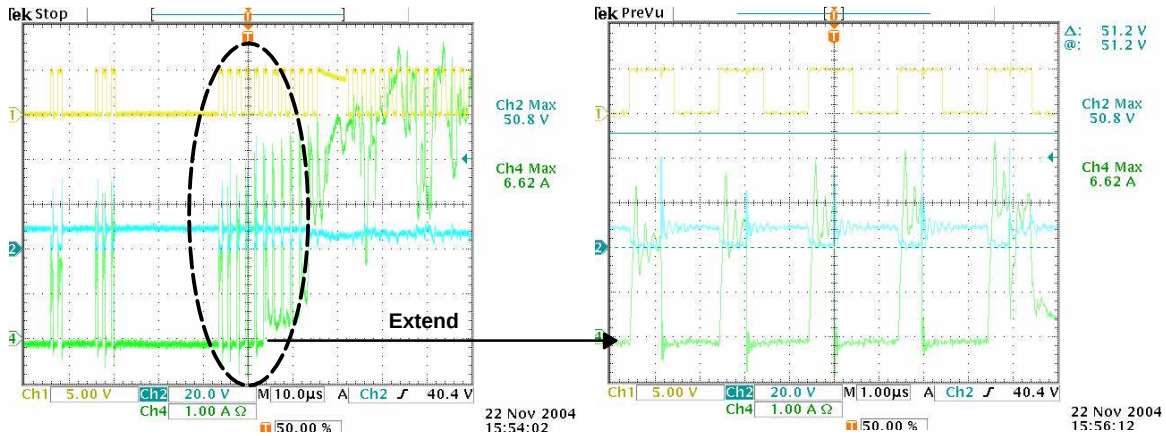

Figure 15. Overvoltage on SW Pin If CHG Pin Remains High During a Flash

2.2 Efficiency

Efficiency is defined as the output power divided by the input power as shown in Equation 5.

$$\eta = \frac{P_{OUT}}{P_{IN}} \qquad \begin{array}{l} P_{IN}\text{: Input power} \\ P_{OUT}\text{: Output power} \end{array} \tag{5}$$

The primary charging energy (P_P) charges the primary-side inductor. It is calculated as shown in Equation 6.

$$P_P = V_{BAT} \times I_{BATave} \qquad \begin{array}{l} V_{BAT}\text{: Battery voltage} \\ I_{BATave}\text{: Average battery current} \end{array} \tag{6}$$

The secondary discharging energy (P_S) is equal to the energy discharged by the photo flash capacitor. It is calculated as shown in Equation 7.

$$P_S = \frac{1}{2} C_P \times V_{OUT}^{2} \qquad \begin{array}{l} C_P\text{: Photo flash capacitor} \\ V_{OUT}\text{: Output voltage} \end{array} \tag{7}$$

Therefore, efficiency is calculated as shown in Equation 8.

$$\eta = \frac{P_S}{P_P} = \left(\frac{1}{2} C_P \times V_{OUT}^{2}\right) \Big/ V_{VBAT} \times I_{BATave} \times T \tag{8}$$

Equation 8 computes measured efficiency. However, efficiency also depends on parameters such as battery voltage, peak current, and reverse recovery time (t_{rr}) of diode. These can be checked by using a recommended evaluation board such as the TPS6555xEVM-097. The actual efficiency can be measured with these parameters: VCC, battery voltage, and I_PEAK pin voltage.

Figure 16, Figure 17, and Figure 18 show efficiencies at the power supply voltages of 4.5 V, 5 V, and 5.5 V, respectively.

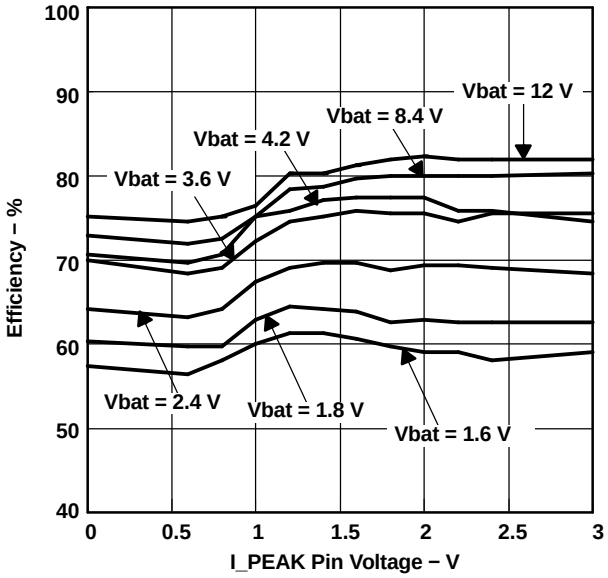

Figure 16. Efficiency at VCC 4.5 V

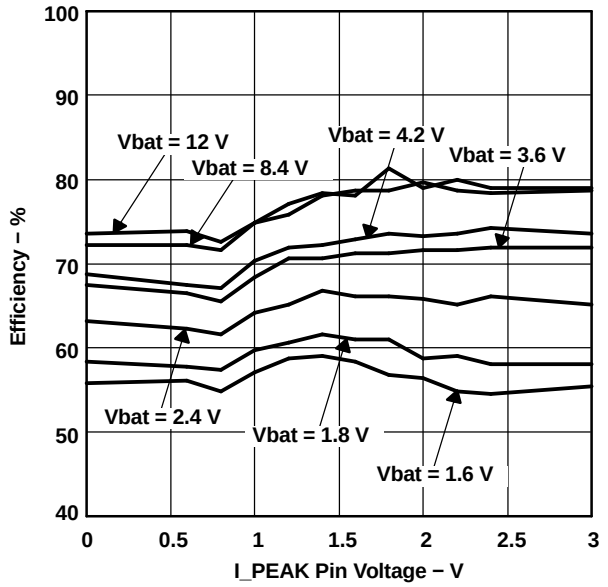

Figure 17. Efficiency at VCC 5 V

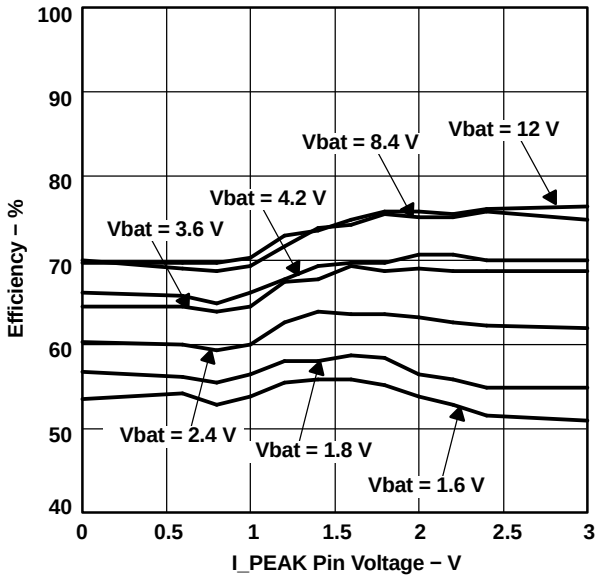

Figure 18. Efficiency at VCC 5.5 V

2.3 Charging Time

Charging time is one of the more important aspects of the photo flash charger. It depends on peak current, battery voltage, target voltage, and efficiency. The average input current from the battery depends on the peak current. The approximate calculation of charging time (T) is shown in Equation 9.

$$T = \left(\frac{1}{V_{BAT}} + \frac{N}{V_{OUT}}\right)\left[\frac{C\left(V^2_{OUT} - V'^2_{OUT}\right)}{\eta} \times I_{PEAK}\right] \quad (9)$$

Nturn: turn ratio of transformer
V_{OUT}: target output voltage
V'_{OUT}: target output voltage
η: efficiency
V_{BAT}: Battery voltage
I_{PEAK}: peak current

For a faster charge time, select a large peak current. To select a large peak current, set the I_PEAK pin voltage high. If possible, select 1.8 A. However, the average input current from the battery must take into consideration the current capability of the battery.

The charging time also depends on the external components used. For detailed information about the selection of transformers and diodes, see Section 3. The charging time is measured by these parameters: VCC, battery voltage, and I_PEAK pin voltage.

Figure 19, Figure 20, and Figure 21 show the charging times at the power supply voltages of 4.5 V, 5 V, and 5.5 V, respectively.

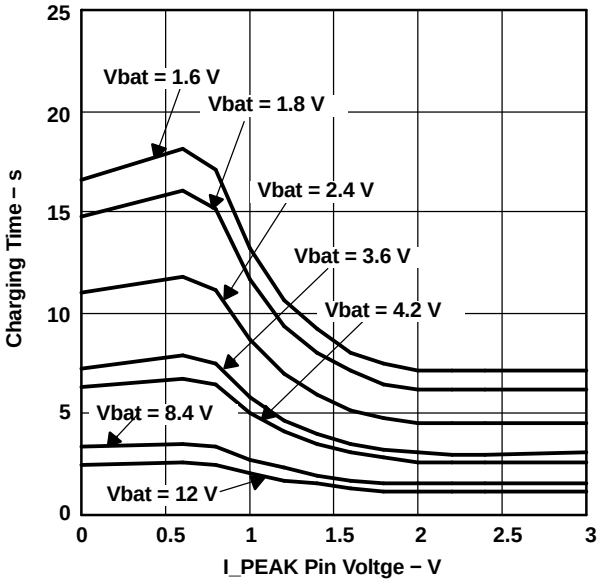

Figure 19. Charging Time at VCC 4.5 V

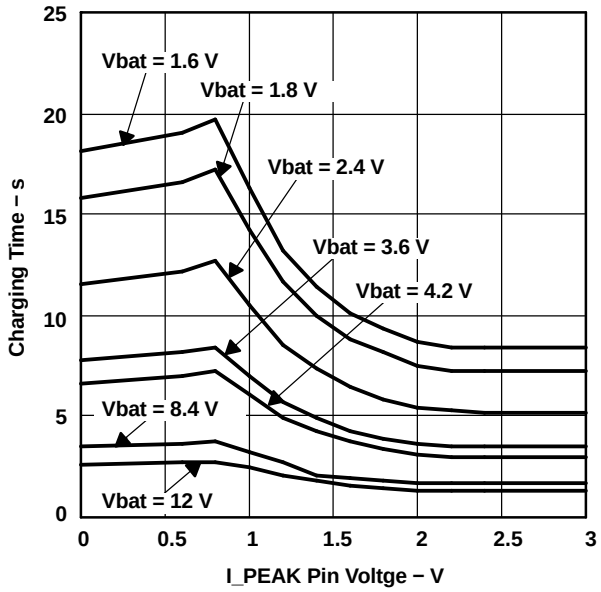

Figure 20. Charging Time at VCC 5 V

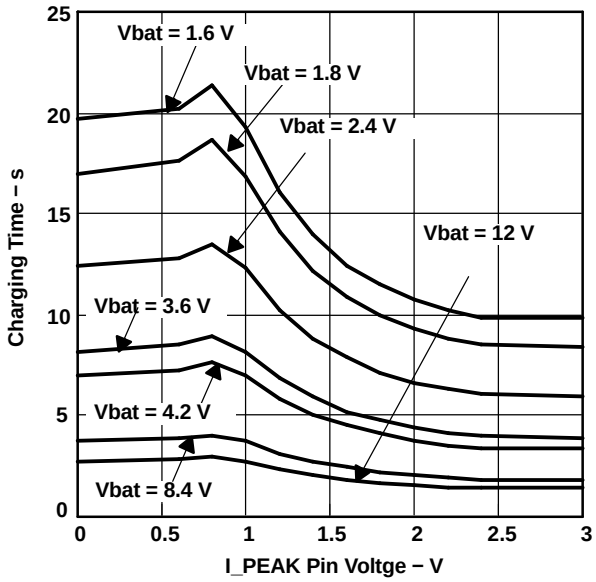

Figure 21. Charging Time at VCC 5.5 V

3 How to Select External Components

3.1 How to Select a Transformer

When designing a photo flash charger it is important to select the proper transformer. The following discussion provides useful information for transformer selection.

3.1.1 How to Determine Turn Ratio and Primary Inductance

First, select the target output voltage. After that, the turn ratio of transformer (N) is calculated by Equation 10. The recommended range of the turn ratio of the transformer is from 10 to 12.

$$N = \frac{V_{OUT} + V_D}{V\_FULL}$$

N: Turn ratio of transformer
V_{OUT}: Target output voltage
V_D: Forward diode voltage
V_FULL: Primary target voltage

(10)

Next, determine the peak-current value by considering how much voltage to input to the I_PEAK pin (see Section 2.1.3).

The transformer's primary inductance can be calculated using Equation 11 after choosing the peak current.

$$\frac{V_{OUT} \times 300 \times 10^{-}9}{N \times I_{PEAK}} \leq L_P \leq 600\ [\mu H]$$

L_P: Primary inductance
T_{on}: Switching ON time

(11)

The minimum peak current is defined by the minimum OFF time, and the maximum peak current is defined by MAX ON TIME protection. The recommended range is from 5 µH to 15 µH.

3.1.2 Leakage Inductance, Parasitic Capacitance, and DC Resistance

The leakage inductance of the transformer is determined by the coefficient of coupling, K, of the transformer (see Equation 12). For best results, the coefficient coupling should be more than 0.97.

$$K = \frac{L_P - L_{PI}}{L_P}$$

L_P: Primary inductance
L_{PI}: Primary leakage inductance

(12)

Table 1 shows the maximum allowable leakage inductance to protect the FET from inductive spikes when the FET turns off.

Table 1. Guidelines for Leakage Inductance

I_PEAK Range (A)	Maximum Leakage Inductance (µH)
<1.1	0.20
1.1 to 1.3	0.16
1.3 to 1.5	0.14
1.5 to 1.8	0.12

A poor performing transformer may cause an OVDS protection failure to occur. An OVDS protection forces the TPS65552A to stop charging to protect against excessive current flowing on the primary side of the transformer (see Figure 22 and Figure 23).

If VSW crosses Vbat when the internal FET turns OFF (see Figure 22), the Vzero comparator (U2, see Figure 2) detects the timing error, then turns ON. If this comparator fails to detect the timing error, an overcurrent flows through the primary-side transformer as indicated by the dashed circle in Figure 23. This occurs because the off time is too short to transfer the stored energy from the primary side to the secondary side.

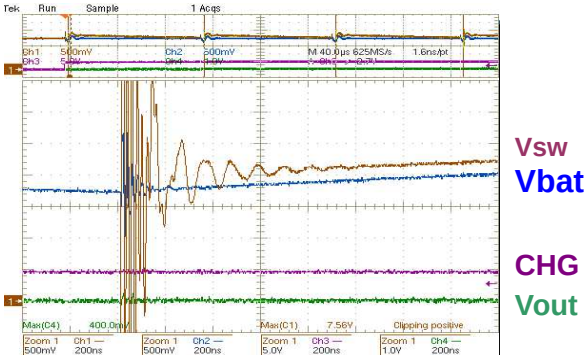

Figure 22. Vsw Exceeding Vbat

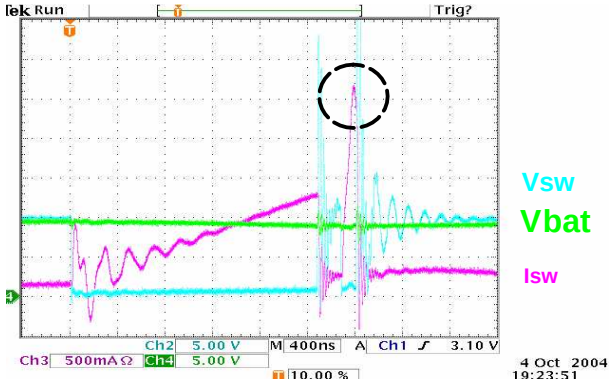

Figure 23. Protection Resulting From Timing Error Detection

The DC resistance is determined by the number of turns of wire in the transformer. A high-DC resistance adds to the overall losses of the transformer and reduces efficiency. Try to select a transformer with the lowest DC resistance. Table 2 and Table 3 list recommended transformers.

Table 2. Recommended Transformers (Tokyo-Coil Engineering)

TYPE NUMBER	SIZE W × D × H (mm)	Lp (µH)	Ls-LEAKAGE (MAX) (µH)	Isw (MAX) (A)	Rpri (mΩ)	Rsec (Ω)	TURN RATIO
TTRN-060S-015	6,8 × 8 × 5	14.0	22	2	200	18	1:10
TTRN-060S-014			27				1:11
TTRN-060S-016			33			21	1:12
TTRN-038S-009	6,5 × 6,4 × 4	14.0	27	1.3	86	15	1:10
TTRN-038S-006			33			15	1:11
TTRN-038S-010			39			18	1:12
TTRN-038S-011	6,5 × 6,4 × 4	7.0	15	2	86	10	1:10
TTRN-038S-007			20			10	1:11
TTRN-038S-012			22			11	1:12

General Enquiry (Tokyo-Coil Engineering)

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WEB http://www.tokyo-coil.co.jp/

Table 3. Recommended Transformers (Kijima-musen)

TYPE NUMBER	SIZE W × D × H (mm)	Lp (µH)	Ls-LEAKAGE (MAX) (µH)	Isw (MAX) (A)	Rpri (mΩ)	Rsec (Ω)	TURN RATIO
SBTI-5.6-1	6,3 x 5,6 x 4	9.5	1.5	1.8	106	24.22	1:10
SBTI-5.6-2			1.2		117	26.46	1:11
SBTI-5.6-3			1.6		105	36.56	1:12

General Enquiry (Kijima-musen)

TEL +81-3-3755-1101

FAX +81-3-3755-5577

E-mail sale@kijima-m.co.jp

3.2 How to Select a Diode

3.2.1 Principle of Reverse Current

When selecting a diode, the most important factor to consider is reverse recovery time (Trr). Selecting a slow Trr affects charging time and efficiency. The secondary inductor current flows in reverse during Trr. The mechanism of reverse current is described in the following steps (see Figure 24 and Figure 25).

1. SW = ON
   - When SW is ON, the primary current flows forward and starts charging. Secondary inductor voltage and diode voltage are reverse biased. The diode is OFF and current does not flow .
2. SW turns OFF
   - When SW turns OFF, the primary current stops flowing, and the voltage on the secondary becomes positive, thus biasing the diode; the diode turns ON, and secondary current flows to the output. The current flow on the secondary side is now charging the photo flash capacitor via the diode.
3. E_{TRANS} is almost zero and reverse current flows
   - The energy-charging primary side (E_{TRANS}) decreases to almost zero. When this happens, SW turns back ON. However, the diode cannot turn off immediately because of the reverse recovery time. Hence, reverse current flows through the diode during Trr. When current finally flows forward in the diode, the voltage on the primary side reduces to less than zero, generally, about –0.7 V.
4. Recovery Diode
   - When its energy is moved to the photo flash charger, output voltage goes up to about 300 V and reduces the secondary-side voltage. Because of this, the anode voltage goes down and the cathode voltage goes up. The diode enters a recovering condition and recovers after Trr.
   - When its voltage goes down about –0.7 V, the body diode of the internal FET turns ON. Its voltage goes up to GND. After Trr, the diode recovers and the reverse current stops.

The selection of a slow Trr diode results in high power consumption in the diode because of reverse current flow. Consequently, high diode power consumption results in slow charging time. To obtain faster charging time and efficiency, select the fastest Trr possible. Table 4 and Table 5 list the recommended diodes.

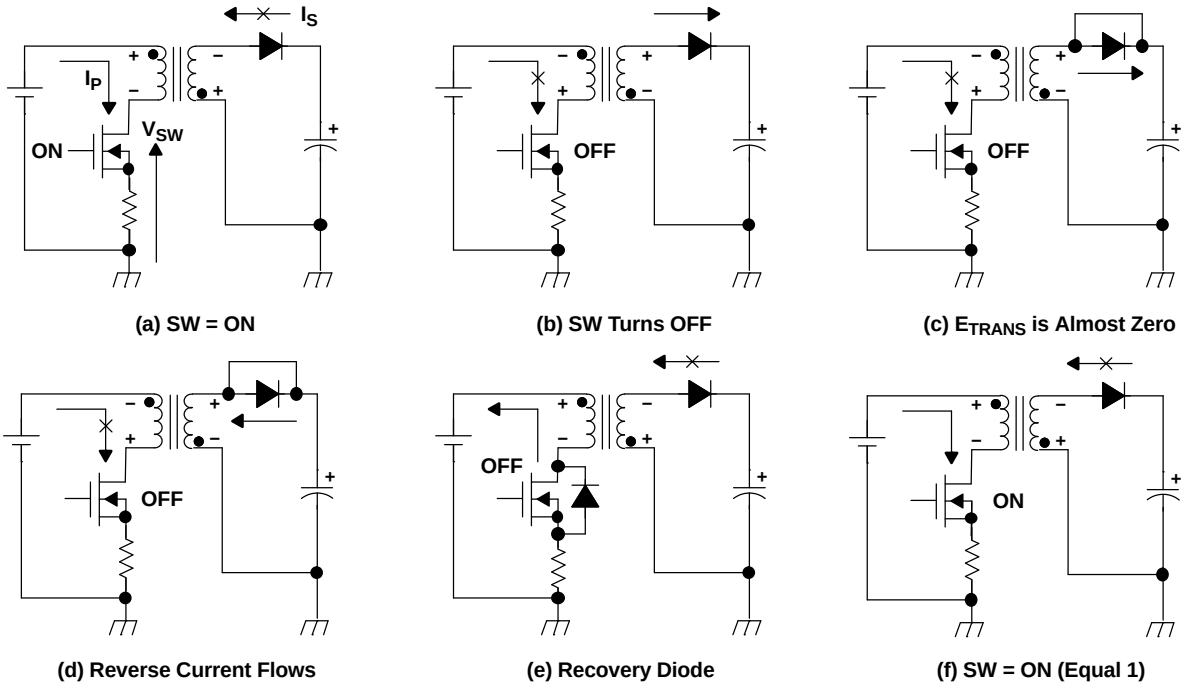


Figure 24. Mechanism of Reverse Current

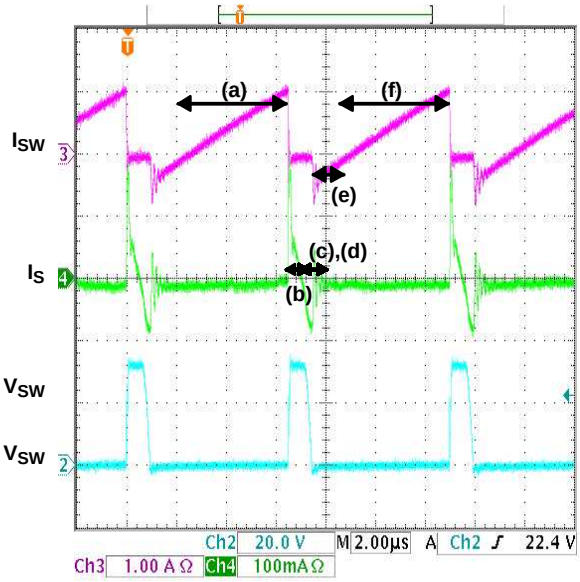


Figure 25. Diagram of Reverse Current

3.2.2 Important Reminders for Selecting Diodes

To select the proper diode for the photo flash charger, consider the following guidelines.

1. Use a faster Trr. The recommended value is less than 100 ns.
2. Current through the diode must not exceed the absolute maximum current flow of the forward current (I_{diode}). I_{diode} can be calculated by Equation 13.

$$I_{diode} = \frac{I\_PEAK}{N}$$

I_PEAK: Peak current flow through primary side inductor
N: Turn ratio of transformer (13)

3. The absolute maximum reverse voltage (V_R) must not be exceeded. It can be calculated by Equation 14.

$$V_R = V_{OUT} + N \times V_{BAT}$$

V_{OUT}: Output voltage
V_{BAT}: Battery voltage
N: Turn ratio of transformer (14)

Recommended diodes are shown in Table 4 and Table 5.

Table 4. Recommended Diodes (Origin Electric)

TYPE NUMBER	MAXIMUM RESERVE VOLTAGE (V)	MAXIMUM FORWARD CONTINUOUS CURRENT (µH)	Trr (ns)
F1P8	800	0.5	30 (1)
FT02P80		0.2	45 (1)
FT02U60	600		70 (2)

(1) The measured condition is IF = 0.5 A, IR = 1 A.
(2) The measured condition is IF = IR = 100 mA

General Enquiry (Origin Electric)

TEL +81-3-5954-9117
FAX +81-3-5954-9122
E-mail h_teramoto@origin.jp
WEB http://www.origin.co.jp/

Table 5. Recommended Diodes (Toshiba)

TYPE NUMBER	MAXIMUM RESERVE VOLTAGE (V)	MAXIMUM FORWARD CONTINUOUS CURRENT (A)	Trr (ns)
CRF02	800	0.5	100 (1)
CRF03	600	0.7	

(1) The measured condition is IF = 1 A, di/dt = -30 A/µs.

General Enquiry (Toshiba)

TEL +81-3-3457-3464
FAX +81-3-5444-9356
E-mail kenji.rikiishi@toshiba.co.jp
WEB http://www.semicon.toshiba.co.jp/

3.3 How to Select an Output Capacitor

Ensure that the output capacitor C1 is a large-value type compared to a forward type. This is because the discharging energy of a flyback transformer is greater than that of a forward transformer. Equation 15 shows the computation for determining the photo flash capacitor value. Using a larger value than the one derived by this computation could burn out the flash element.

$$C_1 \le \frac{2 \times E}{V_{OUT}^2} \quad (15)$$

C_1: Photo flash capacitor value
E: Absolute maximum energy for flash
V_{OUT}: Target output voltage

4 PCB Information

The following PCB layout considerations can also result in better performance.

1. Any design factor resulting in a large leakage inductance value on the primary side should be avoided because it can cause device failure due to overvoltage. The selection of a proper transformer as discussed in the preceding section can help reduce leakage inductance. Figure 26 and Figure 27 show the difference between a good-performing transformer and a poor-performing transformer.
2. The loop indicated by dotted lines shown in Figure 28 should be laid out as small as possible to reduce surge voltage. If this loop is large, the parasitic inductance might cause device failure.
3. The parasitic resistance in the power path from the battery to the primary-side turn of the transformer should not be ignored. The TPS65552A has a one-point ground connection inside the IC at PGND PAD. Therefore, the PCB layout should also keep a one-point connection of ground at the PGND terminal of TPS65552A. Note: a bypass capacitor (C2 in Figure 28) is required to avoid noise by grounding.
4. The TPS65552A uses the V_{CC} input as its reference voltage; therefore, the ground of the power unit that sources V_{CC} should be connected to PGND (see the preceding note 1).

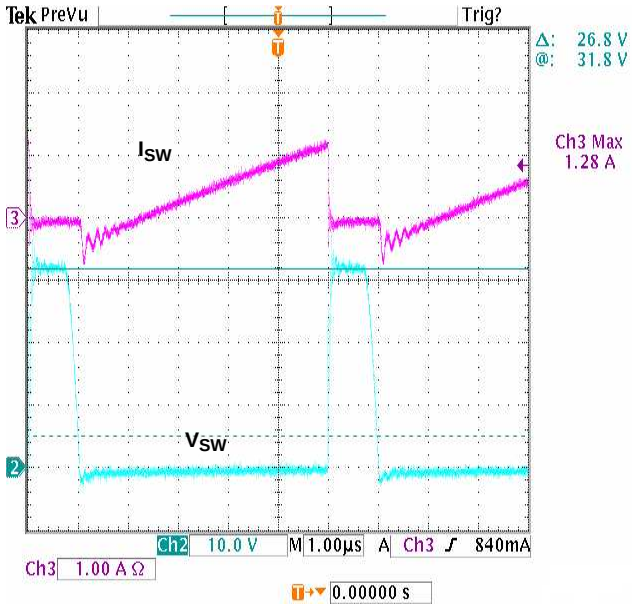


Figure 26. Switching Voltage of a Good-Performing Transformer

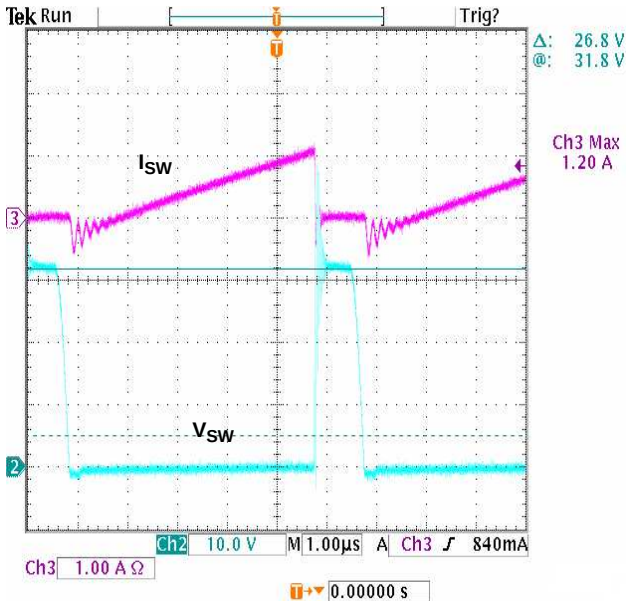


Figure 27. Switching Voltage of a Poor-Performing Transformer

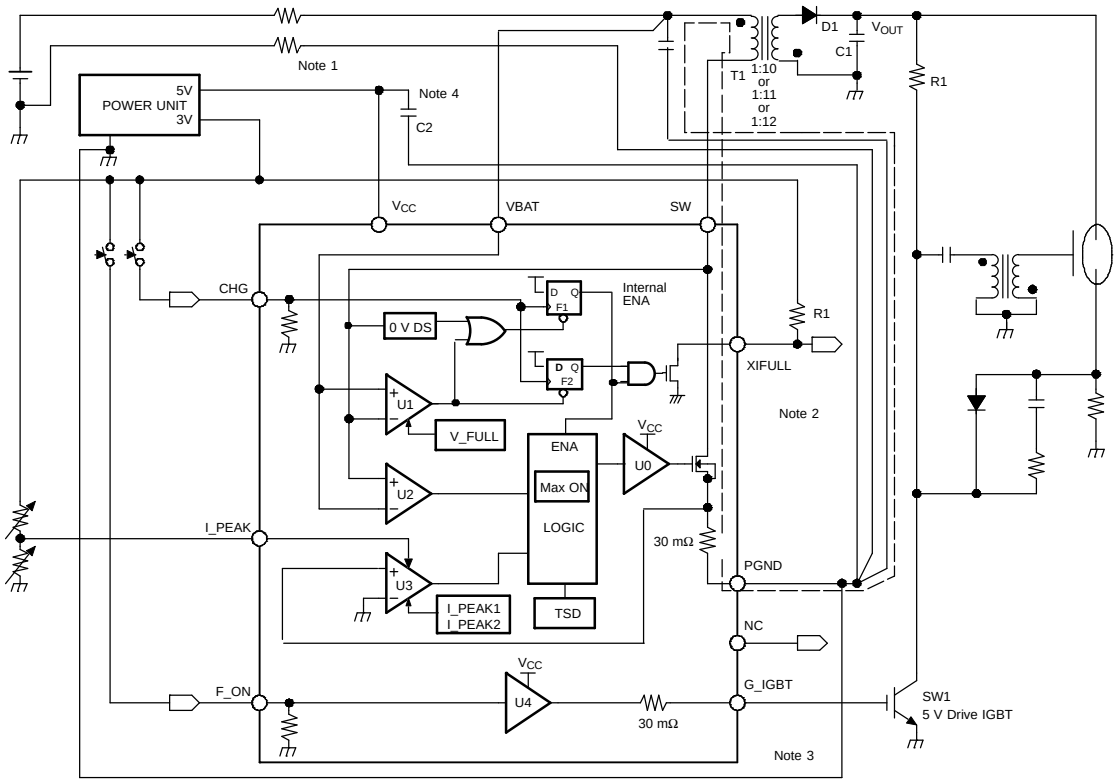


Figure 28. PCB Design Guideline

5 Conclusion

This application report demonstrates several advantages of the TPS65552A:

1. These devices can be designed into a smaller area, and require few external components because of the integrated IGBT driver.
2. The peak current on the primary-side inductor can be set to a maximum of 1.8 A by external voltage reference. This makes it possible to control battery life, to protect against system shutdown by large currents, and to change the charging time.
3. By selecting the proper external components, it is possible to achieve 70% or greater efficiency and charging time less than 4 seconds with a battery voltage of 4.2 V and the voltage on the I_PEAK pin more than 1.4 V.

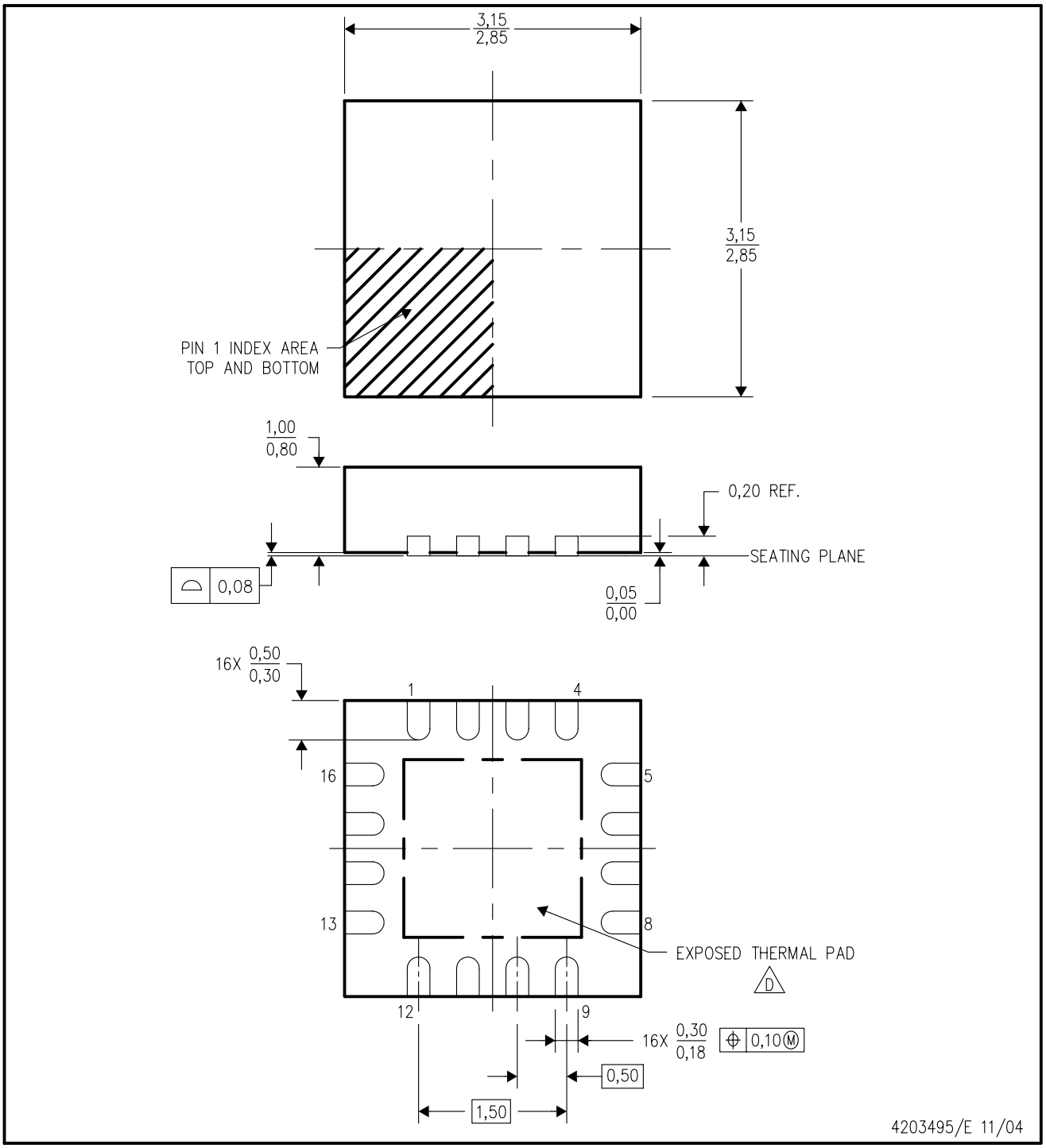
To maximize TPS65552A performance:

1. Choose a diode with the best Trr speed, and select a transformer with the best coefficient of coupling . These affect charging time and efficiency.
2. Good system layout of the PCB can result in enhanced performance.

6 Recommended Foot Pattern Information

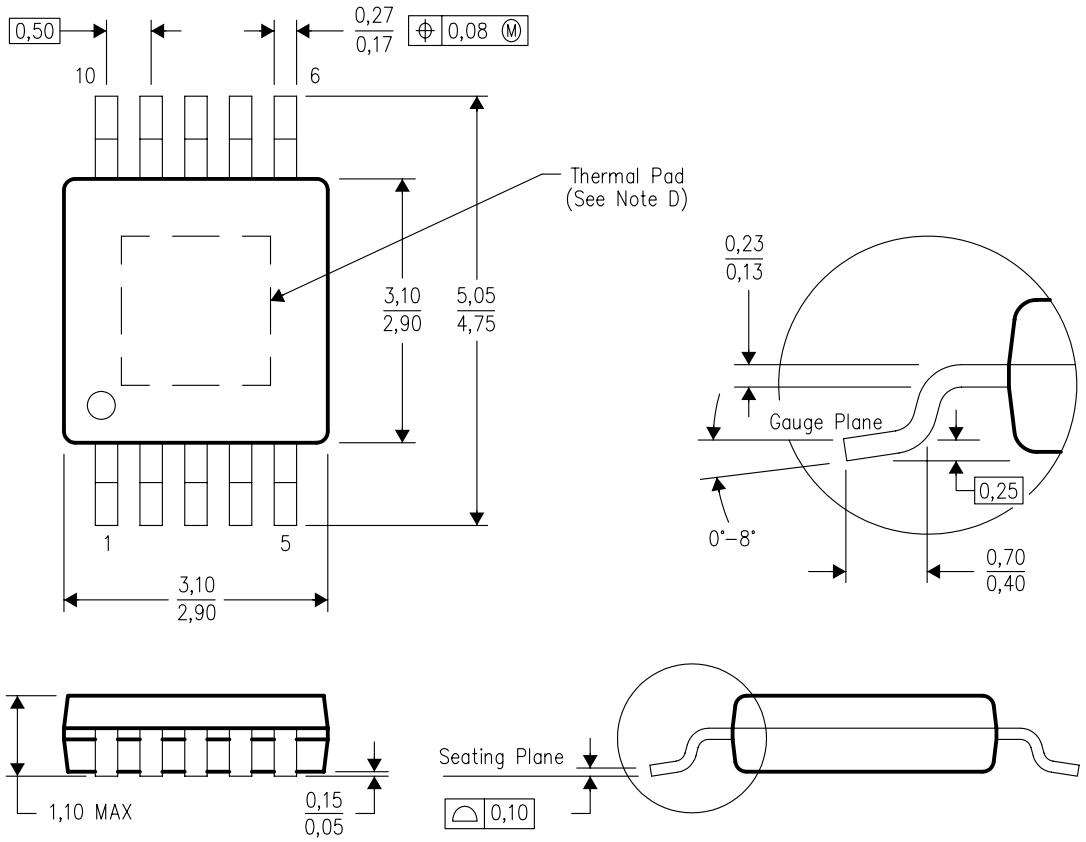
The recommended foot pattern information appears on the following pages.

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073273/D 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187 variation BA–T.

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