

TPS65270 Loop Compensation Design Consideration

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ABSTRACT

Peak current mode (PCM) is a popular, affordable, and stable control mode. This report discusses the control principle and small signal model, as well as the stability and loop compensation approach for TPS65270.

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1 Introduction

TPS65270 is a dual channel DCDC with peak current mode (PCM) implementation. The integrated synchronous rectifier power FET, as well as the novel power save mode, power-up sequence, and over-current protection configuration, benefit the customer design with high flexibility, efficiency, and more compact size.

This dual DCDC is designed with 5- to 16-V wide input, and a loading capability of up to 3/2 A output currents. It is all MOSFET integrated, has individual SS and EN pins, adjusted frequency (300 kHz ~ 1.4 MHz), automatic Power-Save-Mode for light load operations and 24-pin TSSOP and 24-pin 4 x 4 mm QFN.

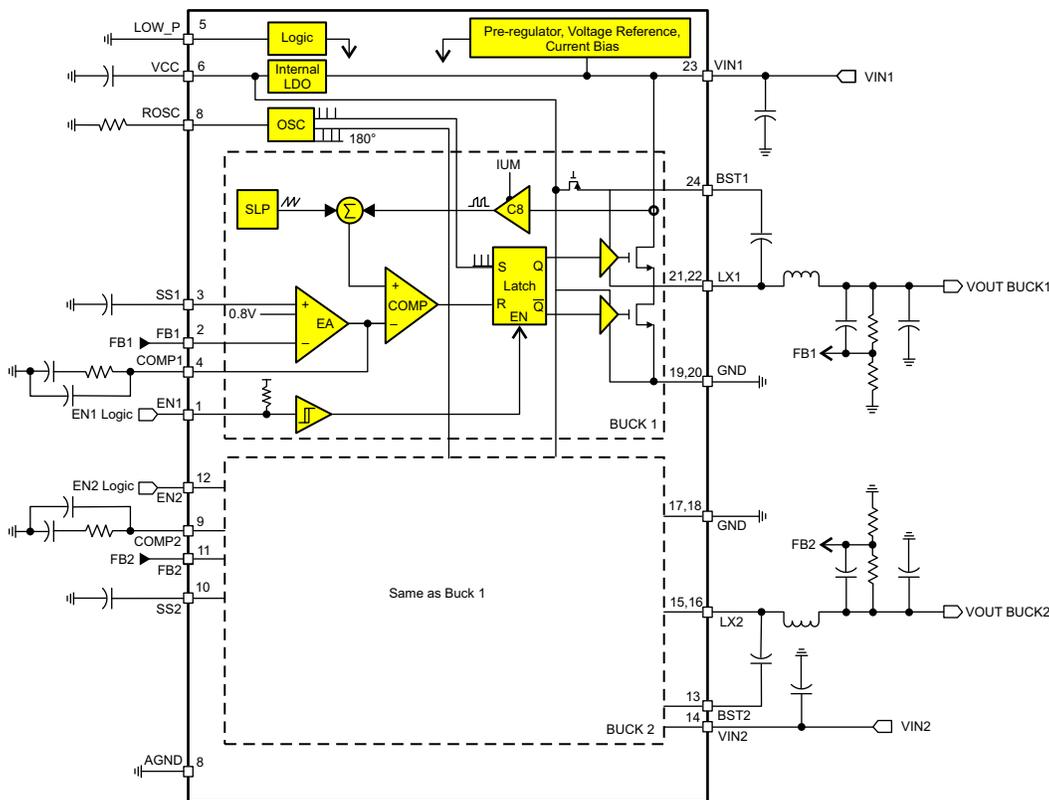


Figure 1. TPS65270 Block Diagram

2 PCM Principle and Modeling

2.1 PCM Behavior

PCM employs a current-sampling RAMP to compare with the output of the Error Amplifier (EA), therefore generating the regulated duty cycle as shown in Figure 2. PCM initiates the fast response by input or loading transient with current and voltage loops, achieving higher crossover frequency.

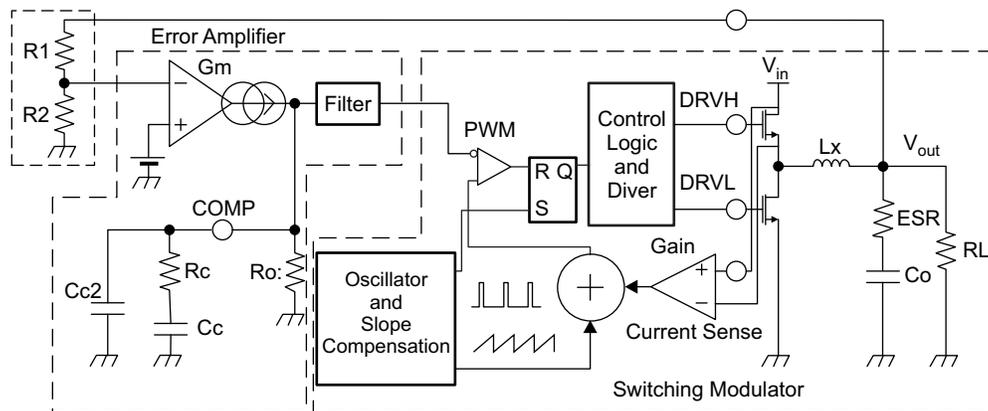
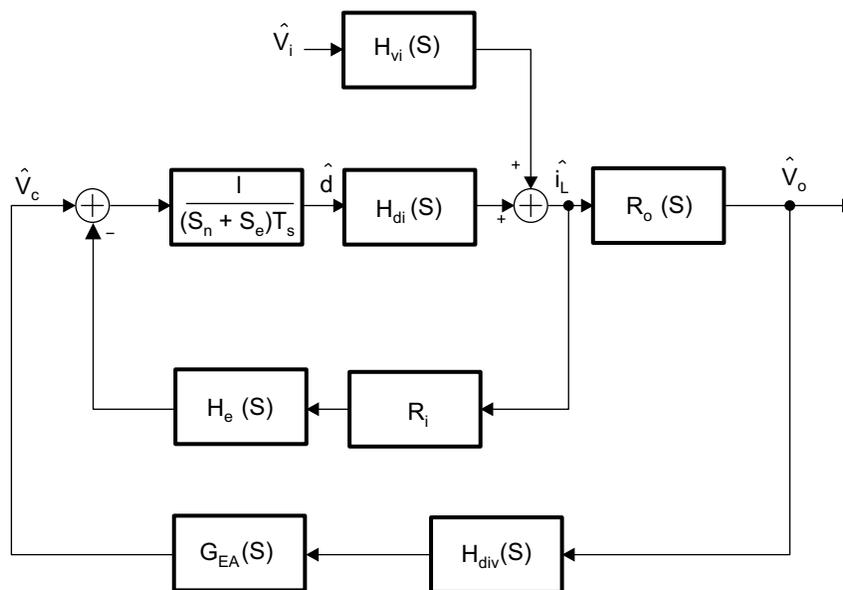


Figure 2. PCM Implementation

2.2 Overall Control Block Diagram Implementation

The PCM converter overall control block is implemented as seen in Figure 3:



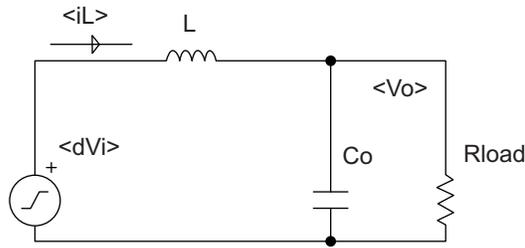
^ means small signal distortion

Figure 3. Overall Control Implementation

$G_{EA}(S)$ is the gain function of the error amplifier with a certain compensation setup. $H_{div}(S)$ is the gain of the divided resistor network.

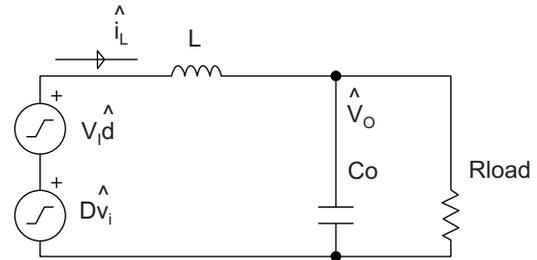
2.3 Small Signal Model of the TPS65270 Synchronous BUCK Converter

Figure 4 shows the average model of the BUCK converter. The small signal of the BUCK converter is in Figure 5:



< > means the average value by a switching cycle

Figure 4. Average Model



^ means small signal distortion

Figure 5. Small Signal Model

2.4 Transfer Function Derivation from the Average Mode and the Small Signal Model

The gain function from inductor current to output is shown in Equation 1:

$$R_o(S) = \frac{V_o(S)}{I_L(S)} = \frac{R_{Load}}{1 + SR_{Load}C_o} \quad (1)$$

The gain function from duty cycle to inductor current is seen in Equation 2:

$$H_{di}(S) = \frac{I_L(S)}{D(S)} = \frac{V_i(1 + SR_{Load}C_o)}{R_{Load} + SL + S^2R_oLC_o} \quad (2)$$

Considering the practical crossover frequency is much higher than the corner frequency, $1/(2\pi\sqrt{LC_o})$, with PCM, we simplify Equation 2 to :

$$H_{di}(S) = \frac{I_L(S)}{D(S)} \approx \frac{V_i}{SL} \quad (3)$$

The gain function from V_{in} to inductor current is seen in Equation 4:

$$H_{vi}(S) = \frac{I_L(S)}{V_i(S)} = \frac{\left(SC_o + \frac{1}{R_{Load}} \right) D}{1 + S \frac{L}{R_{Load}} + S^2 LC_o} \approx \frac{D}{SL} \quad (4)$$

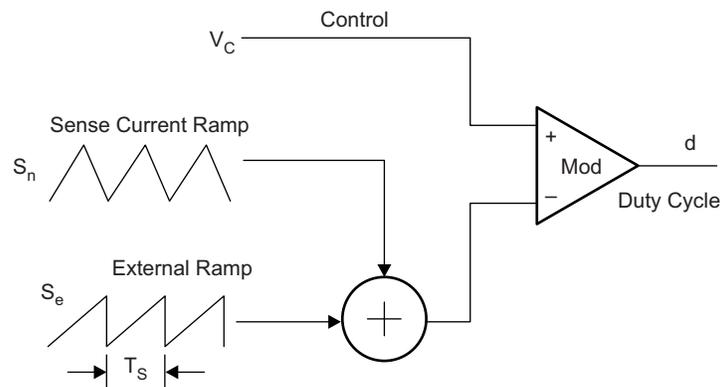


Figure 6. PWM with Slope Compensation

The gain from control to duty cycle is seen in Equation 5:

$$FM = \frac{1}{(S_n + S_e)T_s} \quad (5)$$

Where:

S_n is the rising slope of the inductor current

S_e is the slope compensation rising slope element

T_s is the switching cycle

Considering the sampling-hold circuitry for the current ramp, the gain function is $H_e(S)$:

2.5 Inductor Current Sampling-Hold and Slope Compensation

The Ridley sampling-hold model is shown in Figure 7 and Figure 8:

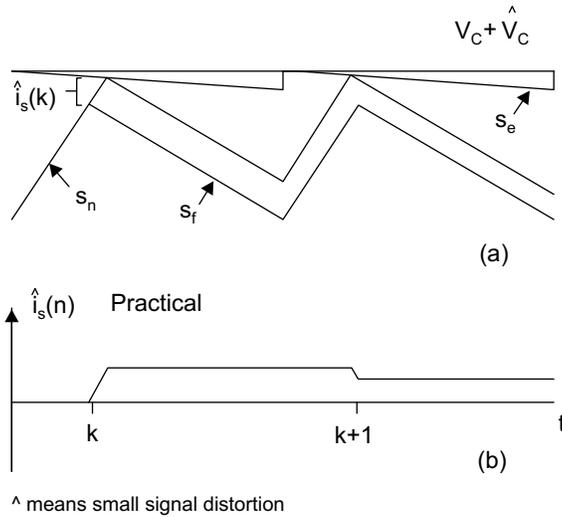


Figure 7. Practical Sampling-Hold Waveforms with the Current and Control Distortion

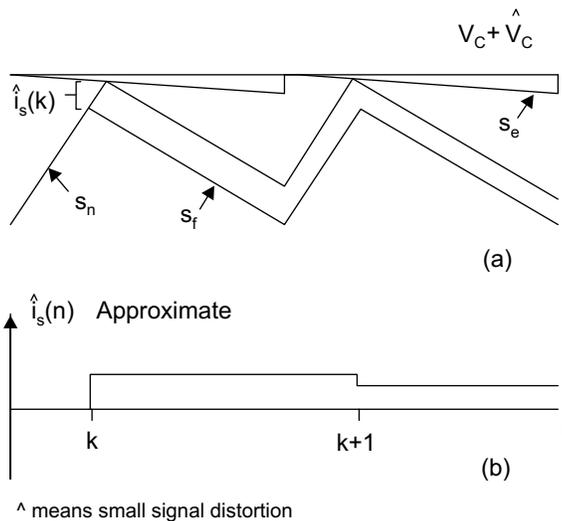


Figure 8. Approximated Sampling-Hold Waveforms with the Current and Control Distortion

The discrete equation is derived to describe the sampling-hold behavior in Equation 6:

$$\hat{i}_L(K+1) = -\alpha \hat{i}_L(k) + \frac{1}{R_i(1+\alpha)} \hat{v}_c(k+1) \quad (6)$$

Here: $\alpha = \frac{S_f - S_e}{S_n + S_e}$ Where:

S_f is the inductor current ramp down slope.

S_n is the rising slope of the inductor current

S_e is the slope compensation rising slope element

Based on the discrete sampling model, Z, domain translation results should be:

$$H(Z) = \frac{I_L(Z)}{V_C(Z)} = \frac{1+\alpha}{R_i} \times \frac{Z}{Z+\alpha} \quad (7)$$

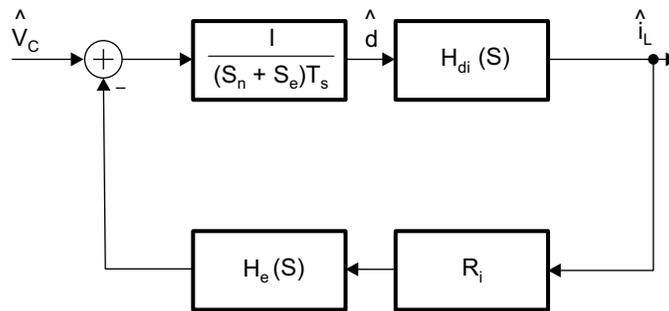
Based on Z domain stability theory, the single pole should meet this condition: $|\alpha| < 1$

As a result, the slope compensation element, S_e , should adequately meet: $S_e > S_n / 2$

With substituting "Z" with " $e^{T_s S}$ " and considering zero order sampling-hold gain $\frac{1-e^{-T_s S}}{T_s S}$, the gain function is seen in Equation 8:

$$H(S) = \frac{1+\alpha}{R_i} \times \frac{e^{T_s S}}{e^{T_s S} + \alpha} \times \frac{1-e^{-T_s S}}{T_s S} = \frac{1+\alpha}{R_i T_s S} \times \frac{e^{T_s S} - 1}{e^{T_s S} + \alpha} \quad (8)$$

According to Figure 6, the $H(S)$ is described as Figure 9, considering Equation 3 for $H_{di}(S)$



^ means small signal distortion

Figure 9. Control Block for Current Regulation Loop

$$\text{As a result: } H_e(S) = \frac{T_s S}{e^{T_s S} - 1} \approx 1 - \frac{S}{2} + \frac{S^2}{\left(\frac{\pi}{T_s}\right)^2} \quad (9)$$

2.6 Simplify the Current Loop Parameters

Based on Equation 9 and Equation 10, the approximate gain from control to inductor current should be:

$$H(S) \approx \frac{1}{R_i} \times \frac{1}{1 + S \left[\frac{T_s L (S_n + S_e)}{V_I R_i} - \frac{T_s}{2} \right] + S^2 \times \frac{T_s^2}{\pi^2}} \quad (10)$$

$$\text{Let: } R_e = \frac{2L}{T_s \left(\frac{2}{1+\alpha} - 1 \right)} : C_e = \frac{T_s^2}{\pi^2 L} \quad (11)$$

And considering Equation 4, let:

$$F_i = \frac{D}{L} \left[\frac{L}{R_e} - \frac{(1-D)T_s}{2} \right]$$

then the current loop is simplified as shown in Figure 10:

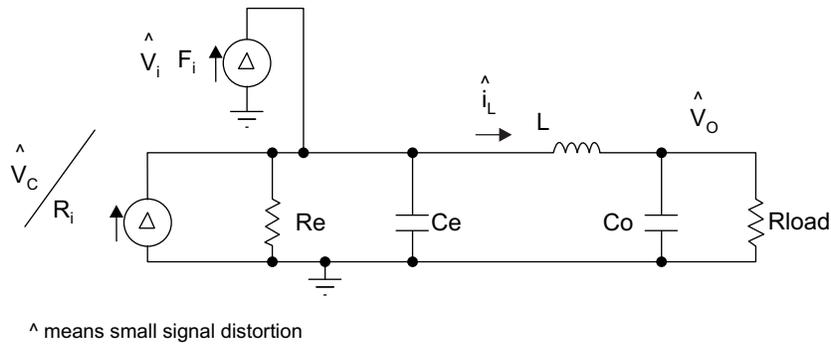


Figure 10. Equivalent Small Signal Model

Figure 10 reveals an internal resistance, R_e and C_e , in the small signal model:

$$\text{If: } R_e = \frac{2L}{T_s \left(\frac{2}{1+\alpha} - 1 \right)} > 0 \tag{12}$$

Then: $0 < 1 + \alpha < 2$; Or $|\alpha| < 1$

As a result $S_e > S_n / 2$

In conclusion, the PCM small signal model is simplified as shown in Figure 10. Meanwhile, a positive R_e brings up a stable system without the sub-harmonic oscillation, which is reached by a certain amount of slope compensation. The simplified model is more feasibly simulated with EDA tools.

3 TPS65270 Modeling and Loop Compensation

3.1 Results vs Simulation Based on a Practical Design

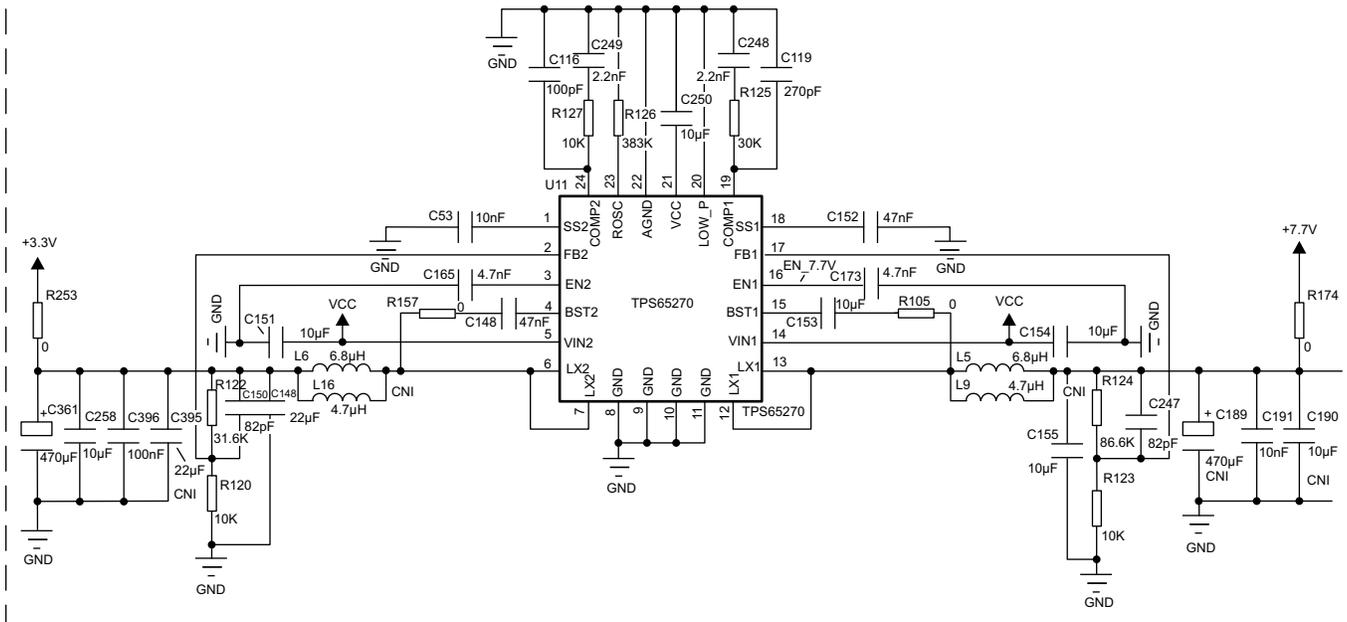


Figure 11. TPS65270 Design with 3.3- and 7.7-V Output

Figure 11 shows the frequency is 635 kHz, input is 12 V and output is 3.3 V/2 A and 7.7 V/1 A. For channel 2 with 3.3-V output:

$$S_n = \frac{(V_i - V_o)}{L} R_i = \frac{(12 - 3.3)}{6.8 \mu\text{H}} \times 0.1 = 0.128\text{V} / \mu\text{s}$$

$$S_f = \frac{V_o}{L} R_i = \frac{3.3}{6.8 \mu\text{H}} \times 0.1 = 0.048\text{V} / \mu\text{s}$$

(13)

TPS65270 slope compensation: $S_e = 0.18 \text{ V}/\mu\text{s}$; then: $\alpha = \frac{S_f - S_e}{S_n + S_e} = -0.427$

According to Equation 11 and Figure 10: $R_e = 3.47 \Omega$, $C_e = 37 \text{ nF}$

The overall small signal modeling using TINA is as follows: Figure 13.

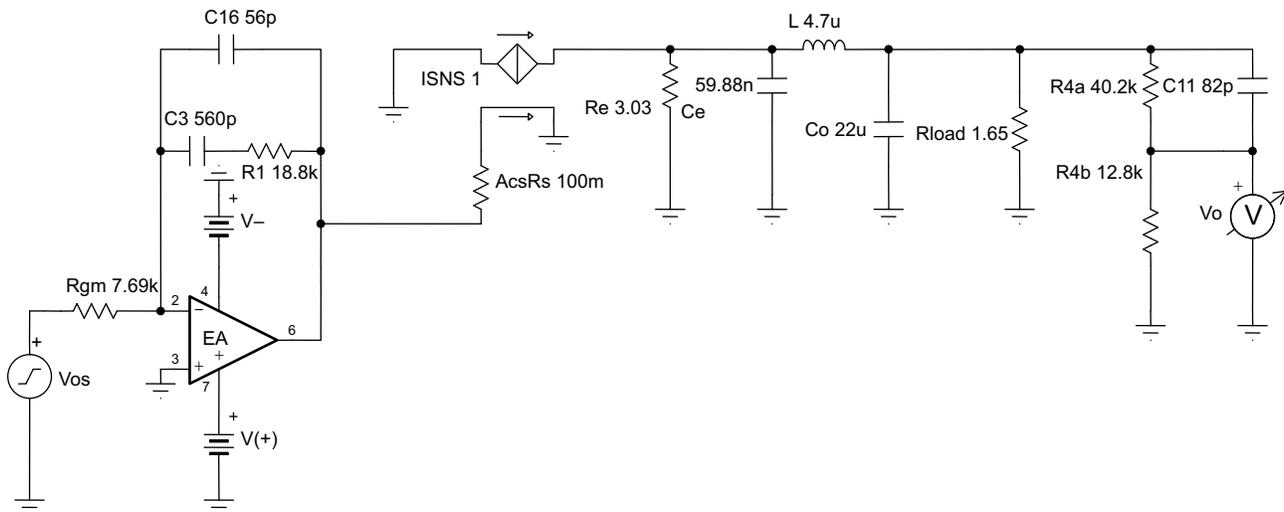


Figure 12. Overall Small Signal Modeling for TPS65270 with 3.3-V/0.65-A Output

Figure 13 shows the AC simulation results. It revealed a 58° phase margin and 80-kHz crossover frequency.

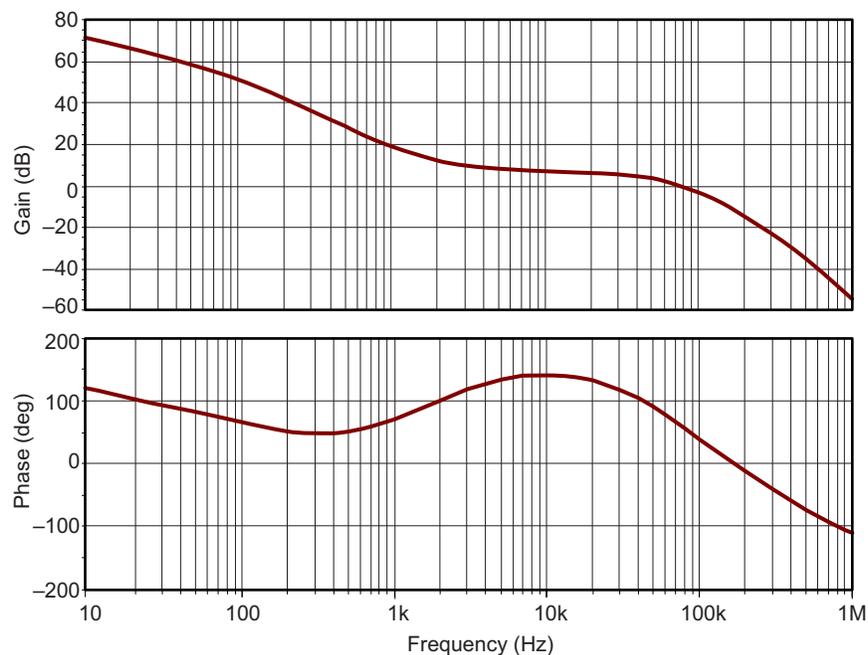


Figure 13. Bode Plot of the AC Simulation

The practical test results for the 3.3 V/0.65 A are shown in Figure 14:

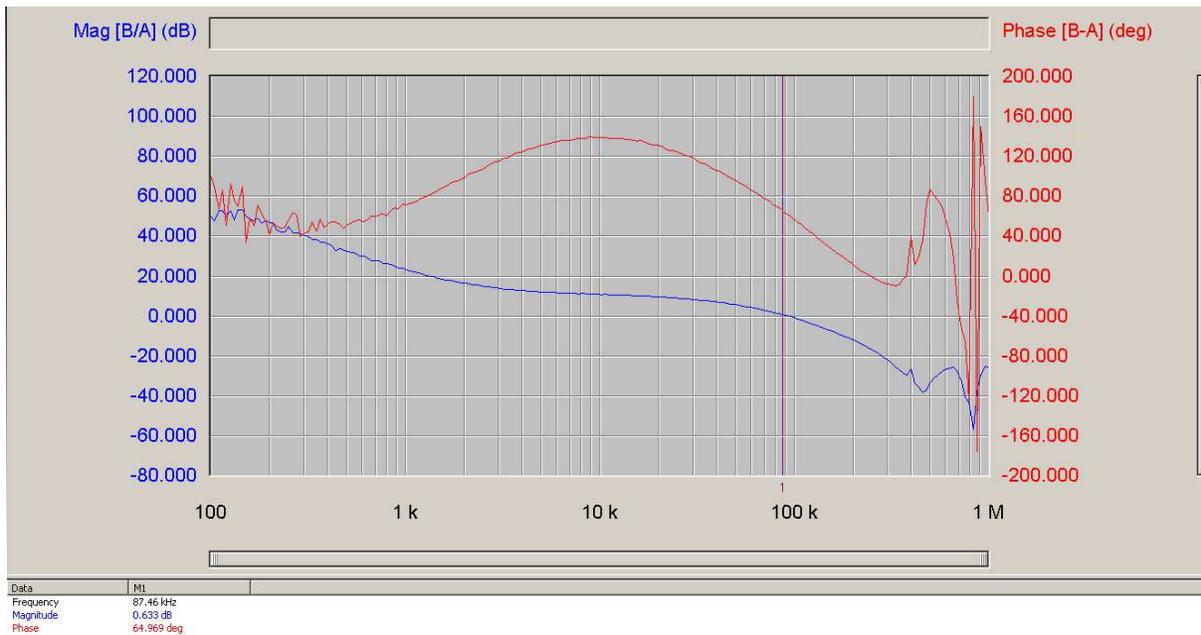


Figure 14. Closed Loop Bode Plot Test Results at Vin = 12 V and Vout = 3.3 V/0.65 A

The loop parameters in Figure 14 are 86-kHz crossover frequency and 60° phase margin. The model shown in Figure 10 is used in PCM loop compensation.

3.2 Simulation for a Specific Design

A design topic: Vin = 12 V, Vout = 3.3 V at 2 A, fs = 600 kHz, L = 4.7 μH

The related parameters are shown in Table 1:

Table 1. Modeling Parameters

Vin (V)	Vout (V)	L (μH)	f (kHz)	Ri	Se (V/μs)
12	3.3	4.7	600	0.1	0.18
Sn (V/μs)	Sf (V/μs)	α	Re	Ce (nF)	
0.19	0.07	-0.30	3.03	59.88	

The small signal modeling from control to output:

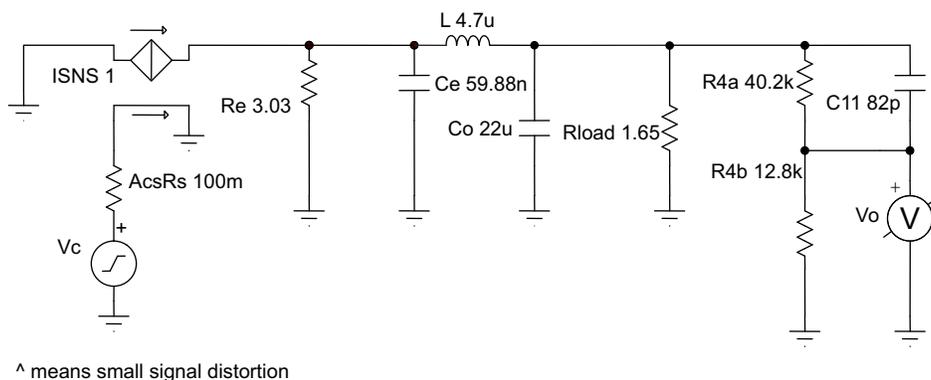


Figure 15. Signal Modeling From Control to Output

The simulation reveals the bode plot in [Figure 16](#).

Assuming a target crossover frequency is 50 kHz, and target phase margin is 70°.

According to the bode plot in [Figure 16](#):

$$G_{co}(50 \text{ kHz}) = -6.87 \text{ dB}; \text{Phase}_{co}(50 \text{ kHz}) = -77^\circ$$

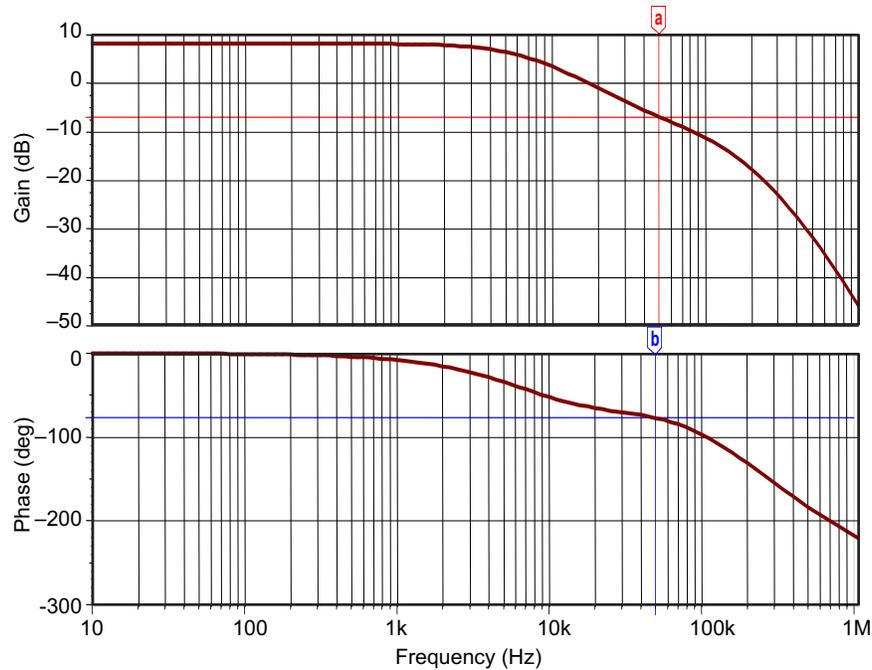


Figure 16. Bode Plot of Control to Output

The Type II compensation network setup:

Assume a crossover frequency of $f_c = 50 \text{ kHz}$.

$$\text{Let: } A = |G_{co}(j2\pi f_c)| = 10^{\frac{-6.9}{20}} = 0.45; \quad K = \text{tg}\left(\frac{70^\circ - (-78^\circ) - 90^\circ}{2} + 45^\circ\right) = 3.5$$

$$\text{And: } \frac{K}{A} = \frac{1}{2\pi f_c R_{gm} C_7}; \quad R_{gm} = \frac{1}{130\mu} = 7.69 \text{ k}\Omega$$

Then: $C_{16} = 52.9 \text{ pF}$, select $C_{16} = 56 \text{ pF}$, $C_3 = (K^2 - 1)$, $C_{16} = 590 \text{ pF}$, select $C_3 = 560 \text{ pF}$:

$$R_{10} = \frac{K}{2\pi C_3 f_c} = 18.8 \text{ k}\Omega$$

As a result in [Figure 17](#) and [Figure 18](#), the final crossover frequency is 49 kHz and the phase margin is 69°.

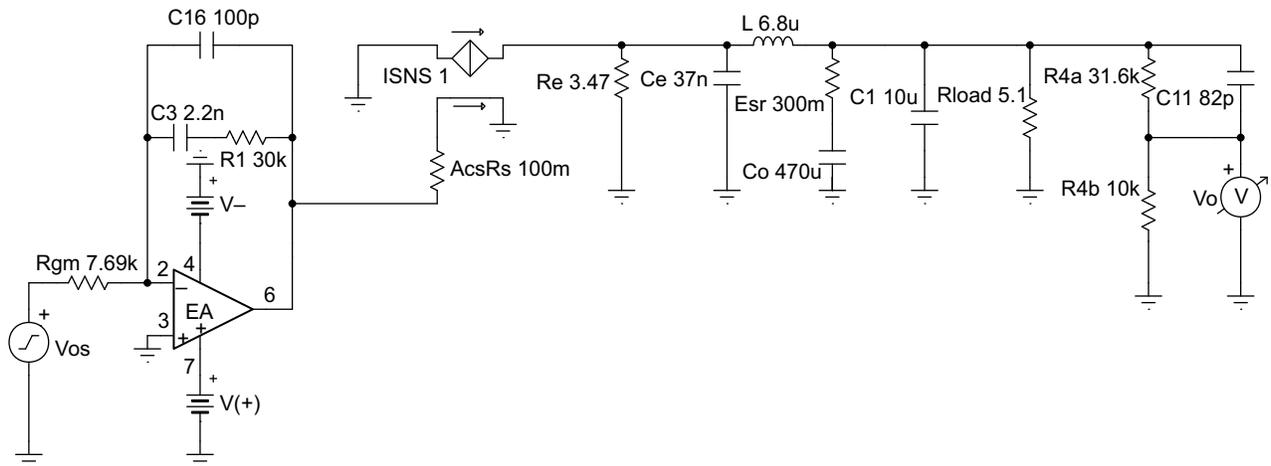


Figure 17. Overall Small Signal Modeling

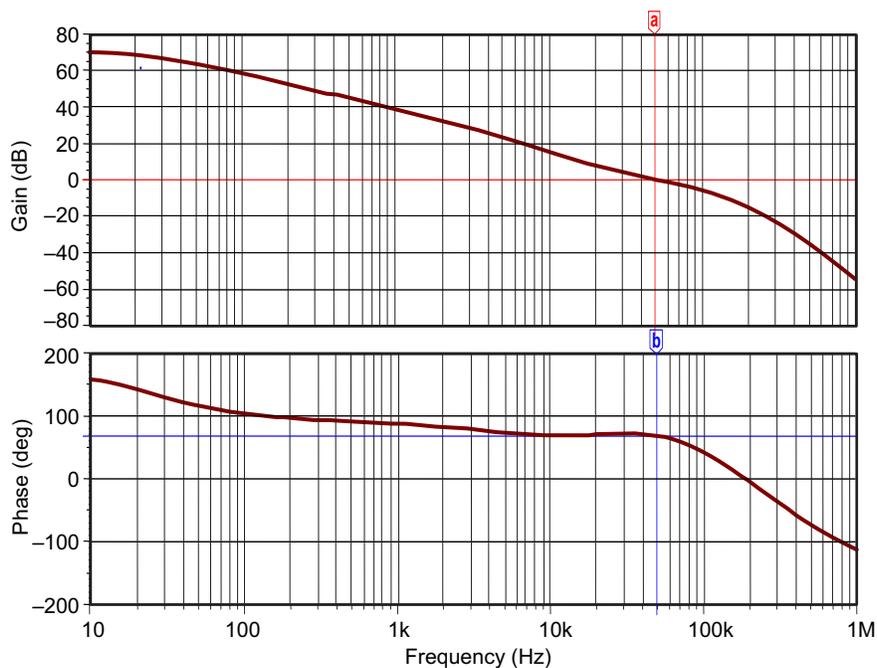


Figure 18. Overall Gain and Phase Bode Plot

4 Conclusion

This application note introduces a practical modeling approach for PCM control using TPS65270. A simple equivalent circuit representation is shown for easy understanding and implementation of peak current-mode control. Simulation results are used to demonstrate the proposed model.

5 References

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