

TPS65320-Q1 and TPS65320C-Q1 Design Checklist

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ABSTRACT

This application note for TPS65320-Q1 and TPS65320C-Q1, which are single high-voltage switch-mode asynchronous buck power supplies with an LDO regulator (see the corresponding device data sheet), lists the connection details for each pin. The pin details include a brief explanation of the function of each pin or signal and whether the signal is analog or digital. Use this information to check the connectivity for each pin on a system schematic.

In the event of any inconsistency between the official specification and any user's guide, application report, or other referenced material, the data sheet specification will be the definitive source. For the TPS65320-Q1 data sheet, see *TPS65320-Q1 40-V Step-Down Converter With Eco-mode™ and LDO Regulator*, [SLVSAY9](#). For the TPS65320C-Q1 data sheet, see *TPS65320C-Q1 36-V Step-Down Converter With Eco-mode™ and LDO Regulator*, [SLVSD50](#).

Table 1. TPS65320-Q1 and TPS65320C-Q1 Design Checklist

NAME	PIN NO.	TYPE	I/O ⁽¹⁾	DESCRIPTION	RECOMMENDED CONNECTION	UNUSED FEATURES
BOOT	1	Analog	O	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in the buck converter.	Connect a capacitor on the order of 100 nF between BOOT and SW; use low impedance, low inductance, and a small loop. Avoid using vias in the signal path.	N/A
COMP	12	Analog	O	Error amplifier output of buck and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the inductor.	Connect Type2 compensation network, designed for a bandwidth of one-sixth to one-tenth of f_{SW} . Calculate using the Component Selection Tool .	N/A
EN1	8	Digital	I	Enable input for Buck (with an internal pulldown resistor). An input voltage higher than 2.5 V enables the converter, whereas an input voltage lower than 0.7 V disables the converter. Note: if disabled, the LDO uses VIN as supply.	Pull high for activation, low to deactivate. Hard-wired or μ C-controlled	Buck is off if left open.
EN2	7	Digital	I	Enable input for LDO (with an internal pulldown resistor). An input voltage higher than 2.5 V enables the LDO, whereas an input voltage lower than 0.7 V disables the LDO.	Pull high for activation, low to deactivate. Hard-wired or μ C-controlled	LDO is off if left open.
FB1	11	Analog	I	Feedback-voltage pin for the buck. The buck converter regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.	Choose resistor network to set FB1 voltage to 0.8 V, allow for >10 μ A current. For noise cancellation, a capacitor on the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A

⁽¹⁾ I = Input; O = Output

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Table 1. TPS65320-Q1 and TPS65320C-Q1 Design Checklist (continued)

NAME	PIN NO.	TYPE	I/O ⁽¹⁾	DESCRIPTION	RECOMMENDED CONNECTION	UNUSED FEATURES
FB2	5	Analog	I	Feedback voltage pin for LDO. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.	Choose resistor network to set FB2 voltage to 0.8 V; allow for >10 μ A current. For noise-cancellation, a capacitor on the order of 47 pF to 100 pF in parallel with the lower resistor can help.	N/A
GND	13	–	O	Ground reference	Provide a low-impedance, low-resistance path to GND, ideally to the GND plane. For lowest noise on the LDO, connect LDO to GND only underneath the IC.	N/A
LDO_OUT	4	Power	O	Linear regulator output. Decouple with a low-ESR ceramic output capacitor in the range of 1 μ F to 47 μ F connected from this terminal to ground.	Decouple with a low-ESR ceramic output capacitor in the range of 1 μ F to 47 μ F connected from this terminal to ground.	N/A
nRST	6	Digital	O	Active low, push-pull reset output, asserted high (at the actual LDO output voltage) after the LDO of the device starts regulating. Note, the pin does not indicate if the Buck is in regulation.	Connect to the interrupt input of the processor or leave open. An additional pullup of, for example, 10 k Ω can strengthen the output.	Leave open
RT/CLK	9	Analog	I	External resistor connected ground to program the internal oscillator. An alternative option is to feed an external clock to provide a reference for the switching frequency.	Connect a resistor to GND for appropriate frequency, for example, 300 k Ω for 400 kHz, 50 k Ω for 2.1 MHz.	N/A (Device does not switch if unconnected.)
SS	10	Analog	I	Soft-start input for buck converter. The buck controller regulates the FB1 voltage to the lower of 0.8 V or the SS pin voltage. An internal pullup current source of typically 2 μ A is present at the pin, and use of an appropriate capacitor connected here can set the soft-start ramp duration.	Connect a capacitor to GND for soft-start; calculate the capacitor value using the Component Selection Tool .	N/A
SW	14	Power	O	Source node of internal switching FET	Keep the trace to the inductor short and low impedance.	N/A
VIN	2	Power	I	Input for internal supply, and drain-node input for internal high-side MOSFET. Connect a bypass capacitor between this pin and ground to filter noise.	Decouple with a total capacitance on the order of 100 μ F, consisting of several smaller, different values in parallel (for example, 82 μ F, 10 μ F, and 2.2 μ F). Keep close to the IC with a low-impedance, low-inductance path. Avoid using vias in the signal path.	N/A
VIN_LDO	3	Power	I	The output of the buck is the LDO input when Buck and LDO are both ON. If Buck is disabled or out of regulation, VIN becomes the input. Alternately, another supply can power VIN_LDO. This supply must not exceed 20 V maximum and must be lower or equal to VIN-voltage. Indifferent if available, in case the Buck is disabled, VIN will still be the source for the LDO. Do not leave this pin unpowered.	This input shares the output capacitor of the buck. If the output capacitor of the buck is far away, decouple close to the pin with approximately 100 nF. If an alternative voltage source is used as LDO-supply, decouple locally with approximately 4.7 μ F plus approximately 100 nF.	N/A

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (January 2015) to B Revision	Page
• Added part number TPS65320C-Q1.....	1
• Added data sheet reference SLVSD50 for TPS65320C-Q1.....	1
• Added alternate power supply information.....	2

Changes from Original (April 2013) to A Revision	Page
• Changed the description, recommended connection, and unused features for EN1 and EN2	1

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