Application Report
SLVA602–November 2013

Design Procedure for TPS54122

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ABSTRACT

This application report details the design procedure of a low-noise, 3-A power supply with the integrated switcher and low-dropout (LDO) regulator of the TPS54122. The designer must know a few parameters in order to start the design process and typically determines them at the system level.

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1 Introduction

The following application report provides a detailed explanation of the design procedure for a low-noise power supply.

The known parameters shown in Table 1 apply to this example.

Table 1. Design Parameters

Parameters	Value
SW output voltage (Vout)	2.16 V
LDO output voltage (LDOVout)	1.8 V
Transient response at Vout	Δ Vout = 5%
Input voltage (Vin)	5 V nominal, 3 V to 5.5 V
Output voltage ripple at Vout (Voripple)	< 30 mV_{PP}
Switching frequency (fsw)	500 kHz
Output current (Iout)	3 A

2 Typical Application Schematic

The application schematic shown in Figure 1 meets the parameters listed in Table 1. This circuit is available as the TPS54122EVM-201 evaluation module. The design procedure is given in this section. For more information about Type II and Type III frequency compensation circuits, see application report SLVA352A, *Designing Type III Compensation for Current Mode Step-Down Converters*.

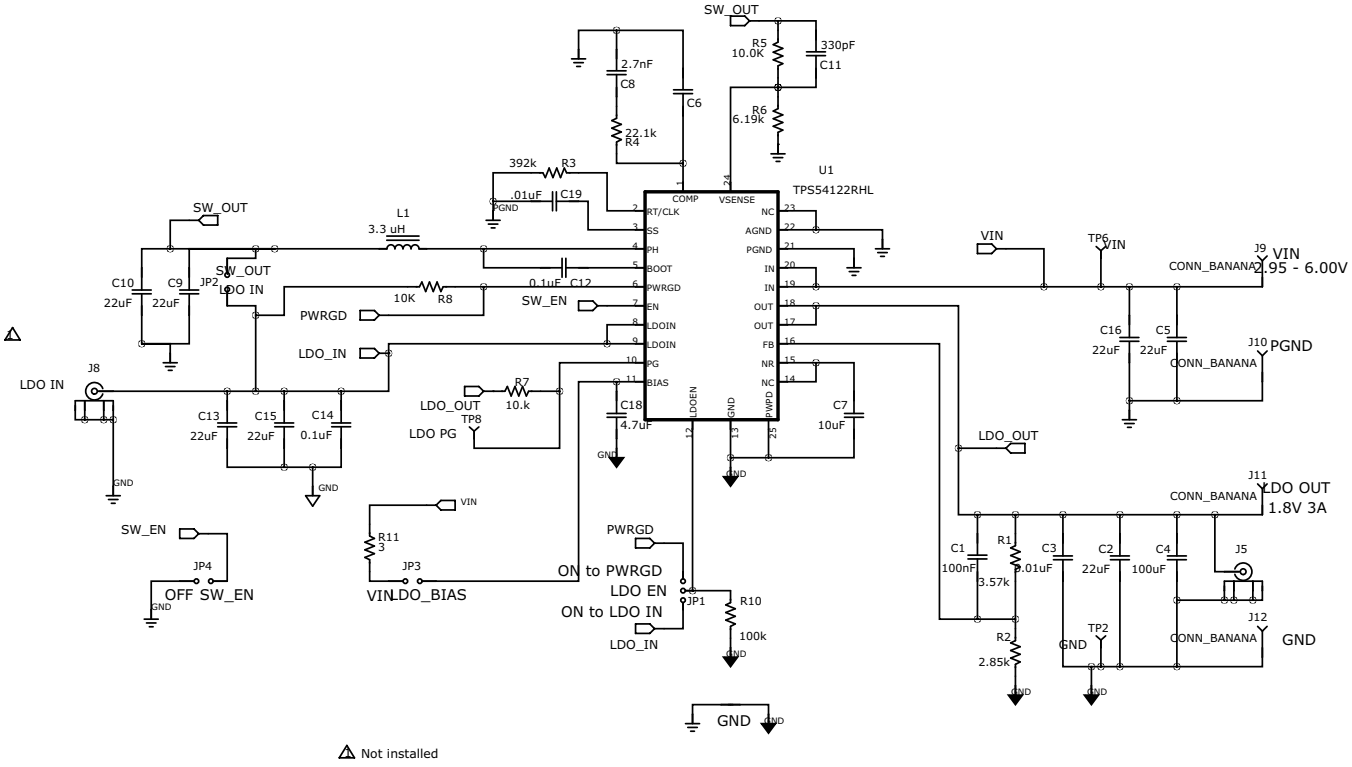

Figure 1. Typical Application Circuit

3 Operating Frequency

The first step is to decide on a switching frequency for the regulator. This step involves a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size, using lower-valued inductors and smaller-output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes additional switching losses that can negatively impact the converter efficiency and thermal performance. In this design, the selection of a moderate switching frequency of 500 kHz achieves both a small solution size and high-efficiency operation. Using the resistor at the RT/CLK pin (R3) sets this frequency.

$$R3\ (k\Omega) = 311890 \times fsw\ (kHz)^{(-1.0793)} \tag{1}$$

Using Equation 1, the required resistance for a switching frequency of 500 kHz is 381 kΩ. This design uses a standard 1%, 392-kΩ resistor.

4 Inductor Selection

Equation 2 is a calculation of the value of the output inductor, where Vout is the output voltage of the switcher. *Kind* is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high-inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Typically, the designer selects the inductor ripple value; however, Kind is typically in the range of 0.1 to 0.3 for the majority of applications.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{2}$$

For this design example, by using Kind = 0.3, the calculated inductor value is 2.9 µH. The chosen standard value was 3.3 µH for this design. For the output filter inductor, do not exceed the RMS current and saturation current ratings. Use Equation 3, Equation 4, and Equation 5 to find the inductor ripple current, RMS current, and peak inductor current.

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{3}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{4}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{5}$$

For this design, the inductor ripple current is 795 mA, the RMS inductor current is 3 A, and the peak inductor current is 3.4 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit, rather than the peak inductor current.

5 Output Capacitor Selection of the Switcher

Consider the three following primary requirements for selecting the value of the output capacitor of the switcher:

- Minimum capacitance to meet the load transient
- Minimum capacitance to meet the output voltage ripple
- Maximum ESR to meet the output voltage ripple

Select the output capacitor based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This is the situation if desired hold-up times occur for the regulator, where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs in the load current, such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the change in load current and output voltage to affect the control loop and adjust the duty cycle to react to the change. Size the output capacitor to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles, while allowing only a tolerable amount of droop in the output voltage. The minimum output capacitance required is determined by Equation 6.

$$Co > \frac{2 \times \Delta Iout}{fsw \times \Delta Vout} \quad (6)$$

where

- ΔIout is the change in output current
- fsw is the regulator switching frequency
- ΔVout is the allowable change in the output voltage

For this example, the transient load response is specified as a 5% change in Vout for a load step of 1 A. Using these numbers (ΔIout = 1 A and ΔVout = 0.05 × 2.16 = 108 mV) gives a minimum capacitance of 37 µF. This value does not take into account the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 7 calculates the minimum output capacitance required to meet the output voltage ripple specification.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \quad (7)$$

where

- fsw is the switching frequency
- Voripple is the maximum allowable output voltage ripple of the switcher output
- Iripple is the inductor ripple current calculated to be 795 mA

In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 7 yields 6.6 µF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR must be less than 38 mΩ.

$$Resr < \frac{Voripple}{Iripple} \quad (8)$$

The capacitance of a ceramic capacitor depends on the dc output voltage. Refer to the capacitor data sheet to select output capacitors based on their voltage rating. For the minimum capacitance that meets the load step specification of 37 µF, this example uses two effective 22-µF, 6.3-V, X5R ceramic capacitors with 4 mΩ of ESR.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Use an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the root mean square (RMS) value of the maximum ripple current. Equation 9 can calculate the RMS ripple current the output capacitor must support. For this application, Equation 9 yields 230 mA.

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \quad (9)$$

6 Input capacitor

The TPS54122 requires a high-quality ceramic, type X5R or X7R, 4.7 µF, input decoupling capacitor on the input voltage rail. In some applications, additional bulk capacitance may also be required for the LDO BIAS input. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54122. The input ripple current for this design, using Equation 10, is 1.35 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \quad (10)$$

The value of a ceramic capacitor varies significantly over both temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. The high capacitance-to-volume ratio and stability over temperature make the X5R and X7R ceramic dielectrics good selections for power-regulator capacitors. The capacitance value of a capacitor decreases as the dc bias across the capacitor increases. For this example design, a ceramic capacitor with at least a 10-V voltage rating is necessary to support the maximum input voltage. For this example, two 22-µF, 10-V capacitors connected to VIN and a 4.7-µF, 10-V capacitor at BIAS. The input capacitance value determines the input ripple voltage of the regulator. Use Equation 11 to calculate the input voltage ripple.

$$\Delta Vin = \frac{Iout\ max \times 0.25}{Cin \times fsw} \quad (11)$$

Using the design example values where Ioutmax = 3 A, C_{IN} = 50 µF, f_{SW} = 500 kHz, Equation 11 yields an input voltage ripple of 30 mV.

7 Input Capacitor of the LDO

Although an input capacitor is unnecessary for stability, connecting a 0.1-µF to 1-µF low equivalent series resistance (ESR) capacitor across the input supply near the LDO input pin is good analog design practice. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device location is several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability. This design example uses two 22-µF input capacitors.

8 Output Capacitor of the LDO

The internal LDO of the TPS54122 is stable with standard ceramic capacitors with capacitance values 4.7 µF or larger. Higher values are recommended for better noise performance. For best noise performance, the evaluated design uses 100-µF, 22-µF, and 0.1-µF ceramic capacitors with a 6.3-V rating. X5R- and X7R-type capacitors are excellent choices because they have minimal variation in value and ESR over temperature.

9 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This feature is useful if a load requires a controlled voltage slew rate. This feature is also useful if the output capacitance is large and requires a large amount of current to charge the capacitor to the output voltage level. The large currents required to charge the capacitor can make the TPS54122 reach the current limit, or the excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use Equation 12 to calculate the soft-start capacitor value.

$$Css = \frac{Tss(ms) * Iss(\mu A)}{Vref(V)} \quad (12)$$

The example circuit has the soft-start time set to an arbitrary value of 3.5 ms, which requires a 10-nF capacitor. In the TPS54122, Iss is 2.2 µA and Vref is 0.827 V.

10 Bootstrap Capacitor

Connect a 0.1-µF ceramic capacitor between the BOOT to PH pin for proper operation. Use a ceramic capacitor with X5R or better-grade dielectric. The capacitor must have 10 V or higher voltage rating.

11 Output Voltage Feedback Resistor Selection

Choose resistors R5 and R6 to set the output voltage of the switcher, and choose R1 and R2 to set the output voltage of the LDO. This example design uses 6.19 kΩ for R6 and 2.85 kΩ for R2. Use Equation 13 and Equation 14 to calculate R5 and R1.

$$R5 = \frac{Vout - Vref}{Vref} R6 \quad (13)$$

$$R1 = \frac{LDOVout - LDOVref}{LDOVref} R2 \quad (14)$$

where

- Vout is the output of the switcher
- LDOVout is for the LDO
- Vref is 0.827 V
- LDOVref is 0.8 V

The closest 1% resistors from the calculated results of Equation 13 and Equation 14 for R5 and R1 are 10 kΩ and 3.57 kΩ, respectively.

12 Switcher Minimum and Maximum Output Voltage

The internal design of the TPS54122 sets a minimum switcher output voltage limit for any given input voltage. The output voltage can never be less than the internal voltage reference; the minimum controllable on-time may limit the output voltage. In this case, Equation 15 gives the minimum output voltage:

$$Voutmin = Ontimemin \times Fsmax \times (Vinmax - Ioutmin \times 2 \times RDS) - Ioutmin \times (RL + RDS) \quad (15)$$

Where:

Voutmin = minimum achievable output voltage
Ontimemin = minimum controllable on-time (65 ns maximum)
Fsmax = maximum switching frequency including tolerance
Vunmax = maximum input voltage
Ioutmin = minimum load current
RDS = minimum high-side MOSFET on resistance (45 mΩ to 64 mΩ)
RL = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 16:

$$Voutmax = (1 - Offtimemax \times Fsmax) \times (Vinmin - Ioutmax \times 2 \times RDS) - Ioutmax \times (RL + RDS) \quad (16)$$

Where:

Voutmax = maximum achievable output voltage
Offtimemax = maximum controllable off-time (60 ns maximum)
Fsmax = maximum switching frequency including tolerance
Vinmin = mimimum input voltage
Ioutmax = maximum load current
RDS = maximum high-side MOSFET on resistance (81 mΩ to 110 mΩ)
RL = series resistance of output inductor

13 Compensation Component Selection

Several industry techniques can compensate dc-dc regulators. The method in this application report is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60° and 90°. This method ignores the effects of the slope compensation that is internal to the TPS54122. This method ignores the slope compensation; therefore, the actual crossover frequency is usually lower than the crossover frequency in the following calculations.

Type III compensation is used to achieve a high-bandwidth, high-phase-margin design. This design targets a crossover frequency (bandwidth) of 67 kHz. Equation 17 and Equation 18 calculate the power stage pole and zero at 2.5 kHz and 1809 kHz, respectively. For the output capacitance of the switcher (Cout), we must include the two input capacitors on the LDO; therefore, the total capacitance is 4 × 22 µF = 88 µF, and Resr = 4 mΩ / 4 = 1 mΩ.

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \tag{17}$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \tag{18}$$

Now the compensation components calculations are possible. First, calculate the value for R4, which sets the gain of the compensated network at the crossover frequency. Use Equation 19 to determine the value of R4.

$$R4 = \frac{2\pi \times fc \times Vout \times Cout}{gm_{ea} \times Vref \times gm_{ps}} \tag{19}$$

By using Equation 19, R4 = 22.1 kΩ.

Next, calculate the value of C8. Together with R4, C8 places a compensation zero at the dominant power-stage pole frequency f_p. Use Equation 20 to determine the value of C8:

$$C8 = \frac{Vout \times Cout}{Iout \times R4} \tag{20}$$

Using Equation 20, the standard value for C8 is 2.7 nF.

In order to provide a zero around the crossover frequency to boost the phase at crossover, add a capacitor (C11) parallel to R5. Equation 21 gives the value for the C11 capacitor. A close standard value for C11 is 330 pF.

$$C11 = \frac{1}{2\pi \times R5 \times fc} \tag{21}$$

Using the feedforward capacitor, C11, creates a low, ac-impedance path from the output voltage to the VSENSE input of the integrated circuit that can couple noise at the switching frequency into the control loop. Do not use a feedforward capacitor for high-output voltage ripple designs (greater than 15 mV peak-to-peak at the VSENSE input) operating at duty cycles of less than 30%. When using C11, always limit the closed-loop bandwidth to no more than one-tenth of the switching frequency.

Use an additional high-frequency pole, if necessary, to cancel the zero from the output capacitor ESR by adding a capacitor in parallel with the series combination of R4 and C8. Equation 22 calculates the pole that cancels the zero from the output capacitor ESR. Capacitor C6 is optional and not used in this design.

$$C6 = \frac{Resr \times Cout}{R4} \tag{22}$$

14 Noise-Reduction Capacitor

In most LDOs, the bandgap is the dominant noise source. If a noise-reduction capacitor (Cnr) is used with the TPS54122, the bandgap does not contribute significantly to noise. Instead, the output resistor divider and the error amplifier input dominate the noise. To minimize the noise in this application, use a 1-µF noise-reduction capacitor.

In addition to noise-reduction purposes, the capacitor on the NR pin slows start-up time. Changing the value of Cnr can adjust the start-up time of the LDO. In this design, the 1-µF noise-reduction capacitor sets the LDO start-up time to 1 s. For more detail on how to use this pin, see the TPS54122 data sheet.

15 Test Results

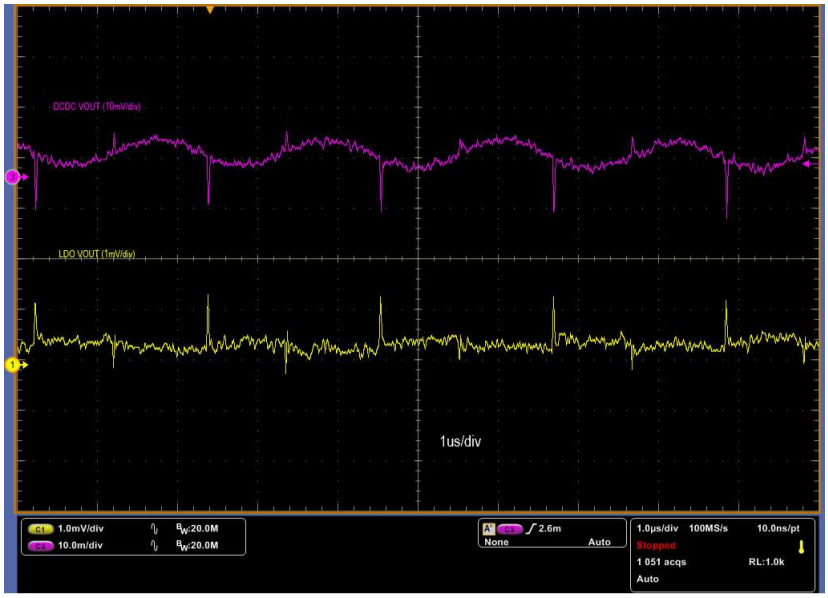

Figure 2. DC-DC VOUT (Vout) and LDO VOUT (LDOVout)
Where Vin = 5 V, Vout = 2.1 V, LDOVout = 1.8 V, Load = 1 A

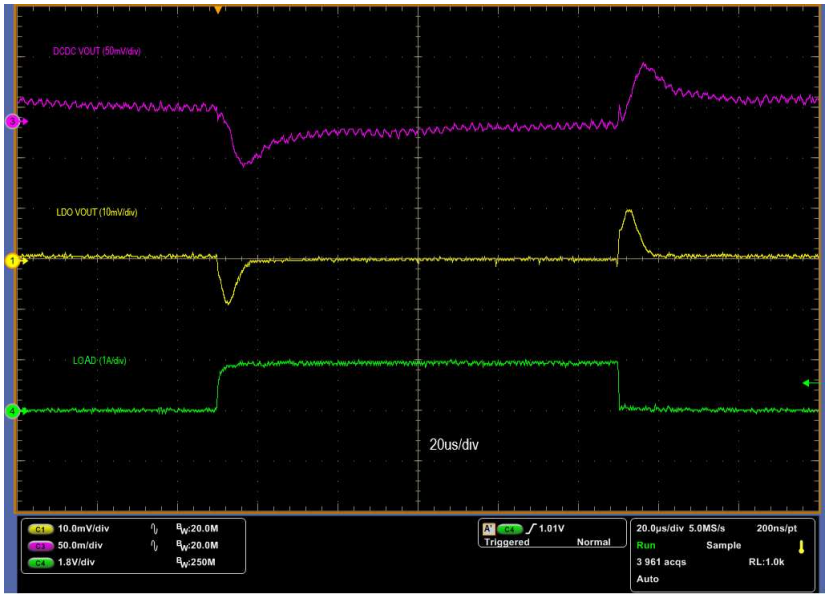

Figure 3. Transient Response
Where Vin = 5 V, Vout = 2.1 V, LDOVout = 1.8 V, Load = 1 A to 2 A

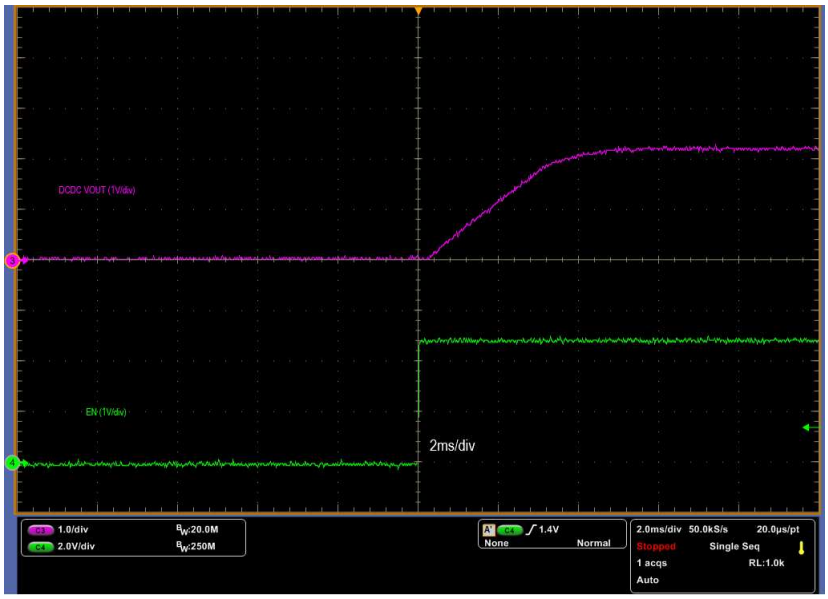

Figure 4. Start-Up Using DC-DC Enable (EN pin)
Where Vin = 5 V, Vout = 2.1 V, LDOVout = 1.8 V, Load = 1 A

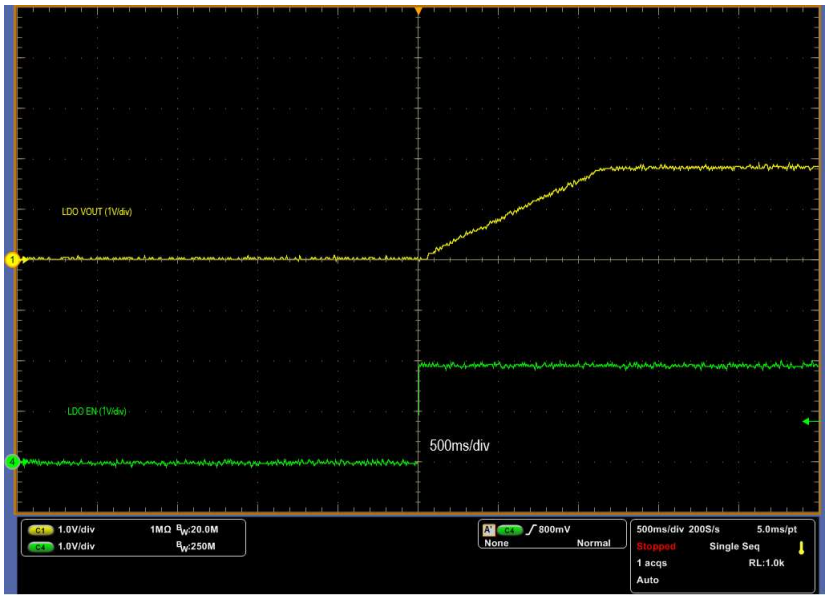

Figure 5. Start-Up Using LDO Enable (LDOEN pin)
Where Vin = 5 V, Vout = 2.1 V, LDOVout = 1.8 V, Load = 1 A

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