

# TPS65981, TPS65982, and TPS65986 Power and Data Role Swaps

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## ABSTRACT

Power and data role swaps allow individual devices to change their roles under certain conditions. This ability allows a power source to become a sink, a data DFP to become a data UFP, or both. The roles are negotiated using USB Power Delivery (PD) messaging according to the USB PD specification. This application report explains the standard implementation of data and power role swaps as well as assigning data and power preferences to individual USB Type-C ports. This application report is to be used with Texas Instruments TPS65981/2/6 family of USB Type-C and USB PD controllers and associated software tools.

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## 1 Introduction

The Power Delivery specification allows two connected dual-role ports to optionally switch their data role, their power role, or both roles using the power-role swap and data-role swap mechanisms.

Texas Instruments TPS65981, TPS65982, and TPS65986 families of USB Type-C and USB PD controllers can be configured to automatically initiate data or power role swaps to a desired state, or the same role swaps may be initiated by an external microcontroller through host interface commands. The control configuration (0x29) register is used to specify automatically initiated role swaps. You can specify a preferred data role by using the *Initiate Swap to DFP* command instead of the *Initiate Swap to UFP* command, and can configure the device to either allow or disallow swaps through the *Process Swap to DFP* and *Process Swap to UFP* bits. The power roles have similar settings.

Using an external microcontroller to modify data and power roles using host interface commands provides an additional level of functionality. Whereas the control configuration register provides a simple preference towards one setting or the other setting, an external microcontroller can use information gathered from the TPS65981, TPS65982, and TPS65986 host interface status registers to make more advanced power and data role decisions. For instance, a microcontroller could use the externally powered bit of the connection partner as stored in the Rx Source Capabilities (0x30) register to make a more informed decision when setting power role orientation.

## 2 Role Swap Configuration in Host Interface Registers

The TPS65982 registers include the following:

- Configuration registers:
  - 0x28, System Configuration register, *Port Info* field
  - 0x29, Control Configuration register, ALL fields
- Status registers:
  - 0x1A, Status register, *Port Role* and *Data Role* fields
  - 0x3F Power status register, *Source* or *Sink* field
  - 0x2D, Boot Status register, *Dead Battery* field
- Run-Time Host-Interface Commands:
  - SWSr, swap to source (power)
  - SWSk, swap to sink (power)
  - SWDF, swap to DFP (data)
  - SWUF, swap to UFP (data)

The Control Configuration register (0x29) is the primary register used to control role swap behavior. This register allows you to configure the initiation of role swaps, which causes the TPS6598x PD controller to automatically initiate the given role swap, and it allows you to configure the processing of role swaps, which controls whether the TPS65981/2/6 USB PD controller accepts or does not accept various role swap requests initiated by the port partner.

In addition to configuring system behavior in the Control Configuration register, you should be aware that the setting of the *Port Info* field of the System Configuration register also affects both the initiation and processing of role swaps.

The Status register (0x1a) reports the current data and power role of the system. The Boot Status register (0x2d) is also important as it reports whether or not the system is currently in Dead Battery Mode, and a system that is in Dead Battery Mode does not support power role swaps. Power status register (0x3F) can be used to look at power role easily.

Finally, four host interface commands can be used to manually initiate a data or power role swap using an external controller. As discussed in this application report, certain system conditions must still be met in order for a role swap to occur. If these conditions are not met, the host interface swap command is rejected.

### 3 Data and Power Role Swap Examples

The [TPS6598x Configuration Tool](#) contains multiple dual-role port configurations, all of which use one of two data and power role swap settings. Refer to the [TPS6598x Application-Customization Tool User Guide](#) to select the appropriate template that best represents your project configuration. Broadly speaking, there are two types of templates: "simplified" and "advanced". This document limits discussion to advanced templates to illustrate detailed functionality of power and data role swaps.

Note that the names of templates discussed below starts with the last portion of the file name that points to the version of the Configuration tool being used, which gets updated whenever a newer version of configuration tool is used. For example, template `TPS65982_HD3SS460_DRP_Host_Full_2_9.tpl` is for the TPS65982 device and was done based on configuration tool version 2.9.

The `TPS65982_HD3SS460_DRP_Host_Full_2_9.tpl` and `TPS65982_AlpineRidge_DRP_Host_Full_2_9.tpl` variants attempt a data role swap if necessary to become a data DFP (essentially a host). These projects do not initiate a power role swap, but accept any power swap request from a connected device.

The `TPS65982_HD3SS460_DRP_Source_Full_2_9.tpl` and `TPS65982_AlpineRidge_DRP_Source_Full_2_9.tpl` variants attempt a power role swap if necessary to become a power DFP (essentially a source). These projects does not initiate a data role swap, but accept any data swap request from a connected device.

Testing these two projects together always generates an automatic data role swap as the source variants have the try.SRC feature enabled, which ensures that when connected to a device that does not have try (SRC enabled), they always connect as a DFP.

The `TPS65982_HD3SS460_DRP_Host_Full_2_9.tpl` and `TPS65982_HD3SS460_DRP_Source_Full_2_9.tpl` can be accessed using the *New Project* option from the *Project* drop-down menu in the configuration GUI.

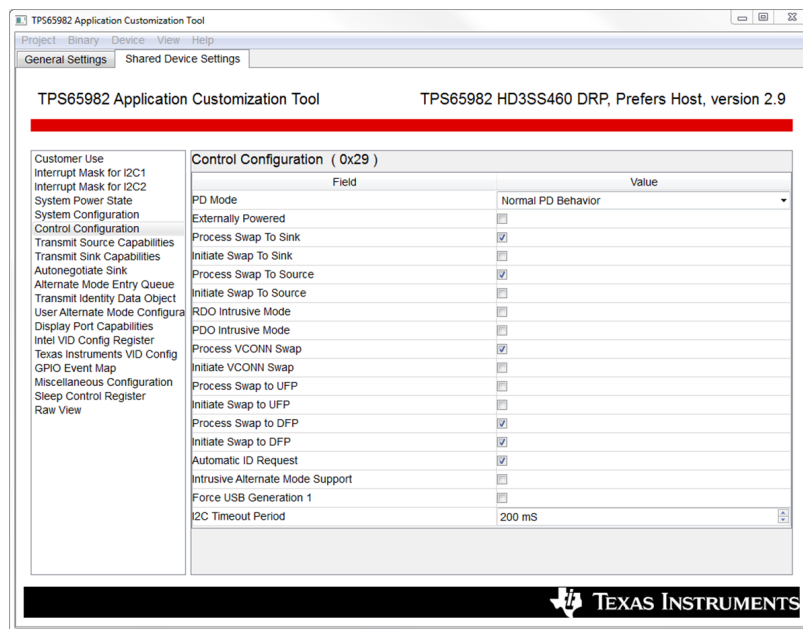


Figure 1. Control Configuration Settings Tab `TPS65982_HD3SS460_DRP_Host_Full_2_9.tpl`

Figure 1 shows the Control Configuration register (0x29) settings for the `TPS65982_HD3SS460_DRP_Host_Full_2_9.tpl` project. For this project, *Process Swap to Sink*, and *Process Swap to Source* are both enabled, but *Initiate Swap to Sink* and *Initiate Swap to Source* are both disabled. This indicates that the system accepts either power role swap request from a connected device but does not (automatically) initiate a power swap request of either type. This is an agnostic configuration since it supports both power roles without driving a preference towards one or the other.

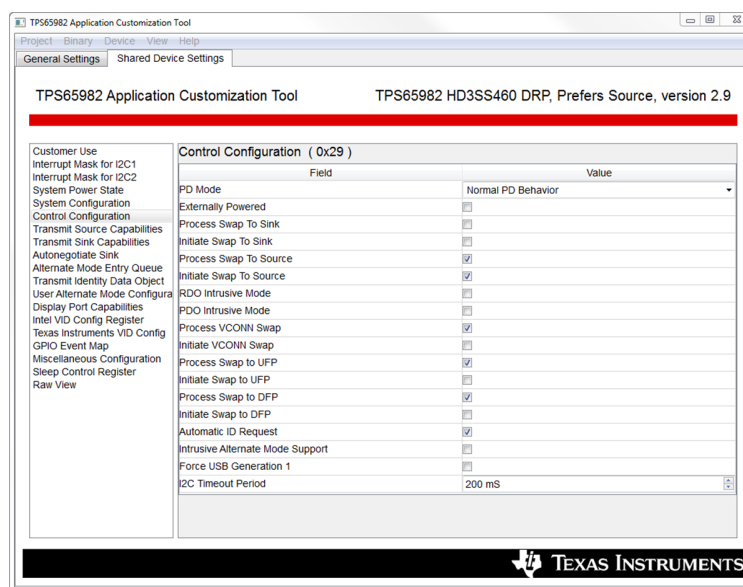
By contrast, the data role swap settings are as follows: *Initiate Swap to DFP* and *Process Swap to DFP* are both enabled, but *Initiate Swap to UFP* and *Process Swap to UFP* are both disabled. This combination indicates that the device always attempts to become the data DFP (host) in the connection.

**NOTE:** The *Swap to DFP* setting indicates that the device being configured swaps to become the DFP for both the *Initiate* and *Process* settings. This setting is a preferred data configuration because it drives the system towards a configuration in which the device is data DFP if possible.

When setting the initiate and process bits in the Control Configuration register, avoiding a configuration that could potentially lead to an infinite sequence of data or power role swaps is important. Firstly, a system should never be configured to initiate swaps in both directions (such as selecting *Initiate Swap to UFP* and *Initiate Swap to DFP* in the same configuration). Firstly, this would be a meaningless configuration because it provides no preference to data or power role and therefore is swapping seemingly for the sake of swapping, but secondly, if the port partner accepts swaps in both directions, this configuration would lead to an infinite series of swaps.

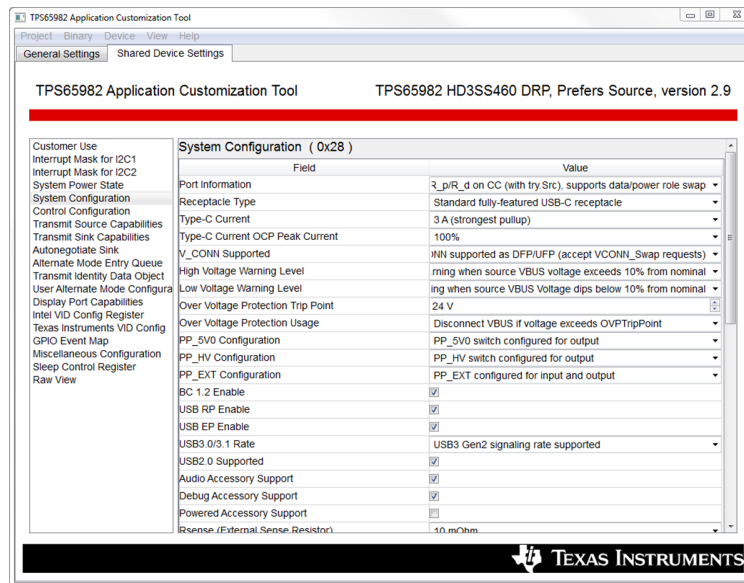
Likewise, any configuration that initiates a data or power role swap should not process swaps in the reverse direction. Two systems that are both configured to *Initiate Swap to DFP* and *Process Swap to UFP* toggle infinitely back and forth as each system continually initiates swaps to attempt to become DFP. In any event, a system that prefers to be configured as DFP would have no reason to accept swaps to UFP since this would require relinquishing the preferred role.

Comparing the settings of [Figure 1](#) to those of the *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* project as shown in [Figure 2](#), it is seen that the latter project is configured to drive towards a power source role by selecting *Process Swap to Source* and *Initiate Swap to Source*, and deselecting *Process Swap to Sink* and *Initiate Swap to Sink*. The data role is left agnostic by enabling the *Process* settings in both directions but disabling the *Initiate* settings.



**Figure 2. Control Configuration Settings Tab *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl***

Verifying that the *Port Information* field in the System Configuration register (0x28) is configured with a port behavior that supports data-role or power-role swaps as needed is required. [Figure 3](#) shows the System Configuration settings used in this template project that prefers to be a power source.



**Figure 3. System Configuration Settings Tab** *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl*

The following PD message trace was taken with a Teledyne LeCroy PD analyzer between two TPS65982 EVMs, one loaded with the *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* example and the other with *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl*. Because *TPS65982\_HD3SS460\_DRP\_Host\_Source\_2\_9.tpl* has the try.SRC feature enabled, the trace always follows this structure so long as either both boards are powered before connection or the board containing the source settings is powered with the host board in Dead Battery Mode. This trace was taken with both boards powered. This example also uses a non-e-marked cable, which leads to the cable resets and VConn Swap, which is discussed.

Packet	Direction	Msg Type	Cable Plug	Msg ID	Obj Cnt	Duration	Time	Time Stamp
4 Packets 38-41	→ CBL	PD Msg Vendor Defined	DFP or UFP	0	1	501.683 us	7.201 ms	1.584 508 000
42	← Left SRC	PD Msg Source Cap	DFP SRC	0	3	501.683 us	1.466 ms	1.627 009 000
44	→ Right SNK	PD Msg Request	UFP SNK	0	1	498.255 us	1.205 ms	1.625 475 000
46	← Left SRC	PD Msg Accept	DFP SRC	1	0	501.683 us	32.019 ms	1.594 990 000
49	← Left SRC	PD Msg PS Ready	DFP SRC	2	0	501.683 us	1.466 ms	1.627 009 000
51	→ Right SNK	PD Msg DR Swap	UFP SNK	1	0	498.255 us	1.205 ms	1.625 475 000
53	← Left SRC	PD Msg Accept	DFP SRC	3	0	501.683 us	1.389 ms	1.629 681 000
55	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.135 ms	1.631 070 000
56	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.132 ms	1.632 703 000
57	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.132 ms	1.634 333 000
58	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.209 ms	1.635 963 000
59	→ Right SNK	PD Msg VConn Swap	DFP SNK	2	0	498.255 us	1.195 ms	1.637 670 000
61	← Left SRC	PD Msg Accept	UFP SRC	4	0	501.683 us	2.329 ms	1.638 865 000
63	→ Right SNK	PD Msg PS Ready	DFP SNK	3	0	498.255 us	50.399 ms	1.641 194 000
65	→ CBL	Cable Reset				279.972 us	155.028 us	1.691 593 000
66	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.132 ms	1.692 028 000
67	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.131 ms	1.693 658 000
68	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.132 ms	1.695 287 000
69	→ CBL	PD Msg Soft Reset	DFP or UFP	0	0	498.255 us	1.213 ms	1.696 917 000
70	→ CBL	Cable Reset				279.972 us	10.243 ms	1.698 628 000

Figure 4. HD3SS460 DRP Host Connected to HD3SS460 DRP Source PD Trace (Excerpt)

Figure 4 shows the expected sequence of PD operations for this example. This sequence is only a partial trace. The system continues with a Discover Identity, Discover SVIDs/Modes, and mode entry.

1. Packets 01 through 37 (not displayed in Figure 4) — The EVM loaded with FW from *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* connects as the DFP and *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* connects as the UFP. This will always happen, so long as the EVM programmed with the source settings is powered, because these settings enable *try.SRC* and the host settings do not.
2. Packets 38 through 41 — A Discover Identity request and three retries are sent to the cable. Because it is a non-e-marked cable, there is no response.
3. Packets 42 through 49 — The PD power contract is negotiated. See Section 3 of this document for an explanation of the configuration of this stage of PD negotiation.
4. Packet 51 — The EVM configured with *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* makes a data role swap request. This occurs because *Initiate Swap to DFP* is enabled in the Control Configuration register of this project and it is currently the UFP. Additional conditions are required for this to occur, as shown in .
5. Packet 53 — The EVM configured with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* accepts the data role swap request. This occurs because *Process Swap to UFP* is enabled in the Control Configuration register of this project and it is currently the DFP. Additional conditions are required for this to occur, as listed in Table 1.
6. Packets 55 through 58 — The EVM configured with *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* issues a soft reset command to the cable with three retries. The new DFP always attempts a soft reset to the cable following a data-role swap to reset the message ID to 0. The cable used in this example does not respond because it is not e-marked.
7. Packet 59 — the EVM configured with *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* issues a

VConn swap. The PD spec requires that a PD port must provide power to the connection cable in order to issue a cable reset. This VConn swap request is preliminary to the cable reset of packet 65.

8. Packets 61 and 63 — The VConn swap is accepted and then the EVM configured with *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* issues a *PS Ready* command when it is providing power to the cable.
9. Packets 65 through 70 — The host-configured port issues a *Cable Reset* command. Because the cable is not e-marked, it does not return a *Good CRC* message to this *Cable Reset* (all *Good CRC* messages have been removed from this trace to reduce its size). When no *Good CRC* message is received from the cable, the DFP (host) issues one soft reset and three retries to the cable as a result of not receiving *Good CRC* for the soft reset request. After four *Soft Reset* requests with no *Good CRC*, the port issues one final *Cable Reset* and then continues with the rest of its PD negotiation (not shown).

#### 4 Requirements for Data and Power Role Swaps

A number of conditions must be met for the TPS6598x USB PD controller to issue or accept a power or data role swap. If a swap request is not issued or accepted as you expects, these conditions should be checked.

[Table 1](#) summarizes the requirements for each type of swap to be issued or accepted. The combination of conditions in the *Required Conditions* column must be met as specified in the table for the swap to occur. If any of the conditions in the *Blocking Conditions* column are met, the swap does not occur.

**Table 1. Data-Role and Power-Role Swap Requirements**

ACTION	TYPE	REQUIRED CONDITIONS	BLOCKING CONDITIONS
Issue swap to source	Power	Port is currently a Sink AND Initiate Swap to Source == 1 OR SWSr 4CC command issued	A previous swap-to-source request was NAK'd by the far-end PD port controller. Dead Battery flag is set in the Boot Status register (0x2D). The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Accept swap to source	Power	Port is currently a Sink AND Process Swap to Source == 1	The <i>Port Information</i> field in the System Configuration register does not support PR swap. Dead Battery flag is set in Boot Status register (0x2D).
Issue swap to sink	Power	Port is currently a Source AND Initiate Swap to Sink == 1 OR SWSk 4CC command issued	A previous swap-to-sink request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Accept swap to sink	Power	Port is currently a Source AND Process Swap to Sink == 1	The <i>Port Information</i> field in the System Configuration register does not support PR swap.
Issue swap to DFP	Data	Port is currently a UFP (Device) AND Issue Swap to DFP == 1 OR SWDF 4CC command issued	A previous swap-to-DFP request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support DR swap. An Alternate Mode is Active (has been entered and not exited). A Source or Sink Capabilities message has been received from port partner that does not have Dual Role Data bit set.
Accept swap to DFP	Data	Port is currently a UFP (device) AND Process Swap to DFP == 1	The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is Active (has been entered and not exited).
Issue swap to UFP	Data	Port is currently a DFP (Host) AND Initiate Swap to UFP == 1 OR SWUF 4CC command issued	A previous Swap to UFP request was NAK'd by the far-end PD port controller. The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is active (has been entered and not exited). A source or sink capabilities message has been received from port partner that does not have Dual Role Data bit set.
Accept swap to UFP	Data	Port is currently a DFP (Host) AND Process Swap to UFP == 1	The <i>Port Information</i> field in the System Configuration register does not support DR. An Alternate Mode is Active (has been entered and not exited).

## 5 Verification of Data-Role and Power-Role Swaps

The first step in verification of the data-role and power-role swaps is to verify that the settings read from the device match those that were input into the configuration tool. The relevant settings are stored in the Control Configuration register (0x29) and the System Configuration register (0x28). These settings can be modified at runtime by an external microcontroller and therefore ensuring that the settings read as expected is useful.

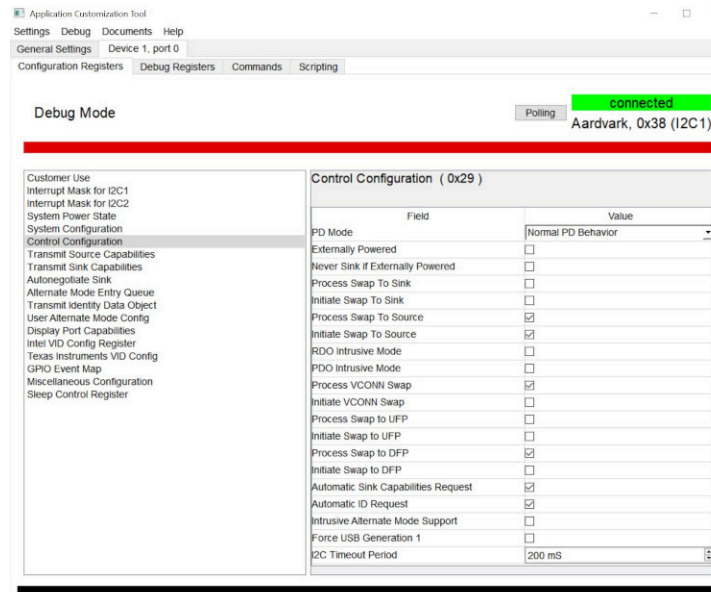


Figure 5. Control Configuration Register *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl*

The settings shown in [Figure 5](#) are verified to match those of the configuration tool as shown in [Figure 2](#). Even when this is the case, you may find cases where swaps do not occur as expected. This section provides two common examples (see [Section 5.1](#) for example 1 and [Section 5.2](#) for example 2) and a walkthrough of a typical debug procedure for these scenarios using the [TPS6598x Configuration Tool](#).

### 5.1 Example 1: Debugging Power Role Swap Exiting Dead Battery Mode Operation

For the first experiment, use the two TPS65982 EVMs programmed with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* and *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* settings from the earlier example. The *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* EVM is left unpowered, while the *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* EVM is powered.

As shown in [Figure 6](#), no power-role swap is initiated by the *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* system, even though it is a sink and has *Initiate Swap to Source* enabled.

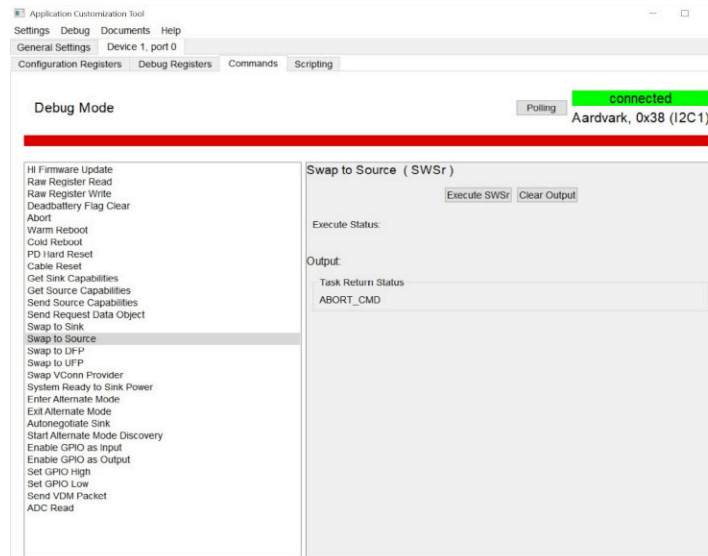


Packet	Direction	DR	PR	Msg ID	Obj Cnt	Msg Type	DR	PR	Msg ID	Obj Cnt	Cmd	Cmd Type	Obj Pos	Vendor ID	Duration	Time	Time Stamp				
32	Right	SRC	DFP	0	2	Source Cap	DFP	SRC	0	2	Fixed	Max Cur	Voltage	Dual Role	3.00 A	5.00 V	1	3.00 A	12.00 V	0	765.776
34	Left	SNK	UFP	0	1	Request	UFP	SNK	0	1	Request	Max Opr Cur/Pow	Opr Cur/Pow	Cap Mismatch	0	0	1	3.00A / 75.00W	3.00A / 75.00W	0	636.363 us
36	Right	SRC	DFP	1	0	Accept	DFP	SRC	1	0					498.256 us	30.947 ms	3 . 001 526 000				
38	Right	SRC	DFP	2	0	PS Ready	DFP	SRC	2	0					498.256 us	11.433 ms	3 . 032 473 000				
40	Right	SRC	DFP	3	1	Vendor Defined	DFP	SRC	3	1	VDM Header	Discover Identity	Initiator	0	PD SID			632.016 us			
42	Left	SNK	UFP	1	4	Vendor Defined	UFP	SNK	1	4	VDM Header	Discover Identity	Resp ACK	0	PD SID	ID Header	Texas				
44	Right	SRC	DFP	4	1	Vendor Defined	DFP	SRC	4	1	VDM Header	Discover SVIDs	Initiator	0	PD SID			632.016 us			
46	Left	SNK	UFP	2	3	Vendor Defined	UFP	SNK	2	3	VDM Header	Discover SVIDs	Resp ACK	0	PD SID	SVIDs	SVID 0	Display Port			
48	Right	SRC	DFP	5	1	Vendor Defined	DFP	SRC	5	1	VDM Header	Discover Modes	Initiator	0	Display Port			632.016 us			
50	Left	SNK	UFP	3	2	Vendor Defined	UFP	SNK	3	2	VDM Header	Discover Modes	Resp ACK	0	Display Port	DP Cap	Port C	UFP			
52	Right	SRC	DFP	6	1	Vendor Defined	DFP	SRC	6	1	VDM Header	Discover Modes	Initiator	0	Texas Instruments			632.016 us			
54	Left	SNK	UFP	4	2	Vendor Defined	UFP	SNK	4	2	VDM Header	Discover Modes	Resp ACK	0	Texas Instruments	Modes	0				
56-119	Right	CBL	DFP or UFP	0	1	Vendor Defined	DFP or UFP	0	1	1	VDM Header	Discover Identity	Initiator	0	PD SID			632.016 us	113.876		
120	Right	SRC	DFP	7	1	Vendor Defined	DFP	SRC	7	1	VDM Header	Enter Mode	Initiator	1	Display Port			632.016 us			
122	Left	SNK	UFP	5	1	Vendor Defined	UFP	SNK	5	1	VDM Header	Enter Mode	Resp ACK	1	Display Port			636.363 us			
124	Right	SRC	DFP	0	2	Vendor Defined	DFP	SRC	0	2	VDM Header	DP Status (0x10)	Initiator	1	Display Port	DP Status	DF				
126	Left	SNK	UFP	6	2	Vendor Defined	UFP	SNK	6	2	VDM Header	DP Status (0x10)	Resp ACK	1	Display Port	DP Status	UFP				
128	Right	SRC	DFP	1	2	Vendor Defined	DFP	SRC	1	2	VDM Header	DP Configure (0x11)	Initiator	1	Display Port	DP Config					
130	Left	SNK	UFP	7	1	Vendor Defined	UFP	SNK	7	1	VDM Header	DP Configure (0x11)	Resp ACK	1	Display Port			632.016 us			
132	Right	SRC	DFP	2	2	Vendor Defined	DFP	SRC	2	2	VDM Header	Enter Mode	Initiator	1	Texas Instruments	Undefined	0x				
134	Left	SNK	UFP	0	1	Vendor Defined	UFP	SNK	0	1	VDM Header	Enter Mode	Resp ACK	1	Texas Instruments			636.363 us			
136	Right	SRC	DFP	3	2	Vendor Defined	DFP	SRC	3	2	VDM Header	SVID Specific Cmd (0x14)	Initiator	1	Texas Instruments						
138	Left	SNK	UFP	1	2	Vendor Defined	UFP	SNK	1	2	VDM Header	SVID Specific Cmd (0x14)	Resp ACK	1	Texas Instruments						

Figure 6. PD Flow With DRP Source Unpowered

If the system settings have been verified, but a data-role or power-role swap is not occurring as expected, initiate the role swap manually through the [TPS6598x Configuration Tool](#).

Because the *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* EVM is not issuing the expected swap request, attach the HW adapter (USB-to-I2C) for the [TPS6598x configuration tool](#) to this EVM and issue the SWSr command.

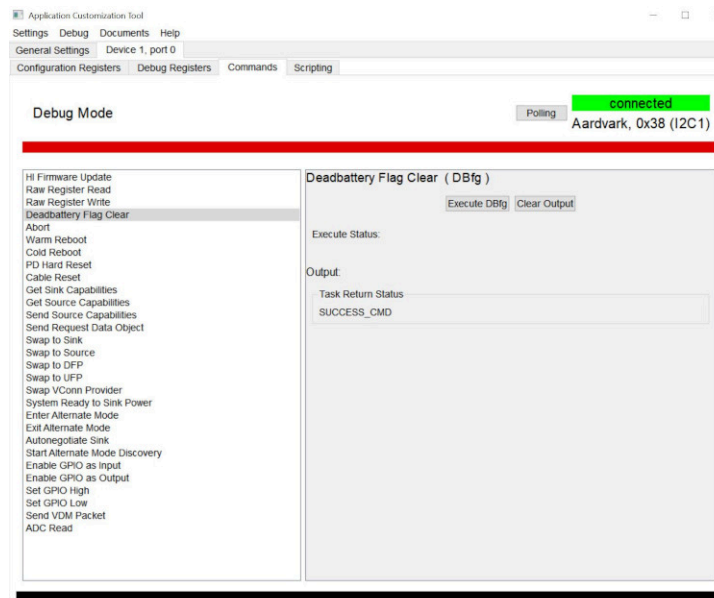


**Figure 7. Failed SWSr When Dead Battery flag is Set to 1 (True)**

Figure 7 shows the feedback from the host interface tools. The tool reports that the SWSr command was aborted. You can read Boot flags register (0x2D) to check if the Dead Battery Flag is set.

To correct this, you can power the board and then issue the DBfg command from the host interface which clears the Dead Battery flag as shown in Figure 8. Clearing of the Dead Battery flag should also be verified by reading the Boot Status register (0x2D) as shown in Figure 9.

The board must be powered before clearing the Dead Battery flag otherwise the device resets and reboots again in Dead Battery Mode operation.



**Figure 8. Successful DBfg Command to Clear Dead Battery Flag**

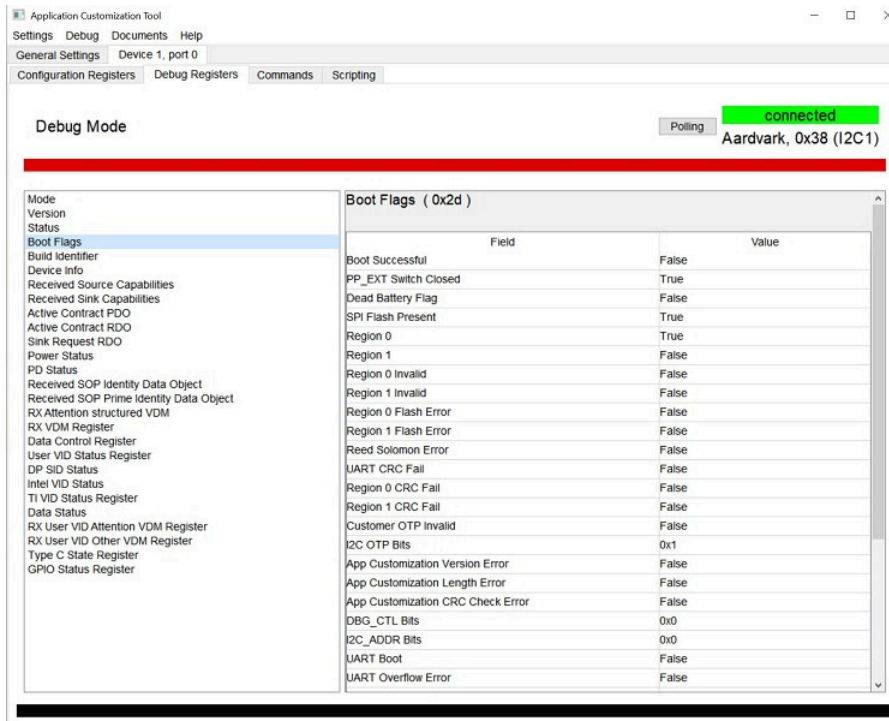


Figure 9. Verified Dead Battery flag Cleared to 0 (False)

When the Dead Battery flag has been cleared, the EVM programmed with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* can be swapped to the power source by issuing the SWSr host interface command as shown in Figure 10.

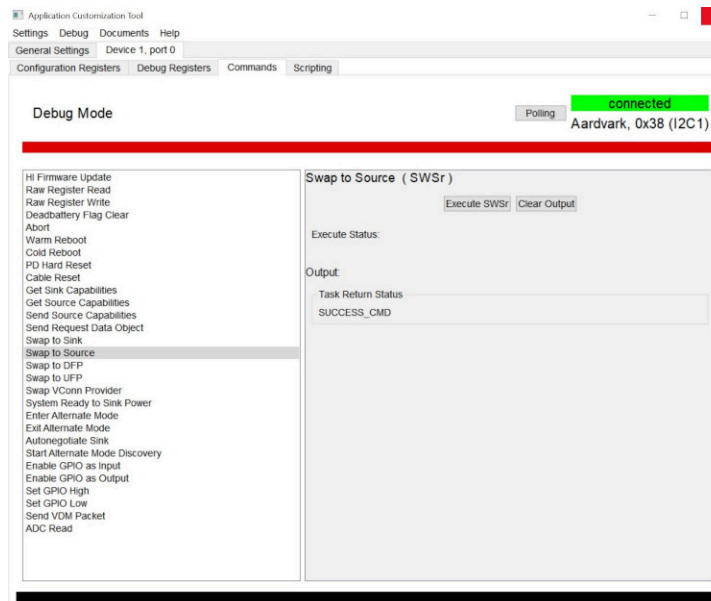


Figure 10. Successful Swap to Source

## 5.2 Example 2: Debugging Swap Reversal from non-Persistent Swap Conditions

Using the TPS65982 EVMs programmed with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* and *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* settings from the earlier example, the host interface tools may be used to issue a power-role swap.

Taking the lesson learned from [Section 5.1](#), power both EVMs and then connect. The PD flow should be as was already shown in [Figure 4](#). The end state of this system is that the *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl* EVM is the power source and the *TPS65982\_HD3SS460\_DRP\_Host\_Full\_2\_9.tpl* EVM is the data host.

As a next step, use the host interface tool to issue a *Swap to Sink* PD message to the port partner.

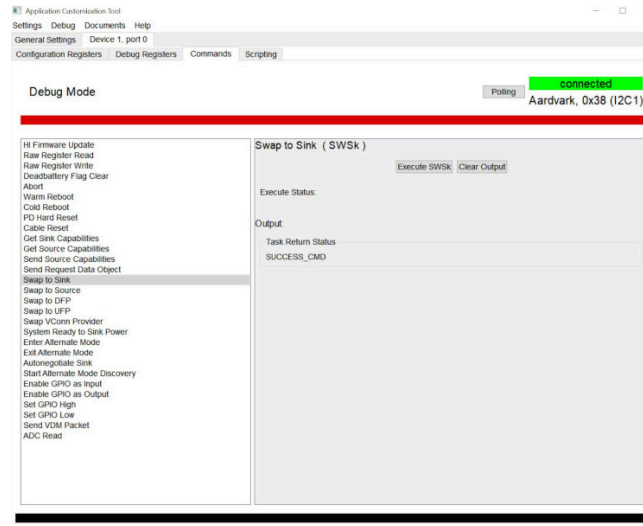


Figure 11. SWSk Command Page Before Execution

[Figure 11](#) shows the command page for the SWSk (swap to sink) host interface command. The tools are attached to the EVM that has been configured with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl*, which always comes up as the power source in this example because it has the *try.SRC* feature enabled.

Before issuing SWSk, the PD Status register, displayed at the bottom of the command page, shows that the system is currently the power source (*Source-Sink* field).

After pressing the *Execute Function* button, the tool indicates a successful execution as shown in [Figure 12](#); however, the PD Status register still indicates that the device is the power source, just as it was before issuing the SWSk command. This scenario is referred to as a *swap reversal* which is an accidental scenario that arises from configuring the TPS65982 device with non-persistent swap conditions.

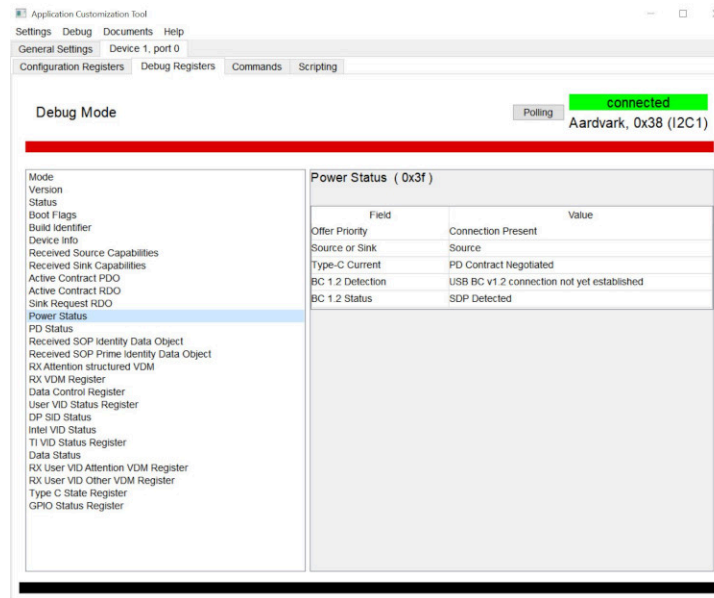


Figure 12. SWSk Power-Role Swap to Sink Attempt (Inconclusive Result)

As shown in Figure 12, the host interface tool reports a successful completion of the *Swap to Source* command, but the Power Status register reports that the device is still a source. The reason that the device is still a source after a *Swap to Sink* command that is reported as successful is shown in Figure 13. This PD capture is started at the point in which the SWSk command is issued from the host interface tool. The trace shows that, in fact, a successful *Swap to Sink* PD message sequence operation does occur (packets 1 through 15); however, the system immediately issues another swap request. The reason is shown by revisiting the Control Configuration register on the device programmed as *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl*.

PD	Packet	Direction	Role	Msg Type	DR	PR	Msg ID	Obj Cnt	Duration	Time	Time Stamp											
PD	Packet 1	Left	SRC	PD Msg	PR Swap	UFP	SRC	6	501.653 us	1.208 ms	17.943 041 000											
PD	Packet 3	Right	SNK	PD Msg	Accept	DFP	SNK	5	496.256 us	32.400 ms	17.944 249 000											
PD	Packet 5	Right	SNK	PD Msg	PS Ready	UFP	SNK	7	494.949 us	2.647 ms	17.976 649 360											
PD	Packet 7	Left	SRC	PD Msg	PS Ready	DFP	SRC	6	498.256 us	25.806 ms	17.979 296 000											
PD	Packet 9	Left	SRC	PD Msg	Source Cap	DFP	SRC	0	Fixed	3.00 A, 5.00 V	Fixed	3.00 A, 12.00 V	765.776 us, 1.633 ms									
PD	Packet 11	Right	SNK	PD Msg	Request	UFP	SNK	0	Request	3.00A / 75.00W, 3.00A / 75.00W	Cap Mismatch	0	Obj Pos	1	Duration	636.363 us	Time	1.337 ms	Time Stamp	18.000 000 000		
PD	Packet 13	Left	SRC	PD Msg	Accept	DFP	SRC	1	498.256 us	30.952 ms	18.008 074 000											
PD	Packet 15	Left	SRC	PD Msg	PS Ready	DFP	SRC	2	498.256 us	1.403 ms	18.039 026 000											
PD	Packet 17	Right	SNK	PD Msg	PR Swap	UFP	SNK	1	503.322 us	1.205 ms	18.040 429 000											
PD	Packet 19	Left	SRC	PD Msg	Accept	DFP	SRC	3	498.256 us	31.547 ms	18.041 634 000											
PD	Packet 21	Right	SNK	PD Msg	PS Ready	DFP	SNK	4	491.568 us	2.626 ms	18.073 181 344											
PD	Packet 23	Left	SRC	PD Msg	PS Ready	UFP	SRC	2	501.653 us	5.394 ms	18.075 807 000											
PD	Packet 25	SP <sup>1</sup>	CBL	PD Msg	Soft Reset	DFP or UFP	0	0	501.653 us	1.137 ms	18.081 201 000											
PD	Packet 26	SP <sup>1</sup>	CBL	PD Msg	Soft Reset	DFP or UFP	0	0	501.653 us	1.137 ms	18.082 840 000											
PD	Packet 27	SP <sup>1</sup>	CBL	PD Msg	Soft Reset	DFP or UFP	0	0	501.653 us	1.136 ms	18.084 479 000											
PD	Packet 28	SP <sup>1</sup>	CBL	PD Msg	Soft Reset	DFP or UFP	0	0	501.653 us	1.274 ms	18.086 119 000											
PD	4 Packets 29-32	SP <sup>1</sup>	CBL	PD Msg	Vendor Defined	DFP or UFP	1	1	VDM Header	Discover Identity	Cmd Type	Initiator	Obj Pos	0	Vendor ID	PD SID	Duration	638.442 us	Time	27.812 ms	Time Stamp	18.087 895 000
PD	Packet 33	Left	SRC	PD Msg	Source Cap	UFP	SRC	0	Fixed	3.00 A, 5.00 V	Fixed	3.00 A, 12.00 V	0	Fixed	3.00 A, 20.00 V	0	Fixed	3.00 A, 12.00 V	0	Fixed	3.00 A, 20.00 V	0
PD	Packet 35	Right	SNK	PD Msg	Request	DFP	SNK	0	Request	3.00A / 75.00W, 3.00A / 75.00W	Cap Mismatch	0	Obj Pos	3	Duration	632.016 us	Time	1.337 ms	Time Stamp	18.100 000 000		
PD	Packet 37	Left	SRC	PD Msg	Accept	UFP	SRC	1	501.653 us	32.020 ms	18.118 846 000											
PD	Packet 39	Left	SRC	PD Msg	PS Ready	UFP	SRC	2	501.653 us	18.150 866 000												

Figure 13. PD Trace of Manual Power-Role Swap Followed by Automatic Power-Role Swap

Referring back to Figure 5, recall that the source device has the *Initiate Swap to Source* setting enabled. The behavior of this setting is that it initiates a *Swap to Source* request at any time that the device is a sink and none of the blocking conditions of Table 1 are present. So, in this system, when the manual swap requests swaps power roles, the *Initiate Swap to Source* setting immediately swaps the power role back. In fact, any number of *Swap to Sink* requests are immediately swapped back as long as this setting is enabled.

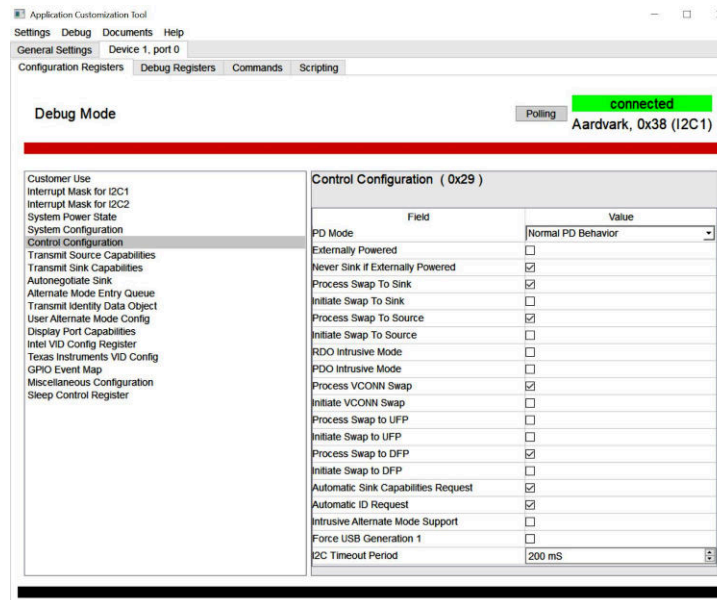


Figure 14. TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl With *InitSwapToSource* Disabled

A simple means of completing this test is to use the host interface tools to disable *Initiate Swap to Sink* in the Control Configuration register (0x29) of the EVM that has been configured with *TPS65982\_HD3SS460\_DRP\_Source\_Full\_2\_9.tpl*.

**NOTE:** Register changes made with the host interface tools are made only in the device RAM, not the system FLASH, and will therefore be reset back to their default values if there is a device reset or power cycle.

Do not forget to click the *Write Register* button after making this change.

The *Process Swap to Sink* field does not need to be enabled for the SWSk command to work properly. This field is only used to evaluate swap requests that are initiated by the port partner.

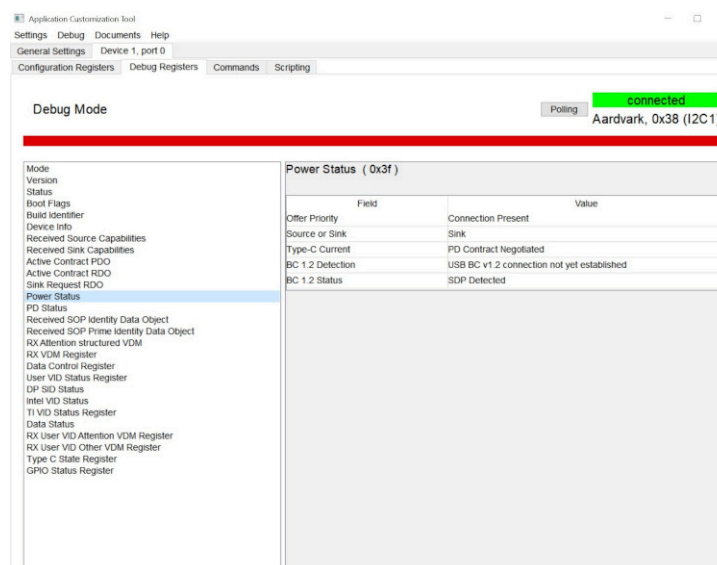


Figure 15. Manual Swap to Sink (Successful and Persistent)

Figure 15 shows the successful completion of the SWSk host interface command after disabling *Initiate Swap to Source* field in Control Configuration register (0x29). The Power Status register now shows the device is the power sink in the connection.



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