PR424
TMS320VC550x Design 7

FEATURES:

- Provides sequenced core and I/O voltages from input voltages from 3.3 V to 5.0 V.
- /RESET delay fixed at 80 ms minimum, 120 ms typical.
- The current draw on the input power supply is minimized by sequencing the core rail first and then the I/O rail.

IMPORTANT WEB LINKS:

- Link to the TI power management home page at http://power.ti.com then select the TI DSP Solutions link for more information and other reference designs.
- Link to datasheets at:
  - http://focus.ti.com/lit/ds/symlink/tps70202.pdf
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.

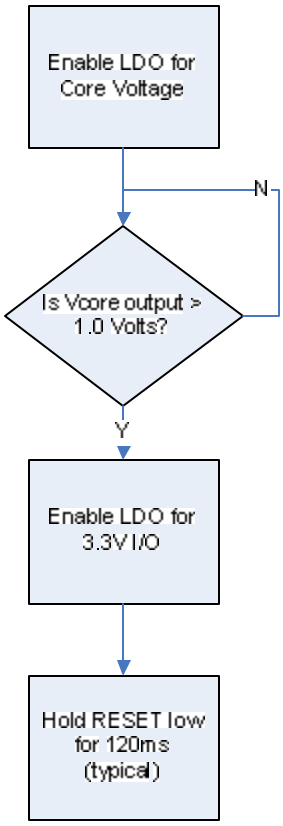
THEORY OF OPERATION:

PR424 uses a TPS70202 dual linear regulator to regulate the input voltage down to the I/O and core voltages.

CIRCUIT LIMITATIONS AND CAPABILITIES:

The TPS70202 is capable of supplying 500 mA of Core current and 250 mA of I/O current. The power dissipation and thus the temperature rise of the TPS70202 is dependant on the output currents and the input voltage. With a 1.2 V core voltage at 250 mA, an I/O voltage of 3.3V at 250 mA and a 5.0 V input, the power dissipation of the TPS70202 would be 2.325 Watts. Depending on board layout and ambient temperature, this power dissipation may raise the junction temperatures above the TPS70202 maximum. A thermal analysis should be performed when drawing large currents or high input voltages are used.

POWER UP SEQUENCING:



The circuit will start to ramp up the I/O voltage immediately after the core voltage is above about 1.0V. The 1.0V limit will vary with the characteristics of the transistor used for the sequencing circuit. Some systems may require a longer time delay between the core and I/O voltage applications. A capacitor can be added between the base of Q1 and ground to slow the turn on of the I/O voltage. The turn on time would be delayed by the RC time constant created by R3 and the added capacitor.

The sequencing circuits can be removed if sequencing is not required. Components R1, R3, and Q1 can all be removed. EN2 can be tied to EN1 or left as an independent enable if desired. This will not effect the minimum duration of the RESET signal.

IMPLEMENTATION NOTES:

- **Component selection:**
  - If different capacitors are used for C3 and C4 than recommended per the BOM, they must meet the ESR requirements per the TPS70202 datasheet.

WAVEFORMS:

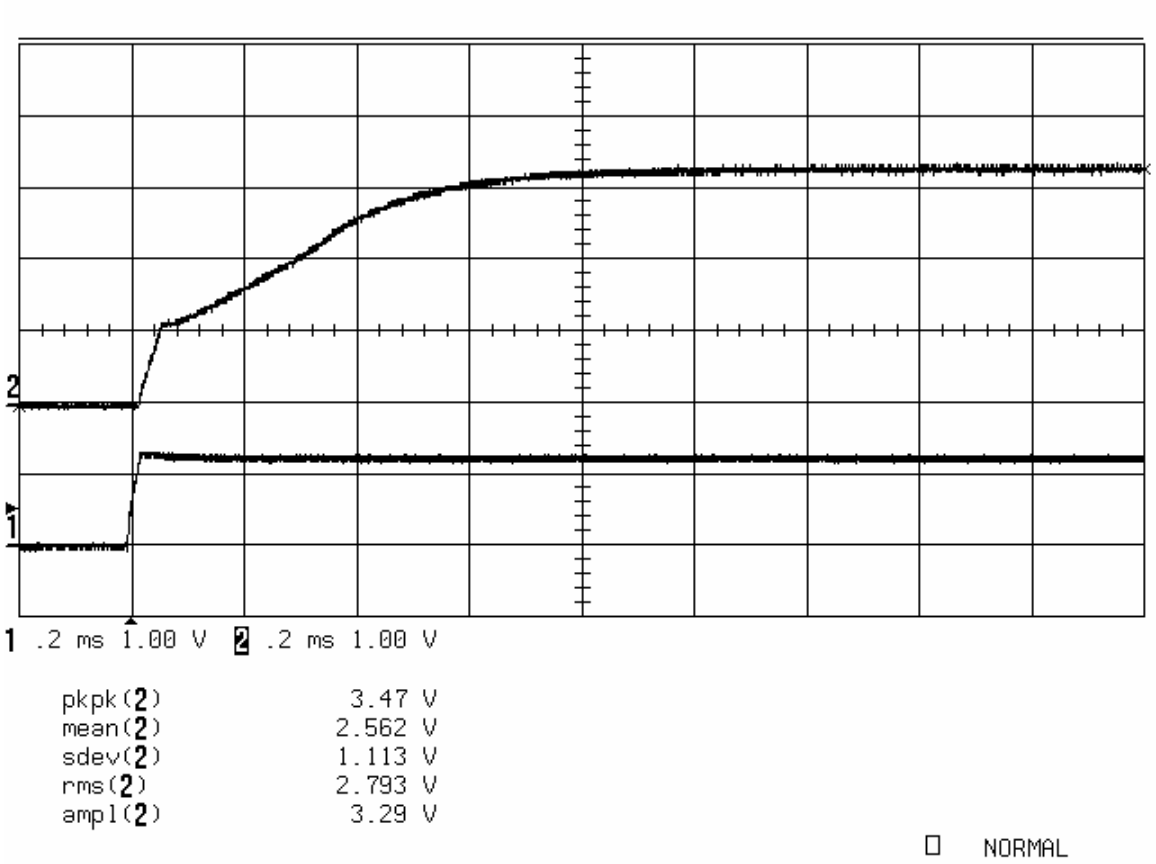


Figure 1 - Power up with V_{IN} = 3.6 V, Vcore=1.2 @ 110 mA, Vi/o = 3.3V @ 50 mA

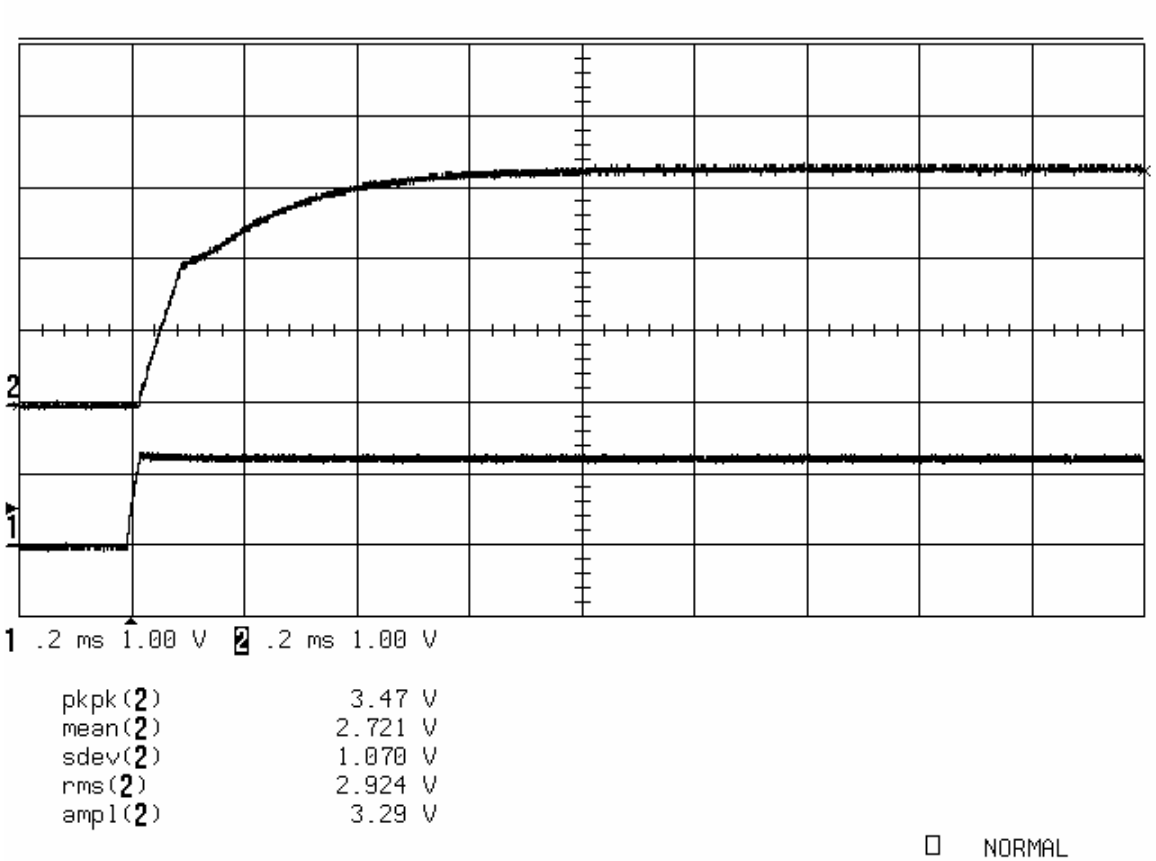


Figure 2 - Power up from Enable when V_{IN} = 3.6 V, Vcore=1.2 @ 110 mA, Vi/o = 3.3V @ 50 mA

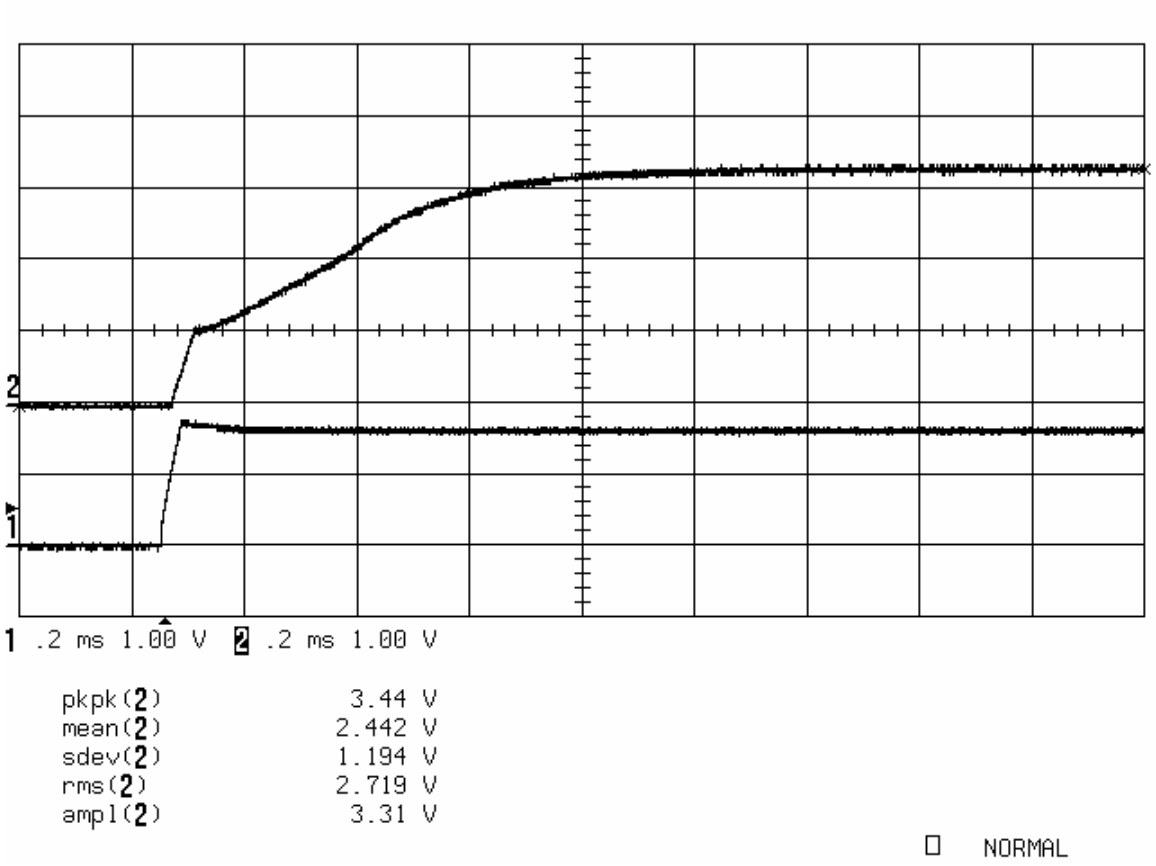


Figure 3 - Power up with V_{IN} = 3.6 V, Vcore=1.6 @ 267 mA, Vi/o = 3.3V @ 70 mA

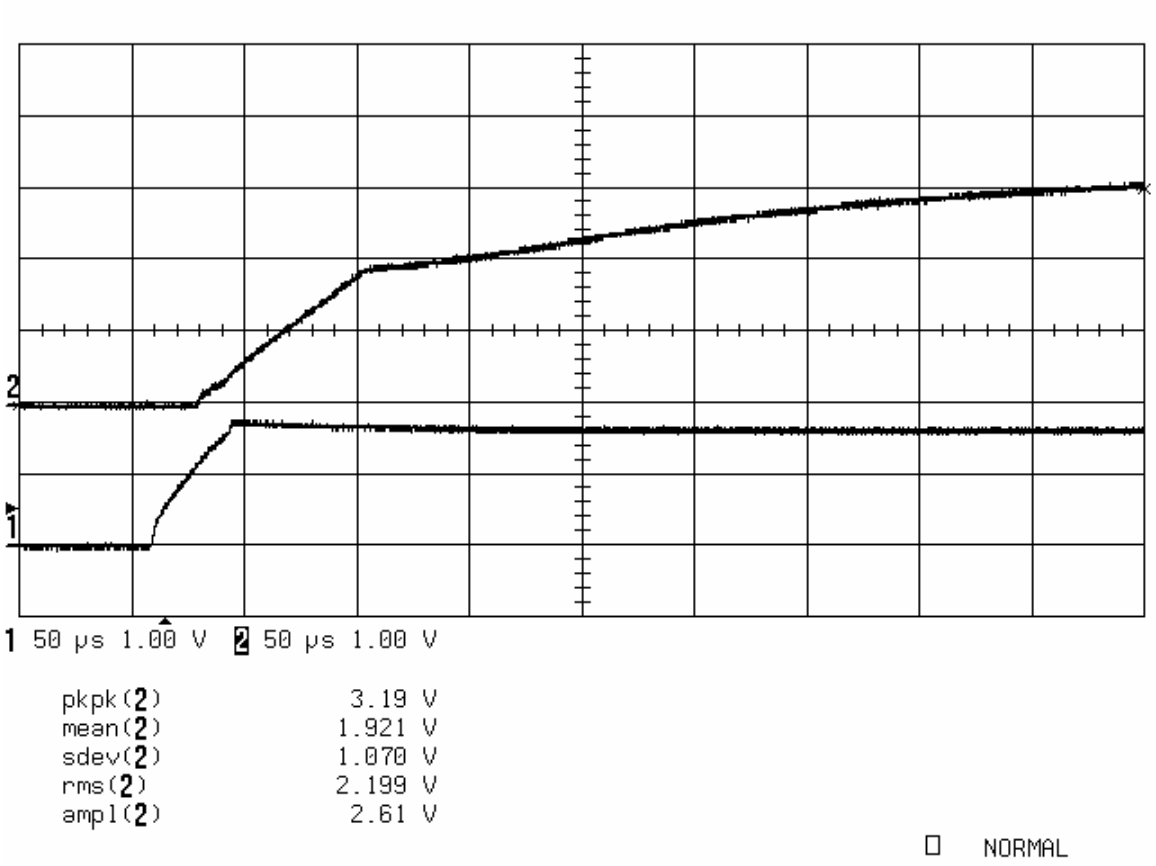


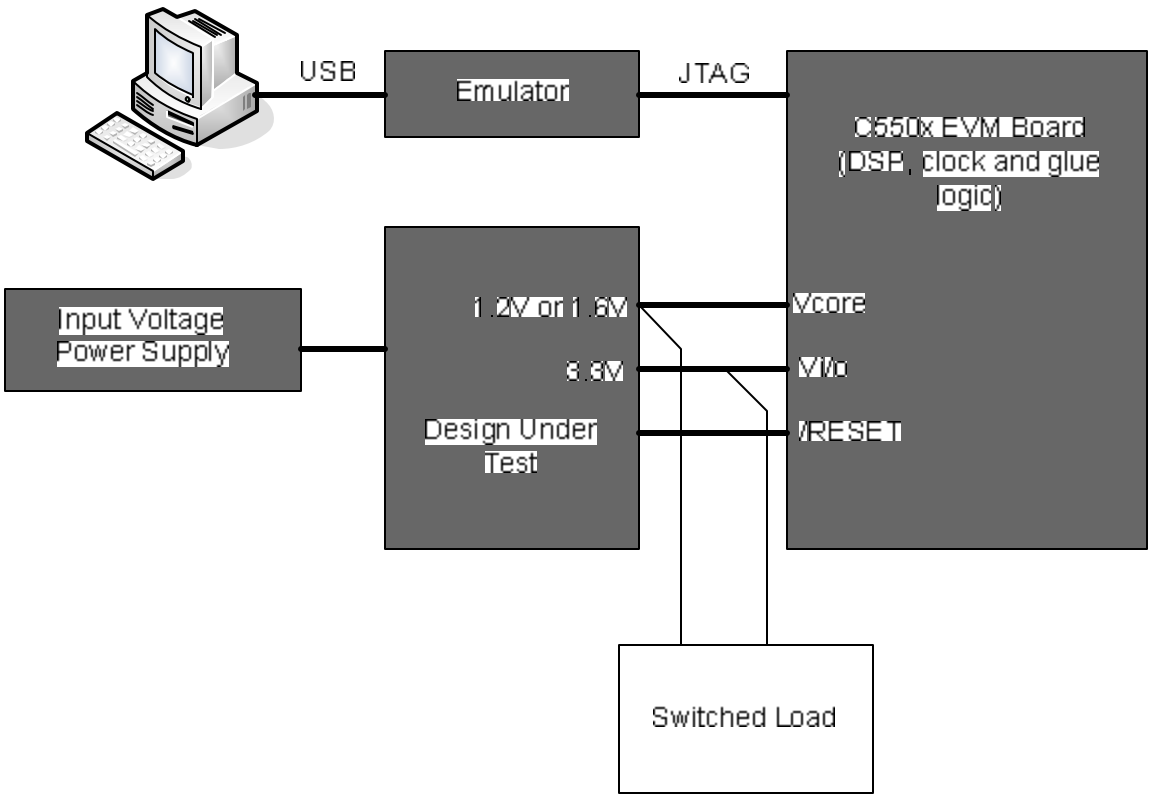
Figure 4 - Power up from Enable when V_{IN} = 3.6 V, Vcore=1.6 @ 267 mA, Vi/o = 3.3V @ 70 mA

TESTING METHOD:

The solution was tested on the bench and in an actual DSP circuit. Bench testing included start up into full DSP load, switched load from no load to full DSP load, and power up sequencing. The full DSP load is defined as the current draw a C550x DSP would present to the power supply under worst operating conditions. This full DSP load current is heavily dependent on board layout, firmware configurations, DSP clock speed, and core voltage. For testing purposes, the following values were assumed to be the full DSP load current.

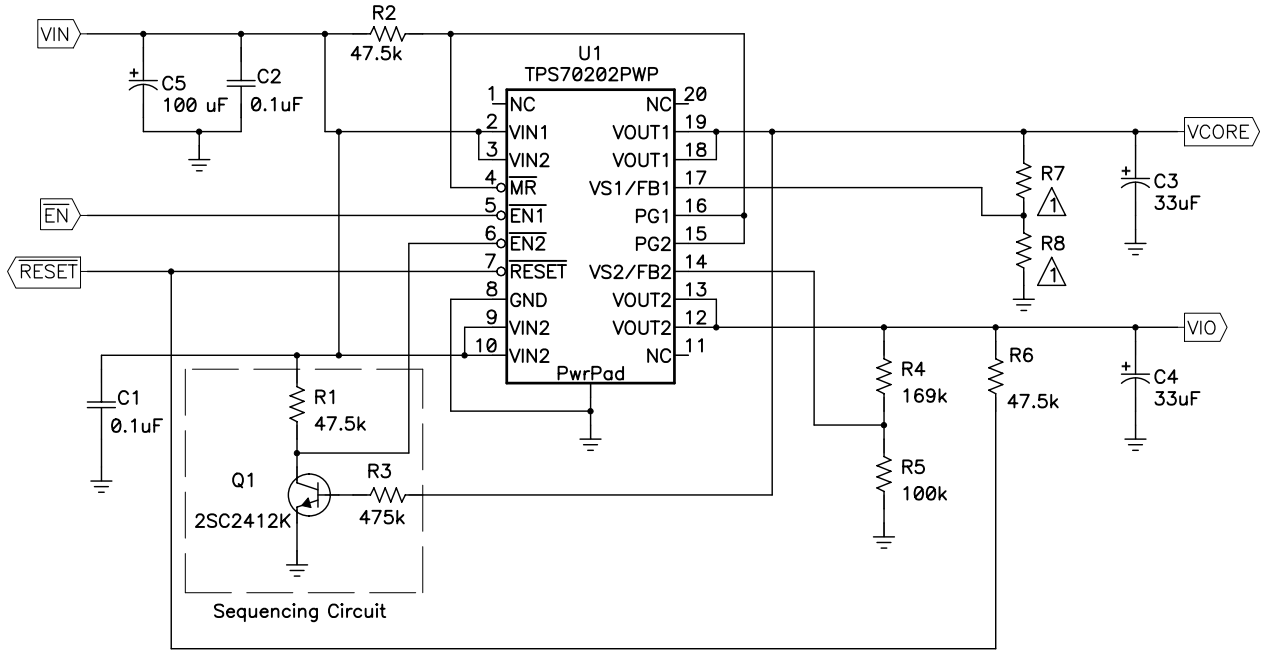
Voltage (V)	Function	Full load current (mA)
1.2	Core	110
1.6	Core	256
3.3	I/O	70

The solution was also tested in an active DSP board. The following test setup was used for this testing:


USB
Emulator
JTAG
C6550x EVM Board
(DSP, clock and glue
logic)
Input Voltage
Power Supply
1.2V or 1.6V
3.3V
Design Under
Test
Vcore
Vio
/RESET
Switched Load

QUESTIONS:

Send an email to mailto:**dsppower@list.ti.com**



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Voltage	R7	R8
1.2V	0	Open
1.6V	10.2k	33.2k

Title	C5000 DSP Attach Design 7 for 3.3 < Vin < 5.0V	
Size B	Number PR424	Rev
Date 02/14/05		Drawn by
Filename pr424.sch		Sheet of

Filename: PR424_bom.xls

Date: 02/14/2005

PR424 BOM

COUNT						
-001	-002	RefDes	Description	Size	Part Number	MFR
2	2	C1, C2	Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%	0603	GRM188R71E104KA01	muRata
2	2	C3, C4	Capacitor, POSCAP, 33-uF, 8-V, 70-milliohm, 20%	6032 (C)	8TPC33M	Sanyo
1	1	C5	Capacitor, Tantalum, 100-uF, 10-V, 100-milliohm, 20%	7343(D)	TPSD107M010R100	AVX
1	1	Q1	Transistor, NPN General Purpose, VCE 50V, VCB 60V, VEB 7V, IC 0.15A	SOT-23	2SC2412K	ROHM
3	3	R1, R2, R6	Resistor, Chip, 47.5k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R3	Resistor, Chip, 475k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R4	Resistor, Chip, 169k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	R5	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	0603	Std	Std
1	0	R7	Resistor, Chip, 0-Ohms, 1/16-W, 1%	0603	Std	Std
0	1		Resistor, Chip, 10.2k-Ohms, 1/16-W, 1%	0603	Std	Std
0	0	R8	Resistor, Chip, xx-Ohms, 1/16-W, 1%	0603		
0	1		Resistor, Chip, 33.2k-Ohms, 1/16-W, 1%	0603	Std	Std
1	1	U1	IC, Dual-output LDO Regulator w/SVS	PWP20	TPS70202PWP	TI

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