TEXAS INSTRUMENTS

APPLICATION NOTE

BUILDING DIGITAL PSK AND QAM DEMODULATORS USING THE GC2011, GC3011 AND GC3021 CHIPS

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1.0 INTRODUCTION

This report describes how one can use the GC2011 Digital Filter, the GC3011 Digital Resampler and the GC3021 Carrier Removal chips to build high performance digital demodulators for most BPSK, QPSK, and QAM radio signals. In order to simplify the RF front-end, these demodulators are fully digital, operating off of a single Analog to Digital Converter (ADC) and a single fixed frequency crystal oscillator. This digital implementation is more flexible than analog or hybrid analog-digital architectures, not only in the range of buad rates and modulation types that can be handled, but also in the types of adaption algorithms that can be used to demodulate them.

The GC2011, GC3011 and GC3021 chips are most useful in digital radios where the baud rate (the symbol rate) exceeds the capabilities of programmable DSP chips (TI's 320 series, ATT DSP series, Motorola's 56000, Analog devices' 2600 series, Intel's i860, etc.). One or more of these programmable DSP chips are powerful enough to demodulate signals with symbol rates below about 100k baud. Above 100k baud one must either use analog techniques or use function specific DSP chips such as the GC2011, GC3011 and GC3021 chips described here. These chips can be used to build demodulators with symbol rates (baud rates) up to 35 mega-buad.

The following discussions assume a working knowledge of digital radio demodulation techniques. For more information on digital radio demodulation the reader is directed to the excellent book DIGITAL COMMUNICATION, by E. A. Lee and D.G. Messerschmitt, Klumer Academic Publishers, 1988. Many of the techniques described here can be found in chapters 6, 9, 13, 14 and 15 of that book.

Section 2.0 describes the generic demodulator architecture for PSK and QAM signals. Section 3.0 describes a passband equalizer which uses the fewest number of chips and is adequate for demodulating signals with symbol rates up to 17.5 mega-baud. Section 4.0 describes a baseband equalizer which handles rates up to 35 mega-baud.

1.1 FUTURE PLANS

Most users will find these chips are adequate, if not overkill, to build most demodulators. While this chip set will serve to get a demodulator to market and will provide a vehicle for optimizing the requisite adaption algorithms, the user should contact GRAYCHIP for information on how to simplify the design for

price, size or power sensitive applications. For example, if an 8 or 10 bit data path is sufficient, then GRAYCHIP could reduce the size of each chip by 30 to 50%. A 50% size reduction could be achieved if the symbol rate is only 5 or 6 mega-baud. A 25% size reduction could be realized by using a 0.6 micron process instead of an 0.8 micron process. A 20% size reduction could be obtained by cutting the number of equalizer taps in half. A combination of these optimizations, depending upon the application, could easily result in a single, low cost chip for volume production of demodulators for microwave links, cable TV decoders (either QAM or VSB modulations), or satellite receivers.

2.0 PSK AND QAM DEMODULATORS

A generic PSK or QAM demodulator architecture using the GC2011, GC3011 and GC3021 chips is shown in Figure 1.

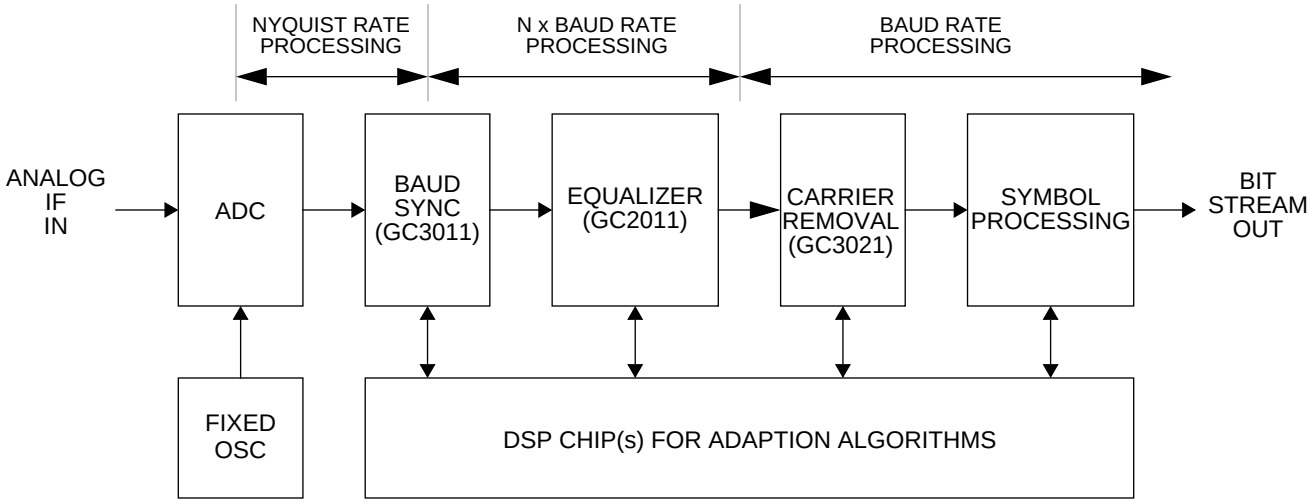


Figure 1. GENERIC DEMODULATOR

In this architecture the analog IF signal is digitized at or above the Nyquist rate for the radio signal. The Nyquist sampled signal is then resampled by a GC3011 chip to a sample rate which is a multiple of the baud rate, typically 4B for real samples and 2B for complex samples. The baud synchronous samples are then passed through a “Fractionally-spaced Forward Equalizer” (FSE) built using GC2011 filter chips. The FSE performs Nyquist (baud-shaping) filtering and removes signal distortion and intersymbol interference (ISI) from the signal. The output sample rate of the equalizer is decimated to be equal to the baud rate of the signal. The carrier removal chip mixes the signal down to baseband and removes any carrier or phase offset from the sample stream. The output bit stream is generated by the symbol processor circuit. This circuit makes symbol decisions, optionally implements decision feedback equalization, and performs any required back-end processing such as differential decoding, trellis decoding, Veterbi decoding, parallel to serial conversion, etc.

Three adaption loops are required to make the demodulator work. First, a baud timing loop adjusts the GC3011's resampling ratio to lock the resampled data rate to a multiple of the buad rate. Second, a carrier loop removes residual carrier and phase offsets from the equalized signal, and third, the FSE coefficient update loop adjusts the equalizer to remove unwanted signal distortion and ISI. The proposed architecture shown in Figure 1 assumes these adaption loops are implemented in one or more programmable DSP chips. In most cases a single DSP chip should be sufficient, but if the signal dynamics require fast tracking loops, then multiple DSP chips could be used, perhaps one for each adaption loop.

The adaption algorithms need access to signal samples at various points within the demodulator. The FSE coefficient update algorithms use the FSE input samples, the baseband samples (after carrier removal), and the carrier removal phase angles. The carrier offset adaption algorithms use either the FSE output samples or the baseband samples. The baud rate adaption algorithms use either the FSE input samples or the baseband samples. The GC2011 filter chips will capture blocks of up to 128 FSE input or output samples for use in the adaption algorithms. The other samples required for adaption are the baseband samples out of the carrier removal circuit and the carrier phase samples (or sine-cosine pairs) used to remove the carrier offset from the baseband samples. The carrier removal chip has the capability to capture blocks of up to 64 of these samples.

The adaption algorithms for the proposed architecture are block oriented in that they capture a block of samples and then use the block to perform a series of updates in the baud, carrier and equalizer loops. If a DSP chip requires 10,000 instructions to perform the series of updates and if the instruction rate is 10 million per second, then the block update rate will be around 1000 per second. If 16 updates are made per block, then the effective update rate is 16,000 updates per second, a rate which should be adequate for most environments.

2.1 BAUD RATE TIMING RECOVERY

The analog radio signal is initially sampled by an ADC operating at a fixed clock rate. The sample rate must exceed the Nyquist requirement for the signal's bandwidth, but does not have to be locked in any way to the signal's baud rate. This simplifies the analog front end by eliminating the need to synthesize an ADC clock locked to a multiple of the baud rate. Instead the proposed architecture uses the GC3011 digital resampler chip to lock the signal's sample rate to the baud rate. The resampling ratio which controls the GC3011 chip is derived either by passing the resampler output samples through a nonlinearity and detecting the baud line in the resulting sequence, or by processing the baseband samples to optimize the sampling phase. Either technique will drive the GC3011 to provide baud synchronous samples.

2.2 CARRIER OFFSET REMOVAL

Either spectral line or decision directed techniques can be used to acquire and remove carrier offset. The spectral line techniques use a power-of-N nonlinearity to create a spectral line at $N\omega_c$, where ω_c is the carrier offset frequency. The offset frequency is then detected from the spectral line and fed back into the carrier removal loop. The decision directed technique uses the phase error between the baseband samples and the symbol decisions to drive the phase offset, and therefore the carrier offset, to zero. The phase errors are used in a PLL which feeds the carrier removal VCO. The decision directed technique gives less phase jitter and is typically preferred over the spectral line technique. The spectral line technique can be useful to speed carrier acquisition by initializing the decision directed loop to the spectral line frequency.

The GC3021 Chip contains the mixer, NCO and phase error loops required to acquire and remove carrier offset. The chip also has the snapshot memories required to capture blocks of baseband output samples and phase angles required to generate the error and phase terms needed in the equalizer updates described in the next section.

2.3 EQUALIZER COEFFICIENT UPDATE

The equalizer coefficient update algorithm is:

$$c_i(k+1) = c_i(k) + \mu\varepsilon(k)x_i^*(k)e^{-j\Phi(k)}$$

Where:

$c_i(k)$ is the coefficient i at time k,

$x_i(k)$ is the data multiplied by $c_i(k)$ in the filter to generate the equalizer output at time k,

μ is the update step size,

$\varepsilon(k)$ is the error at time k, and

$\Phi(\kappa)$ is the phase angle used to remove the phase offset from time sample k.

The error $\varepsilon(k)$ is calculated from the baseband sample at time k and is typically equal to the difference between the nearest constellation point and the baseband sample. Another error formula is the constant modulus algorithm (CMA). The error for CMA is the difference between the baseband sample and the average radius of the constellation. The CMA error criterion is useful to aid initial convergence, especially when preliminary equalization is required before carrier offset can be removed.

The term $e^{-j\Phi(\kappa)}$ is used to remodulate the error back up to the carrier offset frequency of the equalizer.

3.0 THE PASSBAND EQUALIZER

This Section describes a passband demodulator architecture which uses one each of the GC2011, GC3011 and GC3021 chips. The demodulator will handle symbol rates up to 17.5 megabaud. The FSE filter in the demodulator is a 64 tap T/4 spaced equalizer. This is equivalent to a 32 tap T/2 spaced equalizer. A block diagram of the equalizer is shown in Figure 2.

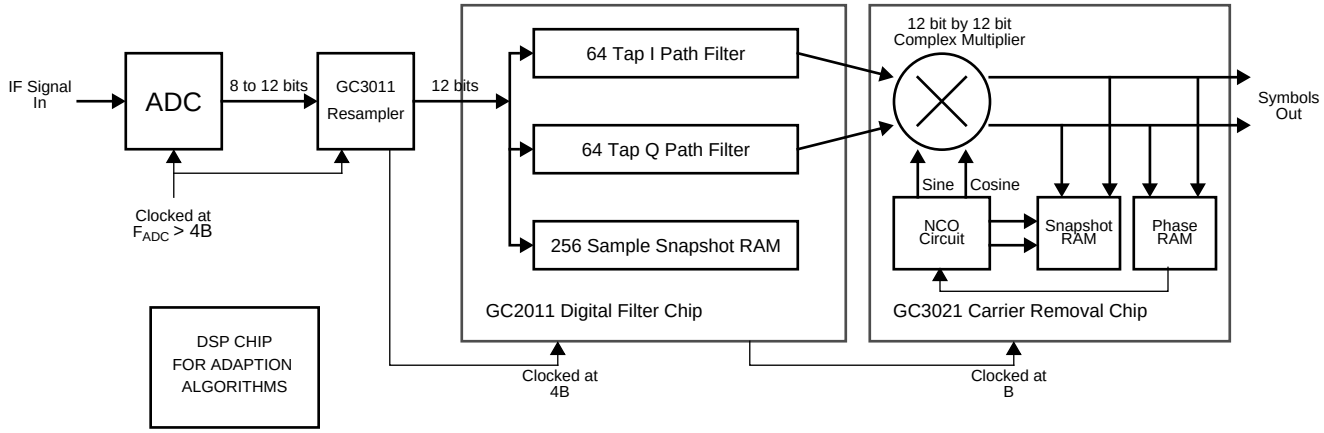


Figure 2. Passband Equalizer

The passband equalizer assumes that the input signal is not down converted to zero frequency, but is left at a center frequency equal to the buad rate, or a frequency equal to the sample rate plus or minus the baud rate. If the signal is sampled at a rate close to 5B, where B is the baud rate, then the center frequency could be at B, 4B, or 6B. This is illustrated in Figure 3(a). The baud timing recovery algorithm (see Section 2.1) sets the resampling ratio of the GC3011 chip so that the chip's output rate is exactly 4B. Note that sampling at 5B will cause signals centered at 4B or 6B to alias down to a center frequency of B.

Another example would be to sample at 4B+delta, where delta is greater than the uncertainty in the signal's baud rate. When sampling at 4B+delta, the signal must be centered at B, 3B or 5B (or any odd multiple of the baud rate).

The resampled signals are simultaneously hilbert transformed, equalized, translated to zero frequency and decimated to the baud rate in the GC2011 digital filter chip. This process is shown in Figure 3.

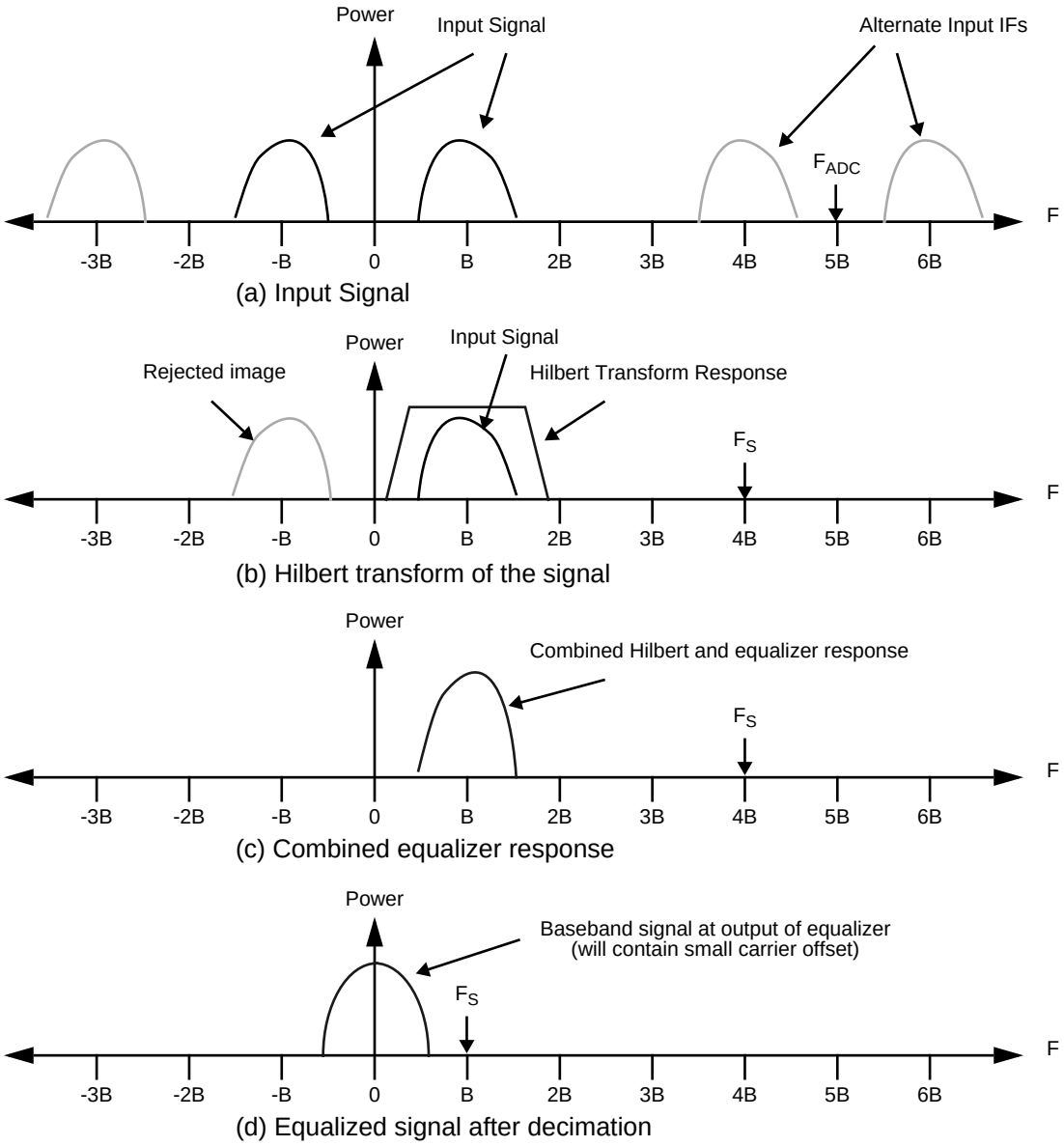


Figure 3. Passband Equalizer Spectral Response

The Hilbert transform is used to create a complex signal by rejecting the negative image of the signal. Figure 3(c) shows the bandpass nature of the equalizer spectrum when the Hilbert transform and the equalizer responses have been combined. The signal is translated to zero frequency by decimating the filter output by a factor of four. This is shown in Figure 3(d).

The input samples to the GC2011 chip are real, the coefficients are complex, and the outputs are complex. This means that the chip will be operating in the decimate by 4 and dual path modes. The filter length in these modes is 64 taps per path. This 64 tap T/4 spaced equalizer is equivalent to a 32 tap T/2 spaced equalizer, or a 16 tap T spaced equalizer. If a longer equalizer is required, then two GC2011 chips could be used to build a 128 tap T/4 spaced equalizer.

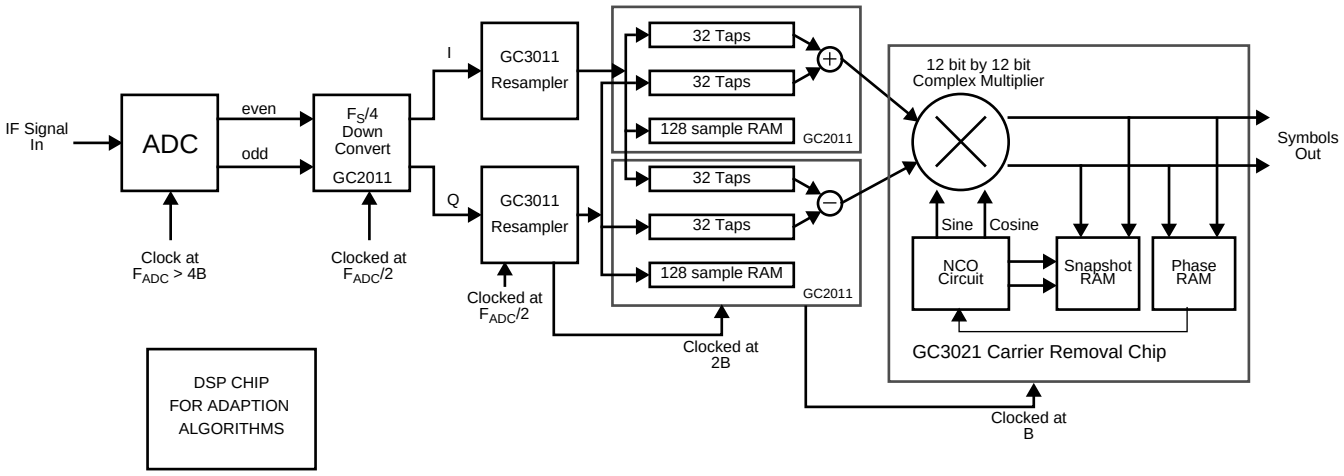
The GC3021 mixer/carrier removal chip contains the numerically controlled oscillator (NCO), the complex multiplier, the phase error lookup RAM and the snapshot RAM required for removing any carrier offset in the signal. The snapshot RAM is used for storing output samples and sine/cosine values.

The demodulator's clock rate can be up to 70 MHz which is the maximum rate of the GC3011, GC3021 and GC2011 chips. The GC3011 will synthesize the 4B clock rate from the ADC clock rate and the GC2011 chip will divide down the 4B clock to B. This will allow the demodulator to handle symbol rates approaching 17.5 megabaud, e.g., one fourth of 70 MHz.

For low power applications the chips will also function at 3.3 volts. At 3.3 volts the equalizer would be able to handle symbol rates up to 11.25 megabaud at a clock rate of 45 MHz. At 3.3 volts and 45 MHz the power consumption will be about one-fourth the power consumed at 5 volts, 75 MHz.

4.0 THE BASEBAND EQUALIZER

A baseband equalizer architecture using three GC2011 filter chips, two GC3011 resampler chips and one GC3021 Carrier Removal chips is shown in Figure 4. In this architecture the GC2011 and GC3011 chips are clocked at twice the symbol rate allowing baud rates up to 35 MHz. The GC3021 chip is clocked at the symbol rate. The filter is a 32 tap T/2 spaced FSE which will perform similar to the passband equalizer described in Section 3.



The input signal is initially centered at a frequency equal $F_{ADC}/4$, (or $F_{ADC} \pm F_{ADC}/4$) where F_{ADC} is the ADC's sample rate. The sampled signal will be centered at $F_{ADC}/4$. The signal is then translated down to zero frequency using the GC2011 chip in an $F_{ADC}/4$ quadrature down convert mode. In this mode the chip accepts pairs of input samples and outputs down converted complex samples. The complex rate out of the chip is $F_{ADC}/2$. The complex samples are then resampled to a rate equal to 2B by a pair of GC3011 chips, one for the I data and one for the Q data.

The complex samples are equalized using two GC2011 filter chips, one producing the I outputs and the other producing the Q outputs. The two chips implement a 32 tap decimate-by-2, complex data by complex coefficient filter.

Except for operating at a higher baud rate, the carrier removal circuit is identical to one in the passband equalizer.

The maximum baud rate of 35 MHz is limited by the 70 MHz maximum operating rate of the demodulator chips which must operate at twice the baud rate.

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GRAYCHIP APPLICATION NOTES:

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Revision 2

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