Texas Instruments

GC101 EVM

User's Guide

May 2005 *Wireless Infrastructure - Radio*

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GC101 EVM

1 OVERVIEW

This User's Guide document gives a general overview of the GC101 EVM, and provides a general description of the features and functions to be considered while using this module.

1.1 PURPOSE

The GC101 EVM is a motherboard style platform designed to evaluate individual Texas Instruments-Graychip devices installed on daughter boards. The platform interfaces to the daughter boards through a 168 pin Dual Inline Memory Module (DIMM) style connector. The EVM interfaces to a host computer over an ECP IEEE1284 interface.

The EVM provides internal DC power based on an external 5v input. The EVM provides digital stimulus and digital monitoring of the daughter card. Multiple devices can be evaluated using a common EVM platform with different daughter boards and PC software.

External digital input and output interfaces are provided on the GC101 EVM. External clock and synchronization signals are also provided.

The on-board memory allows the user to download test patterns and capture processed data with a PC using the provided software. The two digital input connectors allow the user to provide test patterns via an external source. A logic analyzer or digital-to-analog converter EVM can be used to monitor processed data through the output connectors.

The host computer interface controls the EVM operation from a PC. The software supplied allows the user to write or read from the control and page registers of the daughter card under test. Figure 1-1 shows an interface diagram of the components that make up a typical GC evaluation system.

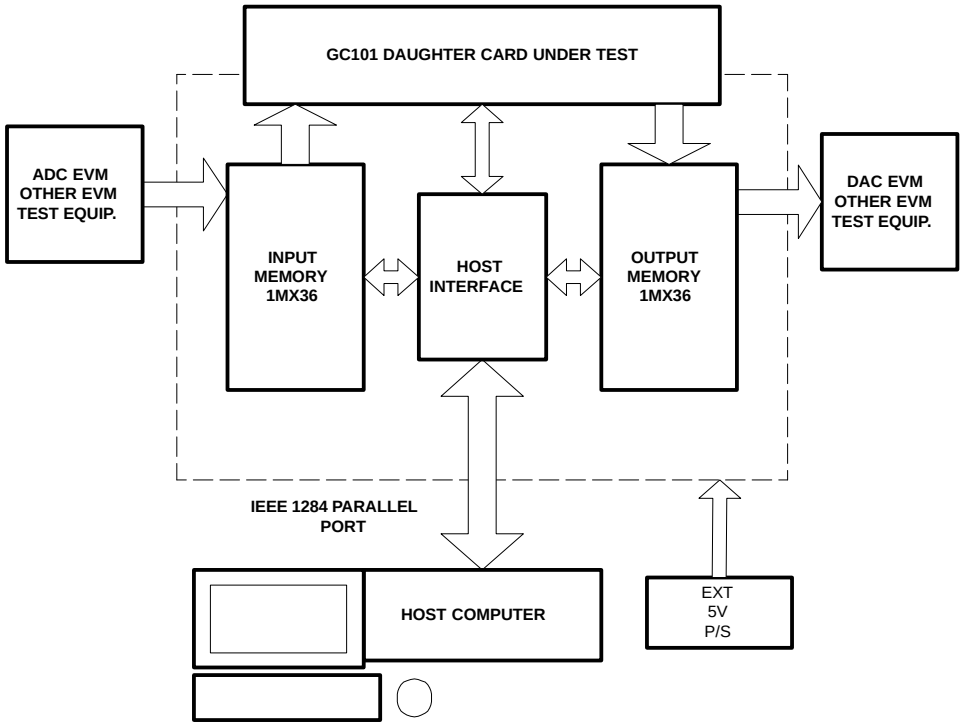


Figure 1. GC Evaluation System

1.2 GC101 EVM BASIC FUNCTIONS

The EVM provides the DC power, local bus programming, clock, data path, digital stimulus, digital monitoring, and local PC host control interface to test a GC101 daughter card.

The DC power is provided from a set of regulators that convert the 5v external power to local EVM power of 1.8vdc and 3.3vdc. Additional power supplies are provided for daughter card 2.5v and 3.3vdc. Additional external power supplies are provided for additional (2) dedicated power supplies on the daughter card.

The Local Bus programming is provided through the local PC host control interface. The clock and data path control provide for internal clock generation, internal sync generation, internal data stimulus, or external signals. The digital monitoring can be provided in all modes, and can be stored in memory and/or output to the digital interface.

The EVM provides a 36 bit stimulus and monitoring path for the daughter card . The 36bit path consists of a memory or external input data, input sync, and input clock.

The EVM has an internal 10Mhz oscillator to develop a 40, 60, 80, 100, or 120 Mhz internal clock. The EVM has an internal PLL that provides for clock multiplication of 1,2,4,6,8,10, and 12. The digital clock can select the Analog PLL or reference clock signal. The clock oscillator is in a socket, and can be changed to a different clock rate. A clock can be provided internally from the digital input connector, or from an SMA external input.

There are two 40pin digital input and output headers for the external input and output data. The sync signal can also be supplied internally, through the external data input, or through an SMA connector.

PC software is supplied to control the EVM. The PC software uses a custom script language to program the EVM. The PC software is available in either a batch processing (Text User Interface) or with a Graphic Control interface (Graphic User Interface). The PC software is installed with the Graphics User software for each daughter card.

The block diagram of the GC101 EVM is shown in Figure 2.

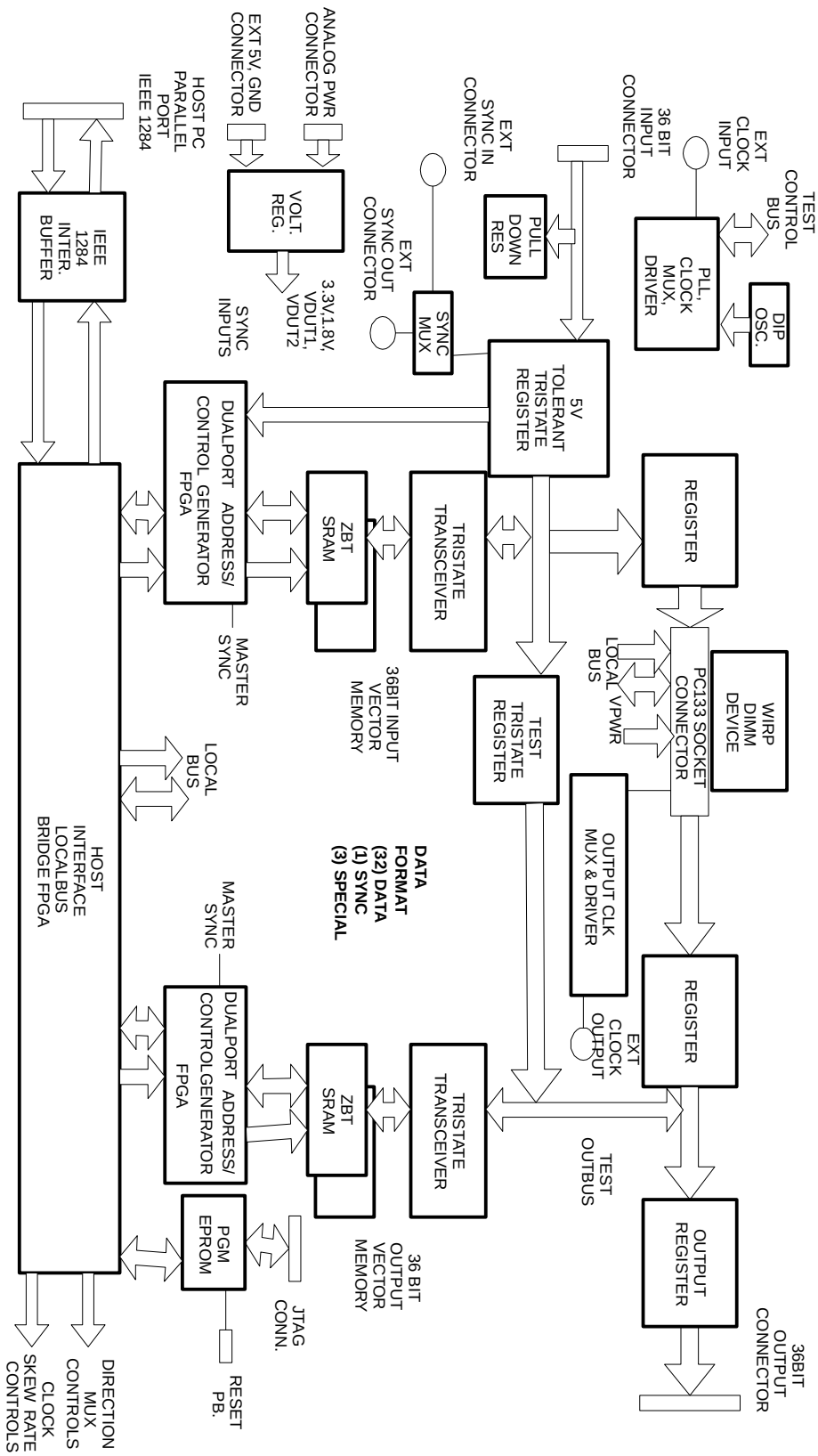


Figure 1–2. GC101 EVM Block Diagram

Figure 2. GC101 EVM Block Diagram

1.3 POWER REQUIREMENTS

1.3.1 SINGLE SUPPLY

The GC101 EVM has on-board regulators that generate all required voltages for both the motherboard and daughter cards. All regulators require an input voltage between 3.0 and 6.0VDC. This input voltage can be provided through mini power jack J9 when using the provided 5 VDC power supply. Another option is to provide 5 VDC to the 10 pin Molex connector P1. Connect 5 VDC to pin 5 and the return to any one of pins 2,4,6,8, or 10.

1.3.2 MULTIPLE SUPPLIES

GC101 EVM individual voltages can be provided through connector P1 as follows:

+1.8VDC	pin 1
+3.3VDC	pin 3
+5VDC	pin 5
VDUT1 (3.3VDC)	pin7
VDUT2 (2.5VDC)	pin 9
GND	pins 2, 4, 6, 8, 10

WARNING
WHEN USING P1 TO PROVIDE +1.8, +3.3V, VDUT1, or VDUT2, THE FOLLOWING INDUCTORS MUST BE REMOVED TO PREVENT DAMAGING THE EVM REGULATORS:

L3 FOR +3.3 VDC,
L4 FOR +1.8 VDC,
L5 FOR VDUT1,
L6 FOR VDUT2

1.3.3 SPARE POWER INPUTS

Connectors J16, J17, and J18 allow additional voltages to be provided to the daughter card connector for use with future daughter boards. These are provided as VDUT3, VDUT4, and a separate GND to the daughter card connector.

1.4 SOFTWARE INSTALLATION

The GC101 EVM operates from the system software that comes with the System Evaluation Kit. See the daughter board (GC5016, GC5316, ect…) User's Guide for software installation and operation. This CD contains software to allow the user to test a TI Wireless Infrastucture Digital Radio Product using the GC101 EVM. The software also allows the user to test the GC101 EVM in a stand alone operation. Details on this software can be found in section 2.4 and Appendix A of this document.

1.5 HARDWARE CONFIGURATION

By using the provided software and on-board jumpers, the GC101 EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration, make the appropriate connections, and load the appropriate software modules. Details of the software operation can be found in the GC5016 Daughter card EVM and GUI Software Guide and Appendix A of this document. Before starting, verify all GC101 EVM jumper settings per the following tables:

Table 1. Two Pin Jumper List Table

JUMPER	FUNCTION	INSTALLED	REMOVED	DEFAULT
W4	Not Used			Removed
W5	Indicates PC parallel port mode for U45 firmware ECP mode	ECP mode	Not ECP mode	Installed
W7	Sets Parallel port interface device drive mode	Open drain	Totem pole	Removed

Table 2. Three Pin Jumper List Table

JUMPER	FUNCTION	LOCATION: PINS 1- 2	LOCATION: PINS 2-3	DEFAULT
W1	Provide 3.3V or 5V to oscillator U41	Provides 3.3V to U41	Provides 5V to U41	1-2
W2	Sets JTAG connector TDI direction	To prom and FPGA's	TO DIMM connector J7	2-3
W3	Sets JTAG connector TDO direction	To prom and FPGA's	TO DIMM connector J7	2-3
W6	Set parallel port bus interface voltage level	5V operation	3.3V operation	2-3
W8	Power select for 8 pin and 14 pin oscillators	Provides +3.3V to pin 14 of U41	Provides +3.3V to pin 8 of U41	2-3

1.6 FIRMWARE DOWNLOADING

The GC101 EVM contains three Altera FPGA 20K Apex devices and two reprogrammable Flash configuration devices, U42 and U59 (EPC2). Upon power-up or system reset (S2), the EPC2s will program the following FPGs in this order:

U12 (Memory In Controller)
U45 (Parallel Port Controller)
U33 (Memory Out Controller).

If firmware other than that delivered with the EVM is to be used, two methods are available for setting up the EVM.

The first is to remove U42 and U59 from the sockets and replace them with two other programmed parts.

The second is to reprogram the Flash devices using the following steps:

1. Connect an Altera ByteBlasterMV parallel port download cable to J13. Make sure pin 1 of cable lines up with pin 1 of J13.
2. With Altera Quartus software up and running, go to the compile mode screen.
3. Set the mode to "JTAG".
4. Click on "Add File". Select desired .pof files and click on "OPEN".
5. Select Program/configure box for the files. Click on "START".
6. The progress indicator will now go from 0% to 100%. Configuration is now complete.
7. Remove the ByteBlaster cable and depress reset button S2.
8. The FPGA status LEDs (D6, D7, and D10) will all be lit when the devices have been configured properly.

2 GC101 EVM OPERATIONAL PROCEDURE

The GC101 EVM can be used to evaluate several available Wireless Infrastucture Digital Radio Products. These products are available on daughter cards which interface directly to the GC101 EVM.

2.1 DAUGHTER BOARD INTERFACE

After loading the proper software that comes with this evaluation kit, insert the daughter card into DIMM connector J7. To ensure the board is seated properly, check to make sure the connector locking tabs are in place on the Daughter Board. The boards are keyed so that they can only be inserted one way. Check Daughter card dipswitch settings (if applicable) per test requirements.

2.2 PARALLEL PORT INTERFACE

Connector J14 on the GC101 EVM provides the parallel port interface to a Laptop/PC. This is a standard 25 pin DB25F connector which supports a IEEE-1284A Type A to Type A parallel port cable. Install a parallel port cable between J14 of the EVM and a parallel port on a PC/Laptop.

2.3 INPUT POWER INTERFACE

Connector J9 provides a method to input +5VDC to the GC101 EVM with the provided AC-to-DC power supply. This provides the only input supply (+5VDC) required by the EVM. The power supply requires 110-120 VAC as in input source. Connect the power supply plug into an AC source and the output connector into J9 of the evm. After applying power, LED's D6, D7, and D10 should be illuminated. These diodes are located in the lower left area of the evm, just above J10. If they do not illuminate after power is applied, make sure the power supply connectors are installed properly and that there is +5VDC present at test point 1 (located just to the right of J9) of the evm. The board will not operate if the LED's are not illumunated.

2.4 GC101 EVM SELFTEST

If the GC101 EVM does not appear to be operating properly, the user can run several board level tests with the provided software. To test the PC interface with the GC101 EVM, run the program called gc101tui.exe, located under the directory C:\GC101_5016\. This will start the GC Text Users Interface Software.

After executing this program, the text user interface main menu shall appear as shown in Figure 3.

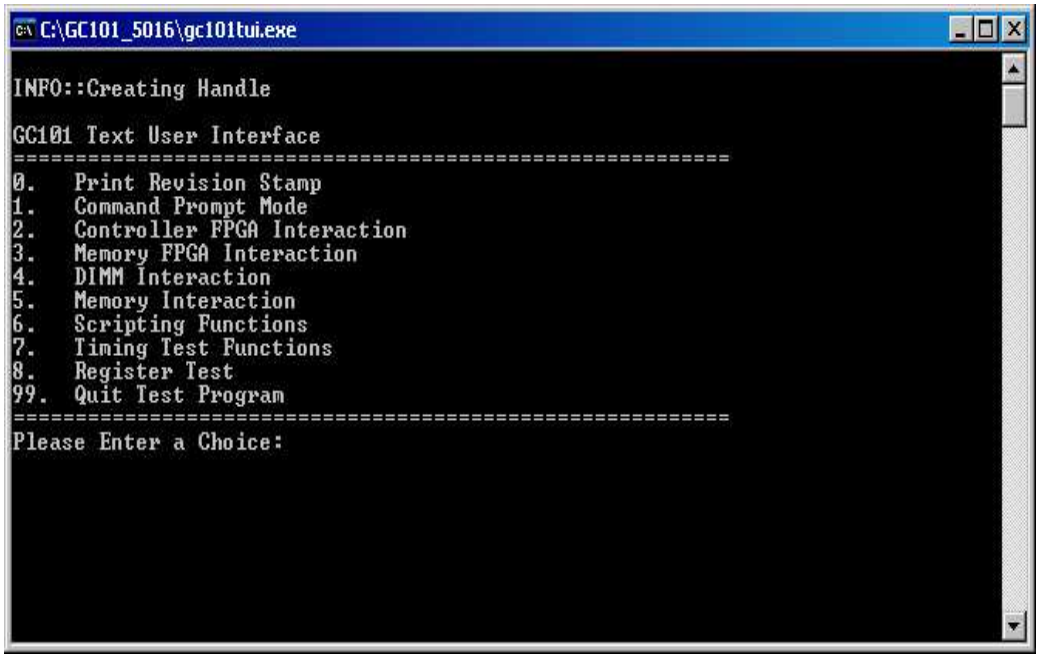


Figure 3. Text User Interface Main Menu

To start the interface test, enter an "8" to select the Register test. This will bring up the register test menu as shown in Figure 2-1.

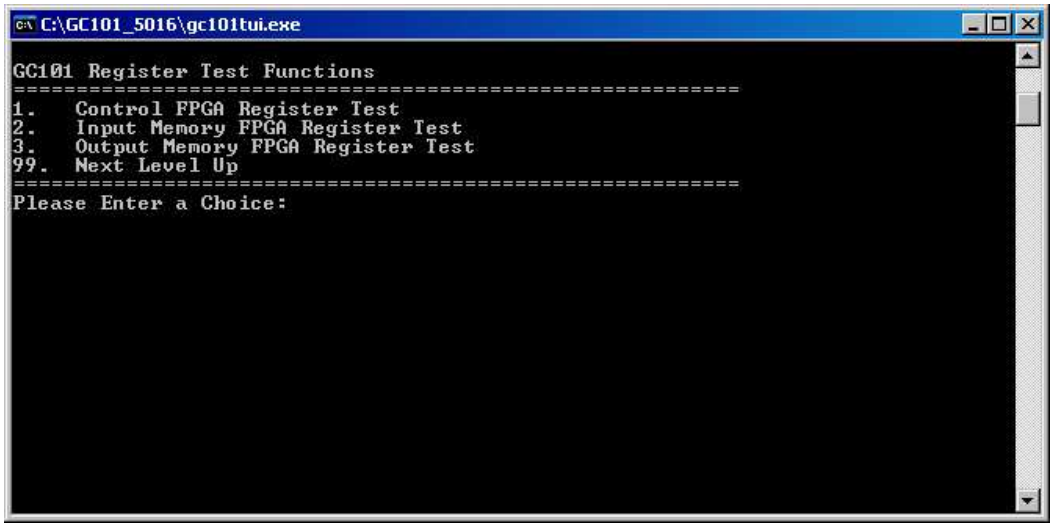


Figure 4. Text User Interface Register Test Menu

To test the parallel port interface, enter an “1” to start the Control FPGA Register test. The software will write to and read from every register stored inside the Control FPGA. Upon completion, the program will report back the total number of test errors that were found. If the number of test errors is 0, the parallel port interface is working properly.

This test can be repeated for both the Input and Output Memory FPGA’s by selecting the appropriate function shown in the menu. A detailed description of the GC Text User Interface software can be found in Appendix A of this document.

3 PHYSICAL DESCRIPTION

3.1 PCB LAYOUT

The GC101 EVM is constructed on a 14-layer, 10.0-inch x 6.5-inch, .125-inch thick PCB using FR-4 material. Figure 5 shows the top layer and Figure 6 shows the bottom layer. The remaining layer information can be provided on request.

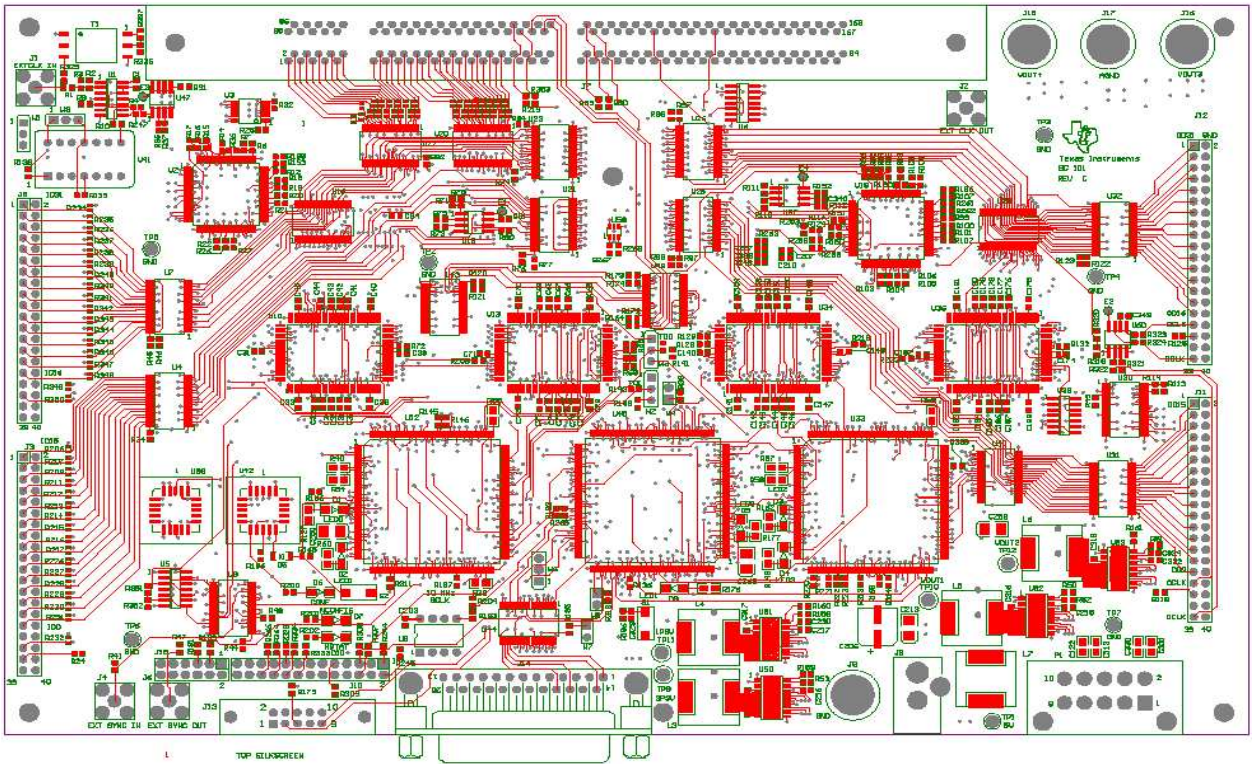


Figure 5. Top Layer

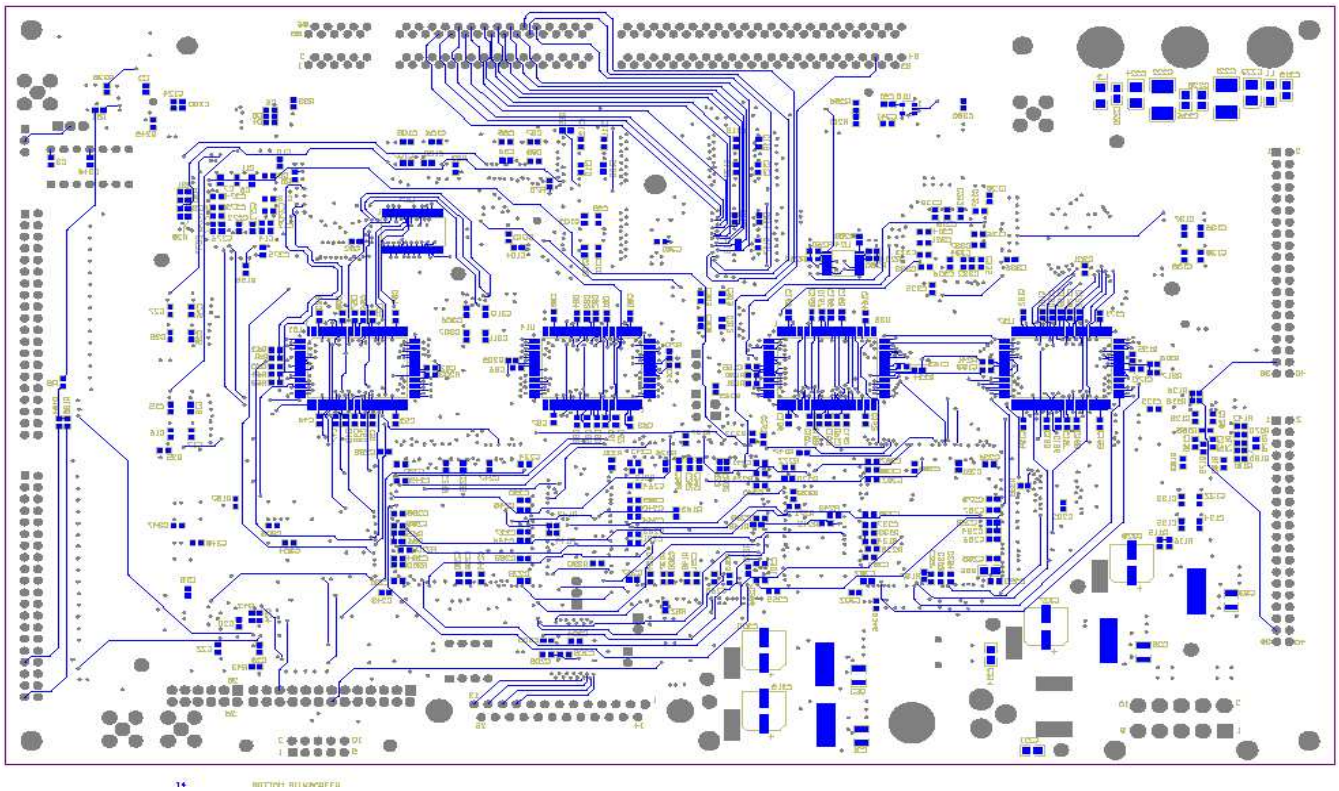


Figure 6. Bottom Layer

3.2 PARTS LIST

Table 3 lists the parts used in constructing the EVM.

Table 3. GC101 EVM PARTS LIST

BILL OF MATERIAL FOR GC101 EVM					
VALUE	**QTY**	**PART NUMBER**	**VENDOR**	**REF DES**	**NOT INSTALLED**
CAPACITORS					
470 Uf, 10V, 10% Capacitor	5	TPSE477M010R0100	AVX	C206 C319 C320 C327 C328	
47uF, Tantalum, 10V, 20%	2	ECS-T1AD476R	Panasonic	C221 C222	
2.2uF, 20V, 20% Capacitor	3	ECS-T1DX225R	Panasonic	C250 C258 C269	
10uF,20V, 20% Capacitor	3	ECS-T1DC106R	Panasonic	C213 C223 C224	
10uF, 10V, 10% Capacitor	4	C1210C106K8PACTU	KEMET	C21 C29 C30 C93	
0.1uF,16V, 10% Capacitor	7	ECJ-2VB1C104K	Panasonic	C113 C122 C211 C219 C220 C330 C331	
1 uF, 10V, 10% Capacitor	3	ECJ-2YB1A105K	Panasonic	C214 C225 C226	

Table 3. GC101 EVM PARTS LIST (continued)

BILL OF MATERIAL FOR GC101 EVM					
VALUE	**QTY**	**PART NUMBER**	**VENDOR**	**REF DES**	**NOT INSTALLED**
0.1uF,16V, 10% Capacitor	280	ECJ-1VB1C104K	Panasonic	C1-C6 C15-C20 C22-C28 C31-C92 C94-C112 C114-C121 C123 C124 C128-C205 C207-C210 C215-C217 C227 C228 C231-C249 C251-C257 C259-C268 C279-C313 C322 C329 C338-C341 C346-C350 R1	C351
0.01uF,16V, 10% Capacitor	34	ECJ-1VB1C103K	Panasonic	C7-C14 C125-C127 C212 C218 C229 C270-C278 C314 C321 C323 C325 C326 C332-C337	
0.047uF,16V, 10% Capacitor	4	ECJ-1VB1C473K	Panasonic	C315 C316 C317 C318	
0.027uF,16V, 10% Capacitor	1	ECJ-1VB1C273K	Panasonic	C324	
0.039uF,16V, 10% Capacitor	1	ECJ-1VB1C393K	Panasonic	C230	
RESISTORS					
0 ohm resistor, 1/8 W, 5%	8	ERJ-6GEY0R00V	Panasonic	R39 R40 R54-R59	
475 ohm resistor, 1/10 W, 1%	2	ERJ-6ENF4750V	Panasonic	R176 R177	
511 ohm resistor, 1/10 W, 1%	4	ERJ-6ENF5110V	Panasonic	R60 R127 R149 R162	
0 ohm resistor, 1/10 W, 5%	65	ERJ-3GEY0R00V	Panasonic	R4 R23 R36 R48 R49 R51 R52 R53 R92 R136 R137 R139 R142 R144 R146 R154-R158 R163 R170 R171 R178 -R183 R185 R187 R189 R190 R191 R198 R219-R223 R242-R245 R264 R266 R307-R315 R326-R334 R338	R72 R138 R143 R145 R147 R148 R184 R203 R204 R205 R209 R210 R218 R224 R225 R233 R241 R325
10 Ohm resistor, 1/16 W, 1%	55	ERJ-3EKF10R0V	Panasonic	R8 R10 R13-R22 R25-R31 R37 R47 R73 R79 R80 R81 R86 R89 R90 R91 R93-R96 R99-R106 R110 R111 R112 R117 R118 R119 R124 R125 R150 R151 R152 R248 R322 R353	R126 R321 R323 R324
130 ohm resistor, 1/16 W, 1%	76	ERJ-3EKF1300V	Panasonic	R5 R6 R7 R12 R32-R35 R43 -R46 R61-R71 R74-R78 R82-R85 R87 R88 R97 R98 R107 R108 R109 R113-R116 R120-R123 R128-R135 R153 R164 R172 R173 R174 R186 R188 R192 R247 R249 R251 R256 R260 R261 R262 R263 R265 R316 R317 R319 R320	

Table 3. GC101 EVM PARTS LIST (continued)

BILL OF MATERIAL FOR GC101 EVM					
VALUE	**QTY**	**PART NUMBER**	**VENDOR**	**REF DES**	**NOT INSTALLED**
1K ohm resistor, 1/16 W, 1%	11	ERJ-3EKF1001V	Panasonic	R140 R165 R167 R168 R175 R194 R253 R255 R257 R259 R269	R141 R250 R252 R254 R258 R336 R337
10K Ohm Resisror, 1/16 W, 1%	14	ERJ-3EKF1002V	Panasonic	R2 R3 R38 R195 R197 R199 R246 R270-R274 R318 R339	R166 R169
4.75K ohm resistor, 1/16 w, 1%	2	ERJ-3EKF4751KV	Panasonic	R196 R351	R267 R268 R352
47.5K ohm resistor, 1/16 W, 1%	0	ERJ-3EKF4752V	Panasonic		R24
49.9 ohm resistor, 1/16 W, 1%	2	ERJ-3EKF49R9V	Panasonic	R42 R193	R9 R11 R41
82.5 ohm resistor, 1/16 W, 1%	3	ERJ-3EKF82R5V	Panasonic	R200 R201 R202	
100 Ohm resistor, 1/16 W, 1%	0	ERJ-3EKF1000V	Panasonic		R50 R159 R160 R161
47.5K ohm resistor, 1/16 W, 1%	35	ERJ-2RKF4752X	Panasonic	R206 R207 R208 R211-R217 R226-R232 R234-R240 R340-R350	
22.1 ohm resistor, 1/16 W, 1%	32	ERJ-2RKF22R1X	Panasonic	R275-R306	
INDUCTORS					
INDUCTOR	2	EXC-ML32A680U		L1 L2	
4.6uF COIL	5	ETQ-P6F4R6HFA	Panasonic	L3-L7	
CONNECTORS, HEADERS, SWITCHES, LED'S & TEST POINTS, JACKS					
SMA connectors	4	901-144-8RFX	AMP	J1 J2 J4 J6	
DIODE, 75V, 500 mW	1	LL4148-13		D5	
Black test point	6	5011K	Keystone	TP2-TP7	
Red test point	5	5010K	Keystone	TP1 TP9-TP12	
2POS_header	3	HTSW-150-07-L-S	Samtec	W4 W5 W7	
3POS_header	5	HTSW-150-07-L-S	Samtec	W1 W2 W3 W6 W8	
3POS-POWER_JACK R/A	1	RAPC722	Switchcraft	J9	
CONNECTOR 10 POS.	1	102153-1	AMP	J13	
Mounting Screws	2			J13	
NUTS	2			J13	
168 Pin Amp Connec-tor RA TH	1	168_IC438_DIMM	AMP	J7	
40 pin header	4	HTSW-120-07-L-D	Samtec	J3 J5 J11 J12	
Connector D-SUB, RCPT R/A 25 POS.	1	745536-2	AMP	J14	
Red Banana Jacks	2	ST-351A	ALLIED	J16 J18	
Black Banana Jacks	2	ST351B	ALLIED	J8 J17	
10 pin Header	1	39-29-1108	MOLEX	P1	
12PIN_IDC	1	HTSW-106-07-L-D	Samtec	J15	
26PIN_IDC	1	HTSW-113-07-L-D	Samtec	J10	
T1-IT-KK81_XFMR	0	MC_KK81	Mini-Circuits		T1
SWITCH	2	EVQ-PJX04M	Panasonic	S1 S2	

Table 3. GC101 EVM PARTS LIST (continued)

BILL OF MATERIAL FOR GC101 EVM					
VALUE	**QTY**	**PART NUMBER**	**VENDOR**	**REF DES**	**NOT INSTALLED**
RED LED	1	CMD15-21SRC/TR8	Panasonic	D7	
GREEN LED	8	CMD15-21VGC/TR8	Panasonic	D1-D4 D6 D8 D9 D10	
Stand Off Hex (1/4 x .5")	6	1902CK-ND	Allied		
IC'S					
CY7B994V	2	CY7B994V-2AC	CYPRESS	U2 U18	
CY7C1372	4	CY7C1372C-167AI or CY7C1372D-167AXI	CYPRESS	U10 U13 U34 U36	U11 U14 U35 U37
EP20K60E-208	2	EP20K60EQC208-1	ALTERA	U12 U33	
EP20K60E-208	1	EP20K60EQC208-3	ALTERA	U45	
EPC2LC20	2	EPC2LC20 PLCC	ALTERA	Insert in U42 U59 socket	
SOCKET	2	PLCC-20-T-A	SAMTEC	U42 U59	
40 megahertz oscilator	1	SG-8002DC-PWT	Epson	Insert in U9 socket	
SOCKET	1	ICA-308-ZS-GG	SAMTEC	U9	
10 megahertz oscillator	1	SG-8002DC-PWT	Epson	Insert in U41 socket	
SOCKET	1	ICA-314-ZS-GG	SAMTEC	U41	
CY2305SI-1H	4	CY2305SI-1H	CYPRESS	U19 U47 U57 U60	
ICS601-01	2	ICS601G-01	ICS	U3 U24	
IDTQS3VH125	4	IDTQS3VH125S1	IDT	U1 U5 U6 U38	
SN74ALVTH16374	10	SN74ALVTH16374GR	TI	U4 U7 U8 U20-U23 U25 U26 U43	
SN74LVC16374A	4	SN74LVC16374ADGGR	TI	U30 U31 U32 U49	
SN74CBTLV16210	4	SN74CBTLV16210GR	TI	U16 U17 U39 U40	
SN74LVC1G04	1	SN74LVC1G04	TI	U15	
SN74LVC161284	1	SN74LVC161284DGGR	TI	U44	
SN74LVC2G14	0	SN74LVC2G14	TI		U58
TPS54614	1	TPS54614PWP	TI	U51	
TPS54615	1	TPS54615PWP	TI	U53	
TPS54616	2	TPS54616PWPR	TI	U50 U52	
JUMPER SHUNT LOCATION: W1 PIN 1-2, W2 PIN 2-3, W3 PIN 2-3, W6 PIN 2-3, W8 PIN 2-3					
JUMPER SHUNT LOCATION: W4 OUT, W5 IN, W7 OUT					

4 CIRCUIT DESCRIPTION

4.1 INPUT CLOCK

The GC101 EVM has three methods for providing an input data clock: using an on-board oscillator, through SMA connector J1, or through input data header J3. The default operation setting is for using the on-board oscillator. SMA connector J1 has provisions for serial and/or parallel termination. The clock input should be a 50 Ohm source, square wave signals, +3.3V referenced to ground, with a duty cycle of 50 +/- 5%. The clock input high voltage must exceed 1.7 V and the input low votlage must be 0.7 V or lower to meet the requirements of the clock MUX input. The GC101 has provisions to allow the user to route the external clock through a transformer to assist with meeting the clock MUX input requirements.

Input Data header J3 has provisions for providing an input clock on pin 33 or pin 39, depending on which resistor (R184 or R185) is installed. This input also has provisions for serial and/or parallel termination.

The on-board 10MHz oscillator provides another option for an input clock source. This device is mounted on a socket to allow it to be easily replaced with a different frequency oscillator if desired. Jumpers W1 and W8 can be used to change the oscillator voltage and which pin receives it. Installing a jumper on pins 1-2 of W1 provides +3.3V to the oscillator while a jumper on pins 2-3 will provide +5V. Installing a jumper on pins 1-2 of W8 provides the power to pin 14 of the oscillator while a jumper on pins 2-3 will provide power to pin 8. This allows both 8 and 14 pin package oscillators to be used with the socket.

The input clock multiplexer U1 is software controlled. The CLKMUXS, CLKMUXSWOSKEW, INCLKSEL script commands in Appendix A are used to control the Clock source selection.

The selected clock is routed to both the Analog PLL and to the Digital PLL. The analog PLL allows for clock multiplication if the Input clock is between 10 and 27Mhz. U3 is the analog PLL. The software controls a x1,x2,x4,x6,x8,x10, or x16 multiplier for the clock input. The CLKMUXS, CLKMUXSWOSKEW, and INANGPLL script commands in Appendix A are to control the Analog PLL multiplication.

U2 is the Input Clock PLL. U2 provides the distributed clock. The minimum clock rate is 25Mhz. Each of the 4 clock banks has software controlled skew and clock division. Bank3 has inversion. U2 has software controls to select the Analog PLL or Selected digital clock, and the operating range of the Digital PLL. The Digital PLL has several controls:

PLL Clock Input Selection
PLL Range
PLL Reference Divide (used for Digital PLL Clock Rate multiplication)
PLL Bank (1-4) Divide and Skew settings

The CLKMUXS, CLKMUXSWOSKEW, and INPLLCLKSEL script software commands are used to control the PLL Clock Input Selection.

The CLKMUXS, CLKMUXSWOSKEW, and INCLKRATE script software commands are used to control the PLL Range.

The PLL Reference Divide is controlled through the software script command INPLLDIV. It is not normally used.

The PLL Bank Divide is controlled through the software script command INPLLDIV. It is not normally used.

The PLL Skew is controlled through the software script command PLLSKEW. Skew control is utilized when the clock rate is >= 80Mhz, and if external clock or external data is selected.

Input Digital PLL Bank#	Provides clock for:
1	External Data input registers, Input MemoryFPGA
2	Input SRAM
3	Test In->Out registers, Daughter card (DIMM) Clock
4	InputBus to DIMM Input registers, Output Digital PLL Input Clock

4.2 INPUT SYNC

The input sync signal is used to develop a reference time for the daughter card circuits. The GC101 EVM has three methods for providing an input sync signal: input SRAM data, through SMA connector J4, or through input data header J3. The default operation setting is for an input sync to be provided by the input SRAM data. The SMA input represents a 50 Ohm load to the source and has provisions for serial and/or parallel termination. The sync input should be a CMOS level signal, logic-low pulse, where the 0-1 transition is time 0. The input sync multiplexer U5 is software controlled.

The Input Sync Selection is controlled through software script commands. The CLKMUXS, CLKMUXSWOSKEW, SYNCINRESET, and SYNCSEL commands can be used to control the selection.

4.3 INPUT DATA

The GC101 EVM has two methods for providing up to 36 bit input data: through input data header J3 and J5, or on-board memory that is loaded from an external PC. The Input data is registered on the GC101 before being transmitted to the DIMM connector for the daughter card.

The default selection of data is the internal Input SRAM data. The SRAM data is loaded into the input SRAM from the host PC. The Input SRAM is controled by the Input Memory FPGA. The Input SRAM can be recorded, written, or read for other uses.

The LSRAM2 software script command is used to load a text-readable hex format into the Input SRAM. The data is organized as two columns, 32bits of data for memory, and 4 bits of special and synchronization data.

The configuration of the Input Memory FPGA to cause the SRAM to be written or read is performed in script files. Typically the setup script file loads the input data. The address generator script file, start script file, and restart script files for each experiment control the In Memory and Out Memory FPGA functions.

The other option for input data is through data header J3. Each input has a 47.5k pulldown resistor. The data input can be either +3.3V or +5V referenced to ground with a maximum data rate of 130 MHz.

The input data is registered, and the software selects whether the input data to be used is from the input connectors or the input memory system.

The Input Bus data is selected based on the tristate enable of the Input registers, or the Bus Transceiver for the InMemory SRAMs.

The software script commands CLKMUXS, CLKMUXSWOSKEW, and InMEMSEL are used to select the data source for the daughter card.

The pinout description for J3 and J5 are shown in Table 4 and Table 5.

Table 4. Input Connector J3 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	ID15	I	Input Data Bit 15	2	GND	-	System Ground
3	ID14		Input Data Bit 14	4			
5	ID13		Input Data Bit 13	6			
7	ID12		Input Data Bit 12	8			
9	ID11		Input Data Bit 11	10			
11	ID10		Input Data Bit 10	12			
13	ID9		Input Data Bit 9	14			
15	ID8		Input Data Bit 8	16			
17	ID7		Input Data Bit 7	18			
19	ID6		Input Data Bit 6	20			
21	ID5		Input Data Bit 5	22			
23	ID4		Input Data Bit 4	24			
25	ID3		Input Data Bit 3	26			
27	ID2		Input Data Bit 2	28			
29	ID1		Input Data Bit 1	30			
31	ID0		Input Data Bit 0 (LSB)	32			
33	ECLK1		External Input Clock 1	34			
35	SP1		Square Input	36			
37	ISYNC		Input Sync	38			
39	ECLK2		External Input Clock 2	40			

Table 5. Input Connector J5 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	ID31	I	Input data bit 31 (MSB)	2	GND	-	System Ground
3	ID30		Input data bit 30	4			
5	ID29		Input data bit 29	6			
7	ID28		Input data bit 28	8			
9	ID27		Input data bit 27	10			
11	ID26		Input data bit 26	12			
13	ID25		Input data bit 25	14			
15	ID24		Input data bit 24	16			
17	ID23		Input data bit 23	18			
19	ID22		Input data bit 22	20			
21	ID21		Input data bit 21	22			
23	ID20		Input data bit 20	24			
25	ID19		Input data bit 19	26			
27	ID18		Input data bit 18	28			
29	ID17		Input data bit 17	30			
31	ID16		Input data bit 16	32			
33			Not Used	34			
35	SP2	I	Spare Input	36			
37			Not Used	38			
39			Not Used	40			

4.4 OUTPUT CLOCK

The output clock is selected as the input clock or the daughter board output clock. The selected clock is input to a 4x analog PLL (U24) and to the Output Digital PLL.

The Output Digital PLL normally selects the Input Clock. The other selection is the DIMM Output Clock. The clock selection is controlled through software script commands; CLKMUXS, CLKMUXSWOSKEW, and OUTCLKSEL.

The selected clock or the 4x analog multiplied clock is selected in the Digital Output PLL. The selected clock is conditioned with a PLL, and buffered to the output memory, Out Memory FPGA, DIMM output registers, and digital output registers. The Digital Output PLL receives the Input clock, and the DIMM output clock. The PLL provides for frequency multiplication, skew adjustment and buffering.

There are 5 sets of Output Clocks:

Ext Clock Output — SMA connector to connect a reference output clock

Bank 1 — DIMM Output registers, and OutMemory FPGA

Bank 2 — OutData bus to Output connector registers

Bank 3 — Output Connector Clock output (through buffer)

Bank 4 — Output SRAMs

The Output Digital PLL clock selection is controlled through a software script command, OUTPLLCLKSEL. Normally this control is set to the selected 1x clock.

The Output Digital PLL range is normally controlled through the Input Clock controls. The PLL range selection is controlled through software script commands; CLKMUXS, CLKMUXSWOSKEW, and OUTCLKRATE.

The Output Digital PLL has 4 banks of outputs that have separate divider and skew controls. The Output Divider functions are not typically used. If used they are controlled through the software script commands: Bank Division – OUTPLLDIV divides all of the clock outputs by 1, 4, or 8. The CLKMUXS and PLLSKEW script commands control the Output PLL Skew values.

The data output connector has an output clock available on either output data header J11 pin 33 or 39, or header J12 pin 33 or 39, depending on resistor installation. See schematic sheet 7 for more details.

4.5 OUTPUT SYNC

There are two different synchronization outputs available. The DIMM Sync Output is data bit D32 on the DIMM Output bus. This can be output on the digital output data, and is also recorded in the Out SRAM.

Another output synchronization provides synchronization timing to the In Memory FPGA Playback counter. The EXT SYNC OUT occurs 2 clock cycles later than the internal start Index.

The DIMM output syncs are available on either output data header J11 pin 37 or J12 pin 37, depending on resistor installation. See schematic sheet 7 for more details.

4.6 OUTPUT DATA

The GC101 EVM has two methods for providing up to 32 bits of output data: through output data header J11 and J12, or recorded in the onboard memory that can be read by an external PC. The default operation setting has data output to the Out SRAM for recording, and output to the data output connectors. The pinout of headers J11 and J12 is per Tables 2-5 and 2-6. To provide maximum performance when connecting the output data from the GC101 to the inputs of a DAC EVM, the user should place 100 Ohm series dampenig resistors as close as possible to the J11 and J12 headers.

The Out SRAM mode is controlled through the OutMemory FPGA. The Out SRAM can be used as a pattern generator if the DIMM Output is isolated and the Out Memory mode is playback. The normal mode is capture (record) where the DIMM Output is recorded to the Out SRAM and registered for output to the Output data connector.

Output data can be driven from the EVM, from the DIMM output, from the InMemory bus, or from the OutMemory. The selection is software controlled. The software script commands CLKMUXS, CLKMUXSWOSKEW, and OUTMEMSEL control these settings.

The pinout description for J11 and J12 are shown in Table 6 and Table 7.

Table 6. Output Connector J11 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	OD15	O	Output data bit 15	2	GND	-	System Ground
3	OD14		Output data bit 14	4			
5	OD13		Output data bit 13	6			
7	OD12		Output data bit 12	8			
9	OD11		Output data bit 11	10			
11	OD10		Output data bit 10	12			
13	OD9		Output data bit 9	14			
15	OD8		Output data bit 8	16			
17	OD7		Output data bit 7	18			
19	OD6		Output data bit 6	20			
21	OD5		Output data bit 5	22			
23	OD4		Output data bit 4	24			
25	OD3		Output data bit 3	26			
27	OD2		Output data bit 2	28			
29	OD1		Output data bit 1	30			
31	OD0		Output data bit 0 (LSB)	32			
33	OUTCLKA		Output Clock	34			
35	OSPS		Spare Output	36			
37	OSYNCOUT		Output Sync	38			
39	OUTCLKB		Output Clock	40			

Table 7. Output Connector J12 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	OD31	O	Output data bit 31 (MSB)	2	GND	-	System Ground
3	OD30		Output data bit 30	4			
5	OD29		Output data bit 29	6			
7	OD28		Output data bit 28	8			
9	OD27		Output data bit 27	10			
11	OD26		Output data bit 26	12			
13	OD25		Output data bit 25	14			
15	OD24		Output data bit 24	16			
17	OD23		Output data bit 23	18			
19	OD22		Output data bit 22	20			
21	OD21		Output data bit 21	22			
23	OD20		Output data bit 20	24			
25	OD19		Output data bit 19	26			
27	OD18		Output data bit 18	28			
29	OD17		Output data bit 17	30			
31	OD16		Output data bit 16	32			
33	OUTCLKA		Output Clock	34			
35	OSPS6		Spare Output	36			
37	OSYNCOUT		Output Sync	38			
39	OUTCLKD		Output Clock	40			

4.7 DAUGHTER CARD DIMM CONNECTOR

The GC101 EVM has a 168 pin DIMM style connector for mating to the different daughter boards. The groups of signals this connector provides are:

```
32bit signal input (D31.. D0) 4 sync/special strobe
input (D35..D32, where D32 is the Sync Input)
 Input Clock and/or
Differential Clock

32bit signal output (D31..D0)
 4
sync/special strobe output (D35..D32 where D32 is the Sync Output)
 Output
Clock and/or Differential Clock

JTAG - TMS, TDI, TCK, TDO
SPI
– SCL, SCData, (*) CNTLSP

LocalBus
 RST#, CE#, RD#, WR#,
CNTLSP
 Address[10..0]
 Data[15..0]

EVM-Type, Binary Code
of Daughter card installed
 3.3v (VDUT1) , 2.5v power (VDUT2), DGND
VDUT3, VDUT4, AGND
```

The control port interface to the DIMM Connector is a register mapped interface in the Control FPGA. The control port has 16bit data, 11-bit address, and chip selects. A spare chip select is output to the DIMM for future usage.

The DWR8,DRD8 are the 8-bit control port read and write commands. The DWR16, and DRD16 are the 16-bit control port read and write commands. See the script commands in Appendix A for more detail.

With the use of script files, the input sync signal used by the Daughter board can be modified to occur as follows:

1. During the beginning of every new frame of data (default case for most experiments).
2. Once during the start of the first frame of data only. This requires the user to generate a custom script file that would disable the sync operation of the internal functions (FIR, NCO, CIC) of the GC5016 device. See the GC5016 data sheet for more information.

The script file would then be entered in the command line box of the GC5016 GUI and executed after the loaded experiment is running.

The DIMM pinout is shown in Table 8.

Table 8. DIMM Connector J7 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	DID31	I	DIMM Input Data Bit 31	85	DOD31	O	DIMM Output Data Bit 31
2	DID30	I	DIMM Input Data Bit 30	86	DOD30	O	DIMM Output Data Bit 30
3	DID29	I	DIMM Input Data Bit 29	87	DOD29	O	DIMM Output Data Bit 29
4	DID28	I	DIMM Input Data Bit 28	88	DOD28	O	DIMM Output Data Bit 28
5	DID27	I	DIMM Input Data Bit 27	89	DOD27	O	DIMM Output Data Bit 27
6	DID26	I	DIMM Input Data Bit 26	90	DOD26	O	DIMM Output Data Bit 26
7	DID25	I	DIMM Input Data Bit 25	91	DOD25	O	DIMM Output Data Bit 25
8	DID24	I	DIMM Input Data Bit 24	92	DOD24	O	DIMM Output Data Bit 24
9	DID23	I	DIMM Input Data Bit 23	93	DOD23	O	DIMM Output Data Bit 23

Table 8. DIMM Connector J7 Pinout (continued)

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
10	DID22	I	DIMM Input Data Bit 22	94	DOD22	O	DIMM Output Data Bit 22
11	DID21	I	DIMM Input Data Bit 21	95	DOD21	O	DIMM Output Data Bit 21
12	DID20	I	DIMM Input Data Bit 20	96	DOD20	O	DIMM Output Data Bit 20
13	DID19	I	DIMM Input Data Bit 19	97	DOD19	O	DIMM Output Data Bit 19
14	DID18	I	DIMM Input Data Bit 18	98	DOD18	O	DIMM Output Data Bit 18
15	DID17	I	DIMM Input Data Bit 17	99	DOD17	O	DIMM Output Data Bit 17
16	DID16	I	DIMM Input Data Bit 16	100	DOD16	O	DIMM Output Data Bit 16
17	DID15	I	DIMM Input Data Bit 15	101	DOD15	O	DIMM Output Data Bit 15
18	DID14	I	DIMM Input Data Bit 14	102	DOD14	O	DIMM Output Data Bit 14
19	DID13	I	DIMM Input Data Bit 13	103	DOD13	O	DIMM Output Data Bit 13
20	DID12	I	DIMM Input Data Bit 12	104	DOD12	O	DIMM Output Data Bit 12
21	DID11	I	DIMM Input Data Bit 11	105	DOD11	O	DIMM Output Data Bit 11
22	DID10	I	DIMM Input Data Bit 10	106	DOD10	O	DIMM Output Data Bit 10
23	DID9	I	DIMM Input Data Bit 9	107	DOD9	O	DIMM Output Data Bit 9
24	DID8	I	DIMM Input Data Bit 8	108	DOD8	O	DIMM Output Data Bit 8
25	DID7	I	DIMM Input Data Bit 7	109	DOD7	O	DIMM Output Data Bit 7
26	DID6	I	DIMM Input Data Bit 6	110	DOD6	O	DIMM Output Data Bit 6
27	DID5	I	DIMM Input Data Bit 5	111	DOD5	O	DIMM Output Data Bit 5
28	DID4	I	DIMM Input Data Bit 4	112	DOD4	O	DIMM Output Data Bit 4
29	DID3	I	DIMM Input Data Bit 3	113	DOD3	O	DIMM Output Data Bit 3
30	DID2	I	DIMM Input Data Bit 2	114	DOD2	O	DIMM Output Data Bit 2
31	DID1	I	DIMM Input Data Bit 1	115	DOD1	O	DIMM Output Data Bit 1
32	DID0	I	DIMM Input Data Bit 0 (LSB)	116	DOD0	O	DIMM Output Data Bit 0
33	GND	-	System ground	117	GND	-	System Ground
34	ICLK9A	I	Input clock	118	CLKOUT+	O	Output clock
35	ICLK9B	I	Input clock inverted	119	CLKOUT-	O	Output clock inverted
36	GND	-	System ground	120	GND	-	System ground
37	DISYNC	I	Input data sync	121	DOSYNCOUT	O	Output data sync
38	NC	-	No Connect	122	NC	-	No Connect
39	DISP1	I	DIMM Square Input	123	DOSP5	O	DIMM Spare Output
40	DISP2	I	DIMM Square Input	124	DOSP6	O	DIMM Spare Output
41	DISP3	I	DIMM Square Input	125	DOSP7	O	DIMM Spare Output
42	NC	-	No Connect	126	NC	-	No Connect
43	GND	-	System ground	127	TMS	I	JTAG test mode select
44	GND	-	System ground	128	TDI	I	JTAG serial input data
45	GND	-	System ground	129	TDO	O	JTAG serial output data
46	GND	-	System ground	130	TCLK	O	JTAG serial clock
47	GND	-	System ground	131	GND	-	System ground
48	GND	-	System ground	132	SCL	I	Serial data clock
49	GND	-	System ground	133	SCDATA	I	Serial data
50	GND	-	System ground	134	RST_	I	Reset (active low)
51	VDUT1	I	Regulated 3.3 VDC	135	CE_	I	Chip enable (active low)
52	VDUT1	I	Regulated 3.3 VDC	136	WR_	I	Write enable (active low)
53	VDUT1	I	Regulated 3.3 VDC	137	RD_	I	Read enable (active low)
54	VDUT1	I	Regulated 3.3 VDC	138	CNTLSP	I/O	Spare control

Table 8. DIMM Connector J7 Pinout (continued)

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
55	VDUT1	I	Regulated 3.3 VDC	139	GND	-	System ground
56	GND	-	System ground	140	A[10]	I	Control address bit 10
57	GND	-	System ground	141	A[9]	I	Control address bit 9
58	GND	-	System ground	142	A[8]	I	Control address bit 8
59	GND	-	System ground	143	A[7]	I	Control address bit 7
60	GND	-	System ground	144	A[6]	I	Control address bit 6
61	GND	-	System ground	145	A[5]	I	Control address bit 5
62	VDUT3(1)	I	VDC FROM J16	146	A[4]	I	Control address bit 4
63	VDUT3(1)	I	VDC FROM J16	147	A[3]	I	Control address bit 3
64	GND	-	System ground	148	A[2]	I	Control address bit 2
65	GND	-	System ground	149	A[1]	I	Control address bit 1
66	GND	-	System ground	150	A[0]	I	Control address bit 0
67	VDUT2	I	Regulated 2.5 VDC	151	GND	-	System ground
68	VDUT2	I	Regulated 2.5 VDC	152	D[0]	I/O	Control data i/o bit 0
69	VDUT2	I	Regulated 2.5 VDC	153	D[1]	I/O	Control data i/o bit 1
70	VDUT2	I	Regulated 2.5 VDC	154	D[2]	I/O	Control data i/o bit 2
71	GND	-	System ground	155	D[3]	I/O	Control data i/o bit 3
72	GND	-	System ground	156	D[4]	I/O	Control data i/o bit 4
73	VDUT4(1)	I	VDC from J18	157	D[5]	I/O	Control data i/o bit 5
74	VDUT4(1)	I	VDC from J18	158	D[6]	I/O	Control data i/o bit 6
75	AGND(1)	-	Analog ground from J17	159	D[7]	I/O	Control data i/o bit 7
76	AGND(1)	-	Analog ground from J17	160	D[8]	I/O	Control data i/o bit 8
77	EVMT4	O	EVM TYPE ID BIT 4	161	D[9]	I/O	Control data i/o bit 9
78	EVMT3	O	EVM TYPE ID BIT 3	162	D[10]	I/O	Control data i/o bit 10
79	EVMT2	O	EVM TYPE ID BIT 2	163	D[11]	I/O	Control data i/o bit 11
80	EVMT1	O	EVM TYPE ID BIT 1	164	D[12]	I/O	Control data i/o bit 12
81	EVMT0	O	EVM TYPE ID BIT 0	165	D[13]	I/O	Control data i/o bit 13
82	GND	-	System ground	166	D[14]	I/O	Control data i/o bit 14
83	GND	-	System ground	167	D[15]	I/O	Control data i/o bit 15
84	3.3V	-	3.3 VDC	168	GND	-	System ground

(1) VDUT3, VDUT4, and AGND are provided for future mixed signal applications

4.8 PARALLEL PORT INTERFACE

The GC101 EVM has a 25 pin parallel port connector (J14) to allow it to interface to a standard computer parallel port. The pinout of J14 is shown in Table 9.

Table 9. Parallel Port Connector J14 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	STROBEN	I	Data Strobe	2	PDB0	I/O	Data Bit 0
3	PDB1	I/O	Data Bit 1	4	PDB2	I/O	Data Bit 2
5	PDB3	I/O	Data Bit 3	6	PDB4	I/O	Data Bit 4
7	PDB5	I/O	Data Bit 5	8	PDB6	I/O	Data Bit 6
9	PDB7	I/O	Data Bit 7	10	INTN	O	Acknowledge
11	WAITN	O	Busy	12	U1	O	Paper end

Table 9. Parallel Port Connector J14 Pinout (continued)

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
13	U2	O	Select	14	DSTBN	I	Auto Feed
15	U3	O	Error	16	RSTN	I	Initialize
17	ASTBN	I	Select Input	18	GND	-	System Ground
19	GND	-	System ground	20	GND	-	System Ground
21	GND	-	System ground	22	GND	-	System Ground
23	GND	-	System ground	24	GND	-	System Ground
25	GND	-	System ground				

The parallel port signals are buffered by U44 before going to the Control FPGA. The Control FPGA implements a multi-address portion of the ECP standard. Single and Block software commands are sent to the EVM from the host PC. The target returns with the requested data for a read command.

4.9 JTAG CONNECTOR

The GC101 EVM has a set of resistors that allow the JTAG chain to include the serial EPROM1, serial EPROM2, InMemory FPGA, Control FPGA, OutMemoryFPGA, SRAMs, and the Daughter card. The default JTAG connection is used to program the Serial FPGA EPROMs. The pinout description for J13 is shown in Table 10.

Table 10. JTAG Connector J13 Pinout

PIN NO.	SIGNAL	TYPE	DESCRIPTION	PIN NO.	SIGNAL	TYPE	DESCRIPTION
1	TCK	I	Clock	2	GND	-	System Ground
3	TDO	O	Data from Device	4	VCC	I	System Power
5	TMS	I	JTAG State Machine Control	6	VCC	I	System Power
7	NC	-	No Connect	8	NC	-	No Connect
9	TDI	I	Data to Device	10	GND	-	System Ground

4.10 CONTROL FPGA

The Control FPGA interfaces between the IEEE1284 ECP port, and the GC101 EVM Baseboard. The Control FPGA responds to addresses within the range of the FPGA. This develops the programming blocks used to control the GC101 EVM and the Daughter card. The Control FPGA Block Diagram is shown in Figure 7.

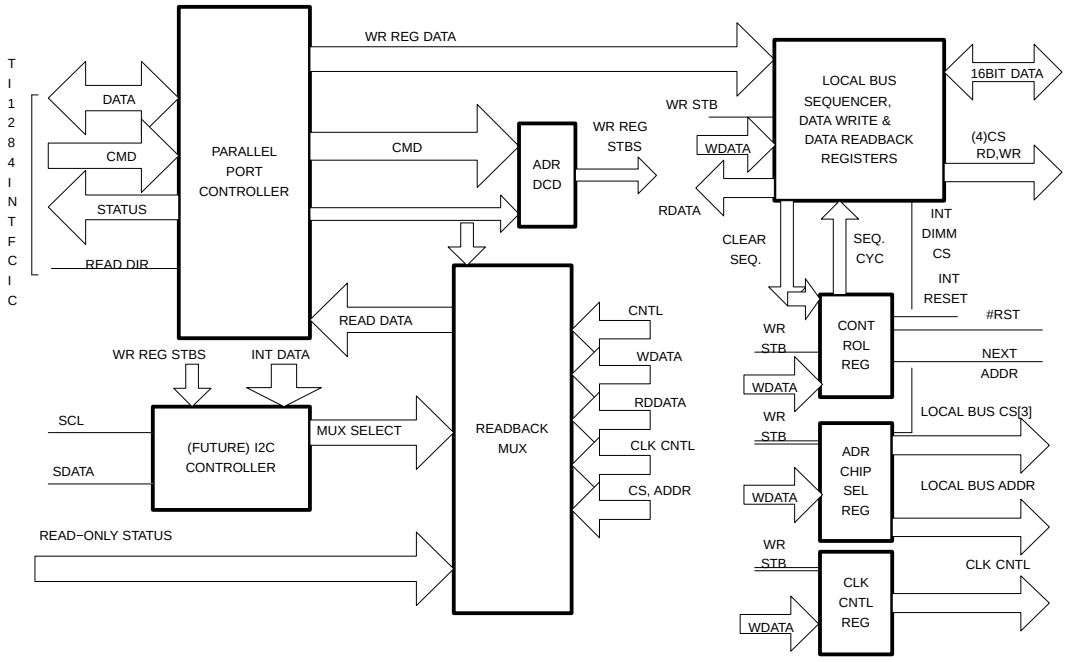


Figure 7. Control PLD Block Diagram

The Control FPGA is made up of several blocks. The Control FPGA is address mapped using the parallel port interface. See the Appendix B for the Control FPGA registers bit definitions.

The Control FPGA sections are:

- IEEE1284 ECP parallel port to Control FPGA Interface
- Address and Chip Select Registers and Logic
- Local Bus Sequencer
- Digital IO Control Registers
- Readback Multiplexer
- (Future) SPI I2C Controller

The Parallel Port Controller and Readback Multiplexer are the Host PC interface to the GC101 EVM. The CNTLFPGAWR and CNTLFPGARD commands in the script file software are used to set the registers. The registers can be set in groups and sequences to write to the Local Bus, Control the Digital IO, Control the clock multiplexer and Analog PLL, and to control the clock skew/ Divider/ PLL Control values.

The software commands CFPGAWR, and CFPGARD are used to write and read the Control FPGA registers.

The Address registers have two 8 bit registers to select and control the 4 chip selects and 12bit address bus.

Separate Chip Select logic is provided for the Control FPGA, Input Memory FPGA, Output Memory FPGA, Daughter board DIMM, and a spare Chip Select. The Chip Select decoding is done after the address register. The spare Chip Select is labelled A11.

The Local Bus Sequencer can provide both 8bit and 16bit interface cycles. The Local Bus Sequencer assumes that the Address bus and Chip Selects are set up before the Local Bus cycle. The Local Bus Sequencer is controlled through the Control FPGA Status register (offset 1). The Local Bus Sequencer can provide either single cycle, sequenced cycle, or continuous cycle capability. Single Cycle is achieved by the Control Register Command Bits being cleared after the Local Bus Sequence.

The Local Bus Sequence operates at the 40Mhz clock, and uses the two 8 bit Data Write registers and two 8 bit Data Read Registers to write or read a value. The Write and Read Sequence timing provides at least one clock cycle to precharge the bus for write operations, and two clock cycles for the device-being-read to precharge the bus for the read operation.

The Local Bus sequences are controlled through software commands for each category Daughter card Control Bus, In Memory FPGA, and Out Memory FPGA. The Memory FPGA Local Bus commands are:

- MEMFPGAWR16
- INMEMFPGAWR16
- OUTMEMFPGAWR16
- MEMFPGARD16
- INMEMFPGARD16
- OUTMEMFPGARD16
- MEMFPGAWR8
- INMEMFPGAWR8
- OUTMEMFPGAWR8
- MEMFPGARD8
- INMEMFPGARD8
- OUTMEMFPGARD8

The Daughter card DIMM Local Bus Commands are:

- DWR8
- DRD8
- DWR16
- DRD16
- DCM8
- DCM16
- DWR16PCS

The Digital IO Control Registers provide digital controls over several different operations on the GC101 EVM:

Digital Input Clock Selection – analog switches select the input clock from the SMA connector, internal Oscillator, or cable clock connection. This is controlled through the CLKMUXS, CLKMUXSWOSKEW, and INCLKSEL software commands. (C0, C1, C2)

Analog PLL Multplier Selection – The selected Digital Input Clock (10 – 27Mhz) is routed to the Analog PLL Multiplier. The Analog Multiplier provides clock multiplication of 1,2,4,6,8,10, or 12x. This is controlled through the CLKMUXS, CLKMUXSWOSKEW, and INANGPLL software commands (C3, 4, 5, 6).

Digital Input PLL Clock Selection – The Analog PLL Output or the selected Digital input clock is used to generate the Input Clock for the GC101. The software commands CLKMUXS, CLKMUXSWOSKEW, and INPLLCLKSEL control this feature (CT10).

Digital Input PLL Clock Rate Selection – The Digital Input PLL has several operating ranges, these are controlled through software commands CLKMUXS, CLKMUXSWOSKEW, and INCLKRATE. (CT0, CT1)

Digital Input PLL Skew Control Selection – There are 5 controlled banks of clock drivers. The control can provide small clock offset times, used to signal propagation delays. These are controlled through software commands PLLSKEW, and CLKMUXS. (CT2,3, 4, 5, 6, 7, 8, 9, and 11)

Digital Input PLL Divider Control Selection – The 4 main clock driver sections can have divided clocks. This is a future feature, and has not been used (ie the default is divide by 1). The software commands are CLKMUXS, and INPLLDIV. (CT13, 14, 16, ICLKSEL)

Digital Input Bus Data Control Selection – The external digital input, or the InMemory Bus can be selected for input to the Daughter card In Bus. The CLKMUXS, CLKMUXSWOSKEW, and INMEMSEL software commands control this feature. (C8, C13)

Sync Input Control Selection – The sync input for the In Bus can be selected from the In Mem, external digital cable, or SMA input. The software commands CLKMUXS, CLKMUXSWOSKEW, SYNCSEL control the selections. Note: The In Memory FPGA can also generate a Memory Sync, or pass the DIMM Sync Output back to the Sync Input. The In Memory FPGA features are not currently used. (C8, C9, and C10)

Test Output Control Selection – The InBus can be connected to the OutBus for test purposes. The CLKMUXS, CLKMUXSWOSKEW, and OUTMEMSEL commands control this feature. (C11)

DIMM Output to OutBus Selection – The Daughter card OutBus can be connected to the OutMem bus. This is a normal signal path. The CLKMUXS, CLKMUXSWOSKEW, and OUTMEMSEL control this feature. (C12)

OutMemBus Enable Selection – The Output Memory can be isolated or connected to the OutBus. The OutMemBus is normally enabled, and is isolated for Output Memory playback or access from the OutMem FPGA. This is controlled through software commands CLKMUXS, CLKMUXSWOSKEW, and OUTMEMSEL. (C14)

Output Clock Selection – The Output Clock can be selected from the Daughter card or a buffered input clock. This is controlled through the software commands CLKMUXS, CLKMUXSWOSKEW, and OUTCLKSEL. (CTT11)

Digital Output PLL Clock Selection – The 4x interpolated Analog PLL Output or the selected Digital input clock is selected and input to the Output Digital PLL. The software commands CLKMUXS, CLKMUXSWOSKEW, and OUTPLLCLKSEL control this feature (OCLKSEL).

Digital Output PLL Clock Rate Selection – The Digital Output PLL has several operating ranges. These are controlled through software commands CLKMUXS, CLKMUXSWOSKEW, and OUTCLKRATE. (CTT0, CTT1)

Digital Output PLL Skew Control Selection – There are 4 controlled banks of clock drivers. The control can provide small clock offset times, used to signal propagation delays. These are controlled through software commands PLLSKEW, and CLKMUXS. (CTT2,3, 4, 5, 6, 7, 8, and 9)

Digital Output PLL Divider Control Selection – The 4 main clock driver sections can have divided clocks. This is a future feature, and has not been used (ie the default is divide by 1). The software commands are CLKMUXS, and OUTPLLDIV. (OPLLD4)

4.10.1 INTERNAL CONTROL BUS

The GC101 EVM Internal Control Bus is generated by the Control FPGA from Parallel Port Commands. The Internal Control Bus is a 16bit data, 12 bit address, WR#, RD#, RST#, CE#, synchronous control bus. The 16bit data is bidirectional. The WR#, RD#, RST# are static control signals. The RST# is a registered bit in the Control FPGA. The WR# and RD# are controlled through the Local Bus Sequencer. The 12 bit Address CNTLSP, A[10..0] are registers in the Control FPGA. There are two 8 bit registers for both Read Monitoring and Write values for the 16 bit control bus.

The internal sequencer is controlled through the main control register. The state machine has a read and write cycle, and provides a self-clear when the cycle is complete.

In a write cycle, the address, chip select, and data registers are loaded before the control register write.

In a read cycle, the address and chip select are loaded before the control register read. Separate latched registers store the read-data values. A special control bit passes back through the parallel port logic to indicate when a local bus cycle is complete.

There are separate CE#s for the Control, Input Memory, DIMM, and Output Memory FPGAs.

The software commands can provide one-cycle, block-cycles, or continuous cycles.

4.11 INPUT MEMORY FPGA

The In Memory FPGA controls the Input SRAM bank, and communicates with the EVM internal Local Bus. The Input Memory FPGA Block Diagram is shown in Figure 8.

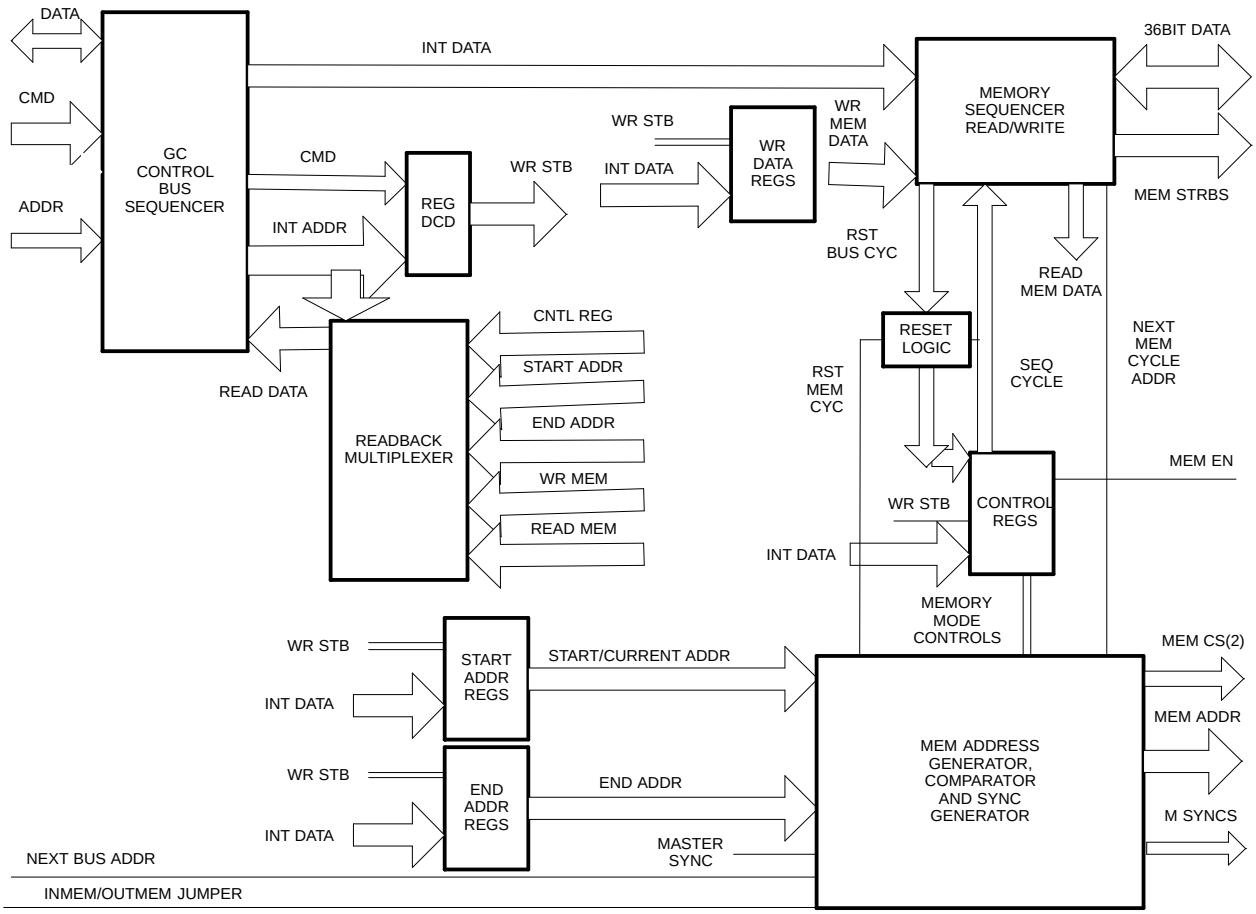


Figure 8. Input Memory FPGA Block Diagram

The Input Memory contains 36 data bits, used to provide stimulus for the daughter card. The Input Memory data and special bits are organized as 32bit data, sync, and 3 special bits. Input Memory has several operating modes:

Playback – the stored data in the Input Memory SRAM is read-out by the InMemory FPGA and sent to the In DIMM bus.

Record – The external digital input is recorded into the Input Memory SRAM. The data may be sent to the In DIMM bus.

Bypass – The external digital input is registered and sent to the In DIMM bus.

The Input data register, InSRAM tristate data switch, one or two banks of SRAM, and the InMemory FPGA make up the Input Memory. The output of the Input Memory is sent to the daughter card, and to the Test Bypass register.

The In Memory FPGA has a start address, and number of cycles counter. The In Memory FPGA outputs an address every 4th clock cycle, to load the address in the Input SRAM. The SRAM increments the intermediate addresses. The Record and Playback data sizes must be evenly divisible by 4.

The Input Memory data switches are controlled through the CLKMUXS, CLKMUXSWOSKEW, and INMEMSEL software commands.

The Local Bus Sequence responds to the Control FPGA Local Bus signals, and writes or reads to internal Memory FPGA registers. See Appendix C for the address definitions of the InMemory and OutMemory FPGA's . The Read back Multiplexer is used to scan the register results and return the values under program control.

The Local Bus Control signals are:

- GCA[10..0] – Local Bus Address
- GCCNTLSP – Local Bus Address A11
- GCC[15..0] – Bidirectional Data D15..0
- GCCEN – Chip Select Active Low
- GCREN – Read Strobe Active Low
- GCWEN – Write Strobe Active Low
- GCRSTN – Bus Reset Active Low

Note:

The Control and Status Register of the Memory FPGA requires two writes to control the Memory Sequencer. The first write is the data to be written with the Valid x2000 set to 0. The second transfer has the same data bits, but the x2000 Valid is used by the internal logic to latch the results.

Note:

x1000 in the Control register is used to identify that 1M SRAMs are being used versus 512K SRAMs.

Note:

A special signal NADDR is used with DMA cycles to load the Memory FPGA by transmitting the next data, and the address is incremented within the InMemory FPGA.

The Memory Sequencer has controls that force a single SRAM write or read cycle, or multiple cycle Writes or Reads. The Memory Sequencer controls the internal In Memory FPGA data translators for the 36bit data, 22 bit address, and chip selects for 2 banks of memory. The Memory Sequencer works with the Control signals and counter advance for the Address Generator. The Memory Sequencer generates the SRAM control signals:

MA[21..0] — Memory Address

MBSEL[1..0] — Memory Bank Select (one signal per bank)

MD[35..33, 31..0] — Bidirectional SRAM Data

MSYNC [M32] — Bidirectional SRAM Data

MADVLD — Memory Address Auto Advance, Load active low

MOEN — Memory Output Enable (Read) Active Low

MWEN — Memory Write Enable Active Low

MCKEN — Memory Clock Enable Active Low

MEN — Memory Cycle Enable Active Low

MASYNC — InSRAM Master Address Sync (goes to OutMemory FPGA)

The Memory Sequencer can generate single SRAM cycles, and multiple SRAM cycles. The single cycle, follows a standard SRAM device. In the multiple cycle mode, the Sequencer generates a 4 cycle address, and write or read cycle. The 4 cycles include incrementing the address generator at the appropriate state.

The Sequencer has a status indication from the DMA COUNT. When DMA COUNT overflows, the continuous cycle is terminated.

The Memory Address can be selected from the Address register, or from an internal address counter. The Memory address register value is loaded into the address counter, when the memory sequencer is started.

If a single address read or write is performed, then the address is not modified. If a block of addresses is read or written, the address counter can provide the updated addresses, synchronized with the memory sequencer controls.

The Address Generator contains two counters: an address counter that increments, also containing decode logic that converts the upper address into the two Bank Select signals, and a DMACOUNTer that accumulates the number of 4 cycle – events, to determine if the record cycle is complete.

The Memory Sequencer has single cycle, block transfer, and continuous cycles. The Memory Sequencer has self-clearing control bits, that allow a single cycle or block cycle to complete. The single cycle is used to read and write to the SRAM from the Control FPGA, through the Memory FPGA registers.

There are two Start address registers:

Upper 8 bit address

Lower 16bit address

When the SRAM is used in a block read (playback) or block write (snapshot record) mode, the SRAM provides the offset addresses 1, 2, and 3. The base address modulo 4 is provided from the Memory FPGA through the address counter.

In the block count mode, a separate counter counts up to overflow, indicating that a block cycle has completed. The DMA Counter, is enabled through the Memory Sequencer. The DMA Counter is loaded with a value of (BlockSize / 4) – 1. When the Memory Sequencer has processed four memory cycles, the DMA count advance is used to advance the block count. When the DMA count overflows, the Memory sequencer can reset the block control run value.

There are several synchronization elements for the Address Generators. Each time the DMA cycle completes, the address counter is reloaded with the start address register value. When this occurs, the Input Memory FPGA outputs a special memory sync signal. This signal is wired from the Input Memory FPGA to the Output for syncrhonization..

The memory FPGA can be synchronized to the DIMM Output Sync, and External Sync, or not synchronized.

4.12 OUTPUT MEMORY FPGA

The Output Memory contains 36 data bits to monitor the daughter card or provide digital output stimulus. The Output Memory data and special bits are organized as 32bit data, sync, and 3 special bits. The Output Memory has several operating modes:

Playback – the stored data in the Output Memory SRAM is read-out by the OutMemory FPGA and sent to the Output Connector (ie GC101 is used as a pattern generator).

Record – The input or daughter card digital output is recorded into the Output Memory SRAM. The output data is also sent to Output Connectors.

Bypass – The input or daughter card digital output is output to the Output Connectors.

The daughter card data register, OutSRAM tristate data switch, one or two banks of SRAM, and the OutMemory FPGA make up the Output Memory.

The Out Memory FPGA is very similar in function to the In Memory FPGA. The primary difference is that the Out Memory FPGA can be synchronized with the InMemory Master Sync or daughter card Sync output.

The Out Memory FPGA has a start address, and number of cycles counter. The Out Memory FPGA outputs an address every 4th clock cycle, to load the address in the Input SRAM. The SRAM increments the intermediate addresses. The Record and Playback data sizes must be evenly divisible by 4.

The Output Memory data switches are controlled through the CLKMUXS, CLKMUXSWOSKEW, and OUTMEMSEL software commands.

See the descriptive section 2.1.16. The synchronization signals for the Out Memory FPGA are different from the InMemory FPGA.

Note:

Due to the special synchronization to the DIMM and the Input Memory FPGA, the Output Memory FPGA is a different FPGA program.

5 SCHEMATICS

This chapter contains the GC101 EVM schematic diagrams.

Appendix A SCRIPT SOFTWARE COMMANDS (USED WITH TEXT USER INTERFACE)

The Scripting language is a set of text lines, used for programming the GC101 EVM. The script language mostly writes data to a register or memory location. There are cases where a delay or register read are implemented. The register read values are read back to the Text User Interface console and to the logging files for file based script processing.

1.0 Control FPGA Write and Read Register Script Commands

2.0 Memory FPGA (In and Out) Write and Read Register Script Commands

3.0 Memory (In and Out) Write and Read Script Commands

4.0 Memory (In and Out) Block Write Script Commands

5.0 Memory (In and Out) File Write and Read Script Commands

6.0 Memory (In and Out) Address Generator Count Write Script Commands

7.0 Clock, Sync, and Datapath Controls

8.0 Synchronous Delay Controls

9.0 DIMM Device Local Bus Programming

10.0 Read Script Commands – reads script lines from a text file

11.0 Miscellaneous Commands

The scripts are organized into groups that perform specific EVM functions. All of the functions for a demonstration or experiment are normally kept within a named folder.

Setup.script — Clock setup for GC101 EVM

Name_addressgensize_setup.script — Control FPGA, clock, sync, data, Memory FPGA setup

Name.setup — Collection of scripts to program, load, collect data, and output a file

Name.capture — Collection of scripts to reprogram address generator, collect data, and output a file

Name_addressgensize_setup2.script — Memory FPGA setup for recapture

Outmem_isol_xx.script — Reconfigures the output memory to upload the data back to the host PC

A.1 CONTROL FPGA WRITE AND READ REGISTER SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
1.1	CFPGAWR	Control FPGA Byte Write Command
1.2	CFPGARD	Control FPGA Byte Read Command

A.1.1 CFPGAWR

Arg1)Hexadecimal BYTE address
(Arg2)Hexadecimal BYTE data

This command is used to write directly to the Control FPGA internal registers.

A.1.2 CFPGARD

(Arg1)Hexadecimal BYTE address

This command is used to read from the Control FPGA internal registers.

A.2 MEMORY FPGA (IN AND OUT) WRITE AND READ REGISTER SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
2.1	MEMFPGAWR16	InMemory or OutMemory FPGA Word Write Command
2.2	INMEMFPGAWR16	InMemory FPGA Word Write Command
2.3	OUTMEMFPGAWR16	OutMemory FPGA Word Write Command
2.4	MEMFPGARD16	InMemory or OutMemory FPGA Word Read Command
2.5	INMEMFPGARD16	InMemory FPGA Word Read Command
2.6	OUTMEMFPGARD16	OutMemory FPGA Word Read Command
2.7	MEMFPGAWR8	InMemory or OutMemory FPGA Byte Write Command
2.8	INMEMFPGAWR8	InMemory FPGA Byte Write Command
2.9	OUTMEMFPGAWR8	OutMemory FPGA Byte Write Command
2.10	MEMFPGARD8	InMemory or OutMemory FPGA Byte Read Command
2.11	INMEMFPGARD8	InMemory FPGA Byte Read Command
2.12	OUTMEMFPGARD8	OutMemory FPGA Byte Read Command

A.2.1 MEMFPGAWR16

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal BYTE address
(Arg3)Hexadecimal WORD data

This command is used to write to the Memory FPGA internal registers over the EVM Local Bus.

A.2.2 INMEMFPGAWR16

(Arg1)Hexadecimal BYTE address
(Arg2)Hexadecimal WORD data

This command is used to write to the InMemory FPGA internal registers over the EVM Local Bus.

A.2.3 OUTMEMFPGAWR16

(Arg1)Hexadecimal BYTE address
(Arg2)Hexadecimal WORD data

This command is used to write to the OutMemory FPGA internal registers over the EVM Local Bus.

A.2.4 MEMFPGARD16

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal BYTE address

This command is used to read from the Memory FPGA internal registers over the EVM Local Bus.

A.2.5 INMEMFPGARD16

(Arg1)Hexadecimal BYTE address

This command is used to read from the InMemory FPGA internal registers over the EVM Local Bus.

A.2.6 OUTMEMFPGARD16

(Arg1)Hexadecimal BYTE address

A.2.7 MEMFPGAWR8

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal BYTE address
(Arg3)Hexadecimal BYTE data

This command is used to write to the Memory FPGA internal registers over the EVM Local Bus.

A.2.8 INMEMFPGAWR8

(Arg1)Hexadecimal BYTE address
(Arg2)Hexadecimal BYTE data

This command is used to write to the InMemory FPGA internal registers over the EVM Local Bus.

A.2.9 OUTMEMFPGAWR8

(Arg1)Hexadecimal BYTE address
(Arg2)Hexadecimal BYTE data

This command is used to write to the OutMemory FPGA internal registers over the EVM Local Bus.

A.2.10 MEMFPGARD8

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal BYTE address

This command is used to read from the Memory FPGA internal registers over the EVM Local Bus.

A.2.11 INMEMFPGARD8

(Arg1)Hexadecimal BYTE address

This command is used to read from the InMemory FPGA internal registers over the EVM Local Bus.

A.2.12 OUTMEMFPGARD8

(Arg1)Hexadecimal BYTE address

This command is used to read from the OutMemory FPGA internal registers over the EVM Local Bus.

A.3 MEMORY (IN AND OUT) WRITE AND READ SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
3.1	MEMWR	InSRAMor OutSRAM Write Command; 36 bits
3.2	MEMRD	InSRAM or OutSRAM Read Command; 36 bits
3.3	INMEMWR	InSRAM Write Command; 36 bits
3.4	INMEMRD	InSRAM Read Command; 36 bits
3.5	INMEMWRNS	InSRAM Write Command; 32 bits
3.6	MEMRDNS	InSRAM Read Command; 32 bits
3.7	OUTMEMWR	OutSRAM Write Command; 36 bits
3.8	OUTMEMRD	OutSRAM Read Command; 36 bits
3.9	OUTMEMWRNS	OutSRAM Write Command; 32 bits
3.10	OUTMEMRDNS	OutSRAM Read Command; 32 bits

A.3.1 MEMWR

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT address
(Arg3)Hexadecimal UINT D31..0
(Arg4)Hexadecimal UINT D35..32

This command is used to write to the In or Out Memory.

A.3.2 MEMRD

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT address

This command is used to read from the In or Out Memory.

A.3.3 INMEMWR

(Arg1)Hexadecimal INT address
(Arg2)Hexadecimal UINT D31..0 data
(Arg3)Hexadecimal UINT D35..32 data

This command is used to write to the InMemory.

A.3.4 INMEMRD

(Arg1)Hexadecimal INT address

This command is used to read from the InMemory.

A.3.5 INMEMWRNS

(Arg1)Hexadecimal INT address
(Arg2)Hexadecimal UINT D31..0 data

This command is used to write to D31..D0 of the InMemory.

A.3.6 INMEMRDNS

(Arg1)Hexadecimal INT address

This command is used to read D31..D0 from the InMemory.

A.3.7 OUTMEMWR

(Arg1)Hexadecimal INT address
(Arg2)Hexadecimal UINT D31..0 data
(Arg3)Hexadecimal UINT D35..32 data

This command is used to write to the OutMemory.

A.3.8 OUTMEMRD

(Arg1)Hexadecimal INT address

This command is used to read from the OutMemory.

A.3.9 OUTMEMWRNS

(Arg1)Hexadecimal INT address
(Arg2)Hexadecimal UINT D31..0 data

This command is used to write to D31..D0 of the OutMemory.

A.3.10 OUTMEMRDNS

(Arg1)Hexadecimal INT address

This command is used to read D31..D0 from the OutMemory.

A.4 MEMORY (IN AND OUT) BLOCK WRITE SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
4.1	BLKMEMWR	Writes a block of SRAM with a constant value
4.2	INMEMBLKWR	Writes a block of InMemory SRAM with a constant value
4.3	OUTMEMBLKWR	Writes a block of OutMemory SRAM with a constant value

A.4.1 BLKMEMWR

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT Start address
(Arg3)Hexadecimal number of integer cycles
(Arg4)Hexadecimal UINT D31..0 data
(Arg5)Hexadecimal UINT D35..32 data

This command is used to write a constant value to a range of In or OutMemory.

A.4.2 INMEMBLKWR

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)Hexadecimal UINT D31..0 data
(Arg4)Hexadecimal UINT D35..32 data

This command is used to write a constant value to a range of InMemory.

A.4.3 OUTMEMBLKWR

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)Hexadecimal UINT D31..0 data
(Arg4)Hexadecimal UINT D35..32 data

This command is used to write a constant value to a range of OutMemory.

A.5 MEMORY (IN AND OUT) FILE WRITE AND READ SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
5.1	LSRAM	Read a Hex-text file, Write to SRAM
5.2	LSRAM 2	Read a 2 column special & data Hex-text file, Write to SRAM
5.3	RSRAM	Read SRAM, Write to Hex-text file
5.4	RSRAM 2	Read SRAM, Write to a 2 column special & data Hex-text file
5.5	INMEMWRFNS	Load InMem SRAM from File; 32bit data
5.6	INMEMWRF	Load InMem SRAM from File; 36bit data
5.7	INMEMRDFNS	Read InMem SRAM write to File; 32bit data
5.8	INMEMRDF	Read InMem SRAM write to File; 36bit data
5.9	OUTMEMWRFNS	Load OutMem SRAM from File; 32bit data
5.10	OUTMEMWRF	Load OutMem SRAM from File; 36bit data

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
5.11	OUTMEMRDFNS	Read OutMem SRAM write to File; 32bit data
5.12	OUTMEMRDF	Read OutMem SRAM write to File; 36bit data

A.5.1 LSRAM

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT Start address
(Arg3)Hexadecimal number of integer cycles
(Arg4)text string – local filename

This function writes the hex file data to D31..0 of the specified memory and address.

The file is read for 'integer cycles' or until end of file, which ever is smaller. The data format is a single column of hex digits.

A.5.2 LSRAM2

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT Start address
(Arg3)Hexadecimal number of integer cycles
(Arg4)text string – local filename

This function writes the hex file data to D31..0 and D35..32, of the specified memory and address. The file is read for 'integer cycles' or until end of file, which ever is smaller. The data format is two column of hex digits D31..0 and D35..32.

A.5.3 RSRAM

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT Start address
(Arg3)Hexadecimal number of integer cycles
(Arg4)text string – local filename

This function reads from the SRAM and writes to the file, data D31..0.

The file is written for 'integer cycles'. The data format is a single column of hex digits.

A.5.4 RSRAM2

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal INT Start address
(Arg3)Hexadecimal number of integer cycles
(Arg4)text string – local filename

This function reads from the SRAM and writes data D31..0 and D35..32 to the file.

The file is written for 'integer cycles'. The data format is two column of hex digits D31..0 and D35..32.

A.5.5 INMEMWRFNS

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the InMemory SRAM from the file data D31..0.

The file is written for 'integer cycles'. The data format is a single column of hex digits.

A.5.6 INMEMWRF

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the InMemory SRAM from the file data D31..0 and D35..32.

The file is written for ‘integer cycles’. The data format is two columns of hex digits D31..0 and D35..32.

A.5.7 INMEMRDFNS

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function reads from the InMemory SRAM, and writes data D31..0 to a file.

The file is written for ‘integer cycles’. The data format is a single column of hex digits.

A.5.8 INMEMWRF

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the InMemory SRAM from the file D31..0 and D35..32.

The file is written for ‘integer cycles’. The data format is two columns of hex digits D31..0 and D35..32.

A.5.9 OUTMEMWRFNS

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the OutMemory SRAM from the file data D31..0.

The file is written for ‘integer cycles’. The data format is a single column of hex digits.

A.5.10 OUTMEMWRF

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the OutMemory SRAM from the file data D31..0 and D35..32.

The file is written for ‘integer cycles’. The data format is two columns of hex digits D31..0 and D35..32.

A.5.11 OUTMEMRDFNS

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function reads from the OutMemory SRAM, and writes data D31..0 to a file.

The file is written for ‘integer cycles’. The data format is a single column of hex digits.

A.5.12 OUTMEMWRF

(Arg1)Hexadecimal INT Start address
(Arg2)Hexadecimal number of integer cycles
(Arg3)text string – local filename

This function writes to the OutMemory SRAM from the file, D31..0 and D35..32.

The file is written for 'integer cycles'. The data format is two columns of hex digits D31..0 and D35..32.

A.6 MEMORY (IN AND OUT) ADDRESS GENERATOR COUNT WRITE SCRIPT COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
6.1	MFPGADMACNTWR	Convert Memory FPGA Count to number of transfers count; loads counter
6.2	INMFPGADMACNTWR	Convert InMemory FPGA Count to number of transfers count; loads counter
6.3	OUTMFPGADMACNTWR	Convert OutMemory FPGA Count to number of transfers count; loads counter

A.6.1 MFPGADMACNTWR

(Arg1) 1 – InMemory, 2 – OutMemory
(Arg2)Hexadecimal Count (number of transfers / 4) - 1

This function writes to the specified Memory FPGA count register.

The count register is used to size the memory for both playback and snapshot functions.

A.6.2 INMFPGADMACNTWR

(Arg1)Hexadecimal Count (number of transfers / 4) - 1

This function writes to the In Memory FPGA count register.

The count register is used to size the memory for both playback and snapshot functions.

A.6.3 OUTMFPGADMACNTWR

Arg1)Hexadecimal Count (number of transfers / 4) - 1

This function writes to the Out Memory FPGA count register.

The count register is used to size the memory for both playback and snapshot functions.

A.7 CLOCK, SYNC, AND DATAPATH CONTROLS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
7.1	CLKMUXS	Clock Setup Command; Default Dig Clock Skew (RevA)
7.2	CLKMUXSWOSKEW	Clock Setup Command; No Dig Clock Skew (RevA)
7.3	PLLSKEW	Controls the Clock Skew for the (4) Dig Clock Banks, (RevA)
7.4	SYNCSEL	Selects the Input Sync Source (*)
7.5	INCLKSEL	Selects the Input Clock Source (*)
7.6	INMEMSEL	Selects the InBus data as external or memory Provides a special Input memory data isolation to read the In Memory
7.7	INANGPLL	Controls the Input Analog PLL Multplier (*)
7.8	INPLLCLKSKEW	Controls the Input Digital PLL Clock Skew
7.9	INCLKRATE	Controls the Input Digital PLL – PLL Range (*)

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
7.10	INPLLDIV	Controls the Input Digital PLL 4 bank Clock Division
7.11	OUTCLKSEL	Selects the Output Digital PLL Clock Source from Daughterboard or Input Clock
7.12	OUTMEMSEL	Selects the Output Memory input source, provides a special test path, provides a special Out Memory isolation to read the Out Memory
7.13	OUTPLLCLKSEL	Selects the Digital Output Clock or the Analog Output PLL 4x clock
7.14	OUTCLKRATE	Controls the Output Digital PLL – PLL Range
7.15	OUTPLLDIV	Controls the Output Digital PLL 4 bank Clock Division
7.16	SYNCINRESET	Provides a special InMemory OFF Configuration to generate a Low Sync Input

A.7.1 CLKMUXS

CLKMUXS – Arg8 Clock Rate for Dig PLL, (RevA) must be a minimum of 25Mhz. Value is Clock Select * Ang PLL Rate of Ang PLL is selected

(Arg1) 1 – Input Clock Source Select
- 0 - use Internal, DIP oscillator (default is 10Mhz)
- 1 – use External SMA
- 2 – use Digital input cable

(Arg2) – Input Memory Digital Data Mode Selection
- 0 – use InMemory as data source
- 1 – use Digital Input data as data source
- 2 – special mode, used when recording to InMemory

(Arg3) – Input Sync Source Select
- 0 - use Sync input from InMemory
- 1 – use Digital Input data for sync source
- 2 – use External Sync-In SMA

(Arg4) – Output Clock Selection
- 0 – use Input Clock, used for synchronous In and OutMemory, and test modes (default)
- 1 – use DIMM Output clock

(Arg5) – OutMemory Digital Data Mode Selection
- 0 – use DIMM as data source; enable OutMemory for recording
- 1 – special test mode; use OutMemory as data source
- 2 – special mode; used when recording to InMemory
- 3 – special mode; used for InMemory -> OutMemory test
- 4 – special mode; used to write and read OutMemory from OutMemory FPGA

(Arg 6) – Input AngPLL Selection – this control takes the digital input clock select (10-27Mhz) and performs a rate multiplication.
1, 2, 4, 6, 8, 10, 12, 16

(Arg 7) – Input Digital PLL Clock Selection
- 0 – Digital Input Clock Selected (see Arg1)
- 1 – Analog PLL Clock Selected (see Arg1, 6)

(Arg 8) – Input Digital PLL Range (floating point value)
- <50e6 – Low
- <100e6 – Midrange
- >= 100e6 High

Note:

This command sets the PLLSKEW to the default value of 4,4,4,4. Use the CLKMUXSWOSKEW to set the other controlled values without changing the PLL SKEW.

A.7.2 CLKMUXSWOSKEW

Same arguments as section 7.1. This command performs the set of commands in section 7.1 without changing the PLL SKEW value.

A.7.3 PLLSKEW

This command controls the timing skew for the Digital PLL for each Clock distribution bank. The Clock Skew controls are used when the standard value 4 4 4 4 does not provide the TSetup and THold margin. Values less than 4 advance the timing. Values greater than 4 retard the timing. Since each skew control is actually a pair of 3-state pins, the control value is expressed as a number from 0 to 8

Skew#	nF1	nF0
0	L	L
1	L	Z
2	L	H
3	Z	L
4	Z	Z
5	Z	H
6	H	L
7	H	Z
8	H	H

(Arg1) – Bank1 Skew
(Arg2) – Bank 2 Skew
(Arg3) – Bank 3 Skew
(Arg4) – Bank 4 Skew
(Arg5) – 0: InPLL, 1: OutPLL

There are two Digital PLLs which is selected by the fifth argument. The circuits driven by the output of the Digital PLL's are as follows:

1. Input PLL
   a. Input FPGA, Input Registers (near 40 pin headers, used with external digital inputs).
   b. Input SRAM memory.
   c. DIMM Clock, Registers for Bypass test.
   d. Registers to DIMM, Clock to Output PLL.
2. Output PLL
   a. Output FPGA, Registers from DIMM.
   b. Output Registers for External Digital Output and Output Connector.
   c. Output Clock for External Digital Output.
   d. Output Memory SRAM.

See the Cypress CY7C994 datasheet for the skew value definitions for the 0 to 8 settings.

A.7.4 SYNCSEL

SYNCSEL – Arg1 Clock Input Sync Source Selection

(Arg1) – Input Sync Source Select

0 - use Sync input from InMemory
1 – use Digital Input data for sync source
2 – use External Sync-In SMA

A.7.5 INCLKSEL

INCLKSEL – Arg1 Input Clock Source Select

(Arg1) – Input Clock Source Select

0 - use Internal, DIP oscillator (default is 10Mhz)
1 – use External SMA
2 – use Digital input cable

A.7.6 INMEMSEL

INMEMSEL – Arg1 Input Bus Data/Mode Selection

(Arg1) – Input Memory Digital Data Mode Selection

0 – use InMemory as data source
1 – use Digital Input data as data source
2 – special mode, used when recording to InMemory

A.7.7 INANGPLL

INANGPLL – Arg1 PLL Multiplier

(Arg 6) – Input AngPLL Selection – this control takes the digital input clock select

(10-27Mhz) and performs a rate multiplication.

1, 2, 4, 6, 8, 10, 12, 16

A.7.8 INPLLCLKSEL

INPLLCLKSEL – Arg1 Select Clock input from Digital Select or Analog PLL

(Arg 1) – Input Digital PLL Clock Selection

0 – Digital Input Clock Selected (see Arg1)
1 – Analog PLL Clock Selected (see Arg1, 6)

A.7.9 INCLKRATE

INCLKRATE – Arg1 Input Digital PLL Clock Rate

(Arg 1) – Input Digital PLL Range (floating point value)

<50e6 – Low
<100e6 – Midrange
>= 100e6 High

A.7.10 INPLLDIV

INPLLDIV – Arg5, PLLBank1, PLLBank2, PLLBank3, PLLBank4, Ref

Note:
All of the PLL Banks need to be within the same range

1, 2, 3	4, 5, 6	8, 10, 12

(Arg1,2,3,4,5) 1, 2, 3, 4, 5, 6, 7, 8, 9,10, 12

The PLL Divide for the bank is normally 1 ‘1’. The divide by 2 or 3 is selected for the entire bank.

A.7.11 OUTCLKSEL

OUTCLKSEL – Arg1, Selected Output Digital PLL Clock Source

(Arg1) – Output Clock Selection

0 – use Input Clock, used for synchronous In and OutMemory, and test modes (default)
1 – use DIMM Output clock

A.7.12 OUTMEMSEL

OUTMEMSEL – Arg1 OutMemory Digital Data Mode Select

(Arg1) – OutMemory Digital Data Mode Selection

0 – use DIMM as data source; enable OutMemory for recording
1 – special test mode; use OutMemory as data source
2 – special mode; used when recording to InMemory
3 – special mode; used for InMemory -> OutMemory test
4 – special mode; used to write and read OutMemory from OutMemory FPGA

A.7.13 OUTPLLCLKSEL

OUTPLLCLKSEL – Arg1 Select the Output PLL Digital source

Currently this is not used, and the default is ‘0’

A.7.14 OUTCLKRATE

OUTCLKRATE Arg1 – Output Digital Clock PLL Range Arg1 – Clock Rate of Output Digital Clock PLL

Currently the software copies this setting from the INCLKRATE, CLKMUXS, or CLKMUXSWOSKEW value.

A.7.15 OUTPLLDIV

OUTPLLDIV – Arg1 Divide Output Clock 1,4,8

Arg1 – Output PLL Divide all banks, 1, 4, 8

A.7.16 SYNCINRESET

SYNCINRESET – No Arg

Calling this command disables the Input Sync Multiplexer, the pull-down resistor pulls the signal low.

A.8 SYNCHRONOUS DELAY CONTROLS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
8.1	WAITCFPGA	Synchronous Delay to Complete ControlFPGA Cycle
8.2	WAITINMEM	Synchronous Delay to Complete InMemoryFPGA Cycle
8.3	WAITOUTMEM	Synchronous Delay to Complete OutMemoryFPGA Cycle

These commands have no arguments. They are used to provide a synchronous delay to the completion of the FPGA cycle. The Control FPGA completes the internal local bus cycle. The Memory FPGAs complete the Snapshot or Single Memory cycles.

A.9 DIMM DEVICE LOCAL BUS PROGRAMMING

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
9.1	DWR8	DIMM Byte Write Command
9.2	DRD8	DIMM Byte Read Command
9.3	DWR16	DIMM Word Write Command
9.4	DRD16	DIMM Word Read Command
9.5	DCM8	DIMM Byte Read, Mask Compare Command
9.6	DCM16	DIMM Word Read, Mask Compare Command
9.7	DWR16PCS	DIMM Word Write Command - Pulse Chip Select

A.9.1 DWR8

(Arg1) Hex Address (BYTE)
(Arg2) Hex Data (BYTE)

This command is used to write an 8bit value to the Local Bus. The Chip Select is the DIMM Chip Select

A.9.2 DRD8

(Arg1) Hex Address (BYTE)

This command is used to read an 8bit value from the Local Bus. The Chip Select is the DIMM Chip Select.

A.9.3 DWR16

(Arg1) Hex Address (BYTE)
(Arg2) Hex Data (WORD)

This command is used to write a 16bit value to the Local Bus. The Chip Select is the DIMM Chip Select.

A.9.4 DRD16

(Arg1) Hex Address (BYTE)

This command is used to read a 16 bit value from the Local Bus. The Chip Select is the DIMM Chip Select.

A.9.5 DCM8

(Arg1) Hex Address (BYTE)
(Arg2) Mask Value (BYTE)

(Arg3) Expected Value (BYTE)
Reads an 8 bit value from address on DIMM and then masks the read value with MaskValue. If the masked output doesn't match the expected output, the DIMM error count is incremented by one. The DIMM Error count can be read with READCNT.

A.9.6 DCM16

(Arg1) Hex Address (BYTE)
(Arg2) Mask Value (WORD)
(Arg3) Expected Value (WORD)

Reads a 16 bit value from address on DIMM and then masks the read value with MaskValue. If the masked output doesn't match the expected output, the DIMM error count is incremented by one. The DIMM Error count can be read with READCNT.

A.9.7 DWR16PCS

(Arg1) Hex Address (BYTE)
(Arg2) Hex Data (WORD)

The command is used to write a 16 bit value to the Local bus. This command changes from the 3 wire standard $\overline{CS}$, $\overline{RD}$, and $\overline{WE}$, to the $\overline{CS}$, $\overline{WE}$ 2 wire mode.

The $\overline{CS}$ de-asserts to latch the write data.

A.10 READ SCRIPT COMMANDS – READS SCRIPT LINES FROM A TEXT FILE

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
10.1	RUNSCRIPT	Calls Setup Parser; passes a file name of setup commands
10.2	SETUP	Calls Setup Parser; passes a file name of setup commands
10.3	DSCRIPT	Calls DIMM Parser passes a file name of setup commands

A.10.1 RUNSCRIPT

(Arg1) ReadFilename – text filename from which to read script lines
(Arg2) LogFilename – text filename to which to write log file output

A.10.2 SETUP

(Arg1) ReadFilename – text filename from which to read script lines; writes to log file

A.10.3 DSCRIPT

(Arg1) read address from global page for checksum
(Arg2) 0: 8bit checksum, 1: 16bit checksum
(Arg3) ReadFilename – text filename from which to read script lines; writes to DIMM log file

A.11 MISCELLANEOUS COMMANDS

INDEX	FUNCTION NAME (UPPER CASE)	COMMAND PERFORMED
11.1	CLEARCNT	Register test error counter = 0
11.2	READCNT	Returns error counter value
11.3	Q	Quits script before end

A.11.1 CLEARCNT

No Arguments
Sets the DIMM Error count to zero.

A.11.2 READCNT

No Arguments
Reads the test error counter.

A.11.3 Q

No Arguments
Quits the current script at this line.

Appendix B CONTROL FPGA REGISTER DEFINITION (USED WITH TEXT USER INTERFACE)

Table B.1. Register Description

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION	PIN
0	D7-D0	RO	Electronic ID/Rev Control PLD x11	
1	D7-D0		Control /Status Register	
	D7	R/W	Next Addr - causes InMem, OutMem to use Next address mode to auto increment MemAddress	
	D6	R/W	RSTN - internal Reset (inv)	
	D5	R/W/C	WR16 - '1' to cause sequencer to perform 16bit write cycle, self clear if CLRBIT set	
	D4	R/W/C	RD16 - '1' to cause sequencer to perform 16bit read cycle, self clear if CLRBIT set	
	D3	R/W/C	WR8 - '1' to cause sequencer to perform 8bit write cycle, self clear if CLRBIT set	
	D2	R/W/C	RD8 - '1' to cause sequencer to perform 8bit read cycle, self clear if CLRBIT set	
	D1	R/W	CLRBIT - set this bit if single sequence cycle (SELF CLEAR) is used	
	D0	R/W	PULSECHIPSEL - '1' for special graychip CS, normally 0	
2	D7-D0		upper address register, chip select register, readback, includes the inverted Chip Selects	
	D7	R/W(inv read) - dec 3	Sel-InMemBusy, OutMemBusy for SelectOut(W), CSN3(DIMMCS) (RO)	
	D6	R/W(inv read) - dec 2	Decx4(W), CSN2 (decode 0 not output) (RO)	
	D5	R/W(inv read) - dec 0	Decx2(W), CSN1 (dec2) (OutMem) (RO)	
	D4	R/W(inv read) - dec 1	Decx1(W), CSN0 (dec1) (InMem) (RO)	
	D3	R/W	ASP - A11	
	D2	R/W	ADDR10	
	D1	R/W	ADDR9	
	D0	R/W	ADDR8	
3	D7-D0		lower address register	
	D7		ADDR7	
	D6		ADDR6	
	D5		ADDR5	
	D4		ADDR4	
	D3		ADDR3	
	D2		ADDR2	
	D1		ADDR1	
	D0		ADDR0	
4	D7-D0		upper data register, not bus pins - input to bus sequencer - write value	
	D7	R/W (reads reg)	D15	
	D6	R/W (reads reg)	D14	
	D5	R/W (reads reg)	D13	

Table B.1. Register Description (continued)

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION	PIN
	D4	R/W (reads reg)	D12	
	D3	R/W (reads reg)	D11	
	D2	R/W (reads reg)	D10	
	D1	R/W (reads reg)	D9	
	D0	R/W (reads reg)	D8	
5	D7-D0		lower data register, not bus pins - input to bus sequencer - write value	
	D7	R/W (reads reg)	D7	
	D6	R/W (reads reg)	D6	
	D5	R/W (reads reg)	D5	
	D4	R/W (reads reg)	D4	
	D3	R/W (reads reg)	D3	
	D2	R/W (reads reg)	D2	
	D1	R/W (reads reg)	D1	
	D0	R/W (reads reg)	D0	
6	D7-D0		upper data register, read by bus sequencer	
	D7	R/O	D15	
	D6	R/O	D14	
	D5	R/O	D13	
	D4	R/O	D12	
	D3	R/O	D11	
	D2	R/O	D10	
	D1	R/O	D9	
	D0	R/O	D8	
7	D7-D0		lower data register, read by bus sequencer	
	D7	R/O	D7	
	D6	R/O	D6	
	D5	R/O	D5	
	D4	R/O	D4	
	D3	R/O	D3	
	D2	R/O	D2	
	D1	R/O	D1	
	D0	R/O	D0	
8	D7-D0		Board Controls - these registers are combined with CTT, L/H if CTT is 0	
	D2	R/W	CTLH10 - spare	
	D1	R/W	CTLH9 - Digital PLL 4F1 Skew Control, Cypress 994	CTLH[9] : 66 : output : LVTTL
	D0	R/W	CTLH8 - Digital PLL 4F0 Skew Control, Cypress 994	CTLH[8] : 69 : output : LVTTL

Table B.1. Register Description (continued)

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION	PIN
9	D7-D0		Board Controls - these registers are combined with CTT, L/H if CTT is 0	
	D7	R/W	CTLH7 - Digital PLL 3F1 Skew Control, Cypress 994	CTLH[7] : 142 : output : LVTTL
	D6	R/W	CTLH6 - Digital PLL 3F0 Skew Control, Cypress 994	CTLH[6] : 145 : output : LVTTL
	D5	R/W	CTLH5 - Digital PLL 2F1 Skew Control, Cypress 994	CTLH[5] : 85 : output : LVTTL
	D4	R/W	CTLH4 - Digital PLL 2F0 Skew Control, Cypress 994	CTLH[4] : 60 : output : LVTTL
	D3	R/W	CTLH3 - Digital PLL 1F1 Skew Control, Cypress 994	CTLH[3] : 62 : output : LVTTL
	D2	R/W	CTLH2 - Digital PLL 1F0 Skew Control, Cypress 994	CTLH[2] : 109 : output : LVTTL
	D1	R/W	CTLH1 - Digital PLL OutputMode,Cypress 994	CTLH[1] : 65 : output : LVTTL
	D0	R/W	CTLH0 - Digital PLL Fs,Cypress 994	CTLH[0] : 61 : output : LVTTL
10	D7-D0		Board Controls - these registers are combined with CTLH, '1' tristate,'0' hiZ	
	D2		CTT10 - spare	
	D1		CTT9 - Digital PLL 4F1 Skew Control, Cypress 994 (inv, 1 to enable)	tristates merged internally in above register
	D0		CTT8 - Digital PLL 4F0 Skew Control, Cypress 994 (inv, 1 to enable)	
11	D7-D0		Board Controls - these registers are combined with CTLH, '1' tristate,'0' hiZ	
	D7	R/W	CTT7 - Digital PLL 3F1 Skew Control, Cypress 994 (inv, 1 to enable)	
	D6	R/W	CTT6 - Digital PLL 3F0 Skew Control, Cypress 994 (inv, 1 to enable)	
	D5	R/W	CTT5 - Digital PLL 2F1 Skew Control, Cypress 994 (inv, 1 to enable)	
	D4	R/W	CTT4 - Digital PLL 2F0 Skew Control, Cypress 994 (inv, 1 to enable)	
	D3	R/W	CTT3 - Digital PLL 1F1 Skew Control, Cypress 994 (inv, 1 to enable)	
	D2	R/W	CTT2 - Digital PLL 1F0 Skew Control, Cypress 994 (inv, 1 to enable)	
	D1	R/W	CTT1 - Digital PLL OutputMode,Cypress 994 (inv, 1 to enable)	
	D0	R/W	CTT0 - Digital PLL Fs,Cypress 994 (inv, 1 to enable)	
12	D7-D0		Board Controls - these registers are used for general control	
	D7	R/W	CKC23 - Fdbk Select	CKC[23] : 164 : output : LVTTL
	D6	R/W	CKC22 - selects Input Clock for test, should always be '1'	CKC[22] : 70 : output : LVTTL
	D5	R/W	CKC21 - U48 CTT Spare (ckt 4)	CKC[21] : 57 : output : LVTTL
	D4	R/W	CKC20 - U48 CTLH Spare (ckt 4)	CKC[20] : 171 : output : LVTTL
	D3	R/W	CKC19 - U48 CTT Spare (ckt 3)	CKC[19] : 56 : output : LVTTL
	D2	R/W	CKC18 - U48 CTLH Spare (ckt 3)	CKC[18] : 98 : output : LVTTL
	D1	R/W(inv read)	CKC17 - inv - '1' to enable OutMemory Transceiver	CKC[17] : 58 : output : LVTTL
	D0	R/W(inv read)	CKC16 - inv - '1' to enable InMemory Transceiver	CKC[16] : 158 : output : LVTTL
13	D7-D0		Board Controls - these registers are used for general control	
	D7	R/W(inv read)	CKC15 - inv '1' select InputClock ICK14 as output clock, used for test mode	CKC[15] : 176 : output : LVTTL
	D6	R/W(inv read)	CKC14 - inv '1' select CLKOUT- as output clock	CKC[14] : 197 : output : LVTTL
	D5	R/W(inv read)	CKC13 - inv '1' select CLKOUT+ as output clock	CKC[13] : 2 : output : LVTTL
	D4	R/W(inv read)	CKC12 - inv '1' to enable DIMMOUTBUS to OutMemBus	CKC[12] : 34 : output : LVTTL
	D3	R/W(inv read)	CKC11 - inv '1' to enable input to output test bus register	CKC[11] : 198 : output : LVTTL
	D2	R/W(inv read)	CKC10 - inv '1' to select Input Conn SYNC as Input Data Sync	CKC[10] : 33 : output : LVTTL

Table B.1. Register Description (continued)

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION		PIN
	D1	R/W(inv read)	CKC9 - inv '1' to select External Sync (SMA) as Input Data Sync		CKC[9] : 196 : output : LVTTL
	D0	R/W(inv read)	CKC8 - inv - '1' to enable Digital Input Data to InMem Bus		CKC[8] : 168 : output : LVTTL
14	D7-D0		Board Controls - these registers are used for general control		
	D7	R/W	CKC7 - Digital PLL, RefSel, '0' Clock Mux, '1' Analog PLL		
	D6	R/W	CKC6 Analog PLL S3 - input needs to be 10-27Mhz		
	D5	R/W	CKC5 Analog PLL S2		
	D4	R/W	CKC4 Analog PLL S1		
	D3	R/W	CKC3 Analog PLL S0		
			AngMult	1 2 4 6 8 10 12	
			S3	1 1 0 0 0 1 1	
			S2	0 0 1 1 1 1 1	
			S1	0 1 0 1 1 0 1	
			S0	1 0 0 0 1 1 0	
	D2	R/W(inv read)	CKC2 - inv - '1' to enable local oscillator clock		CKC[2] : 121 : output : LVTTL
	D1	R/W(inv read)	CKC1 - inv - '1' to select digital input cable clock		CKC[1] : 17 : output : LVTTL
	D0	R/W(inv read)	CKC0 - inv - '1' to select external clock		CKC[0] : 91 : output : LVTTL
15	D7-D0		Read Only Status Port		
	D7	R/O	spare - 0		nput
	D6	R/O	LOCK - Cypress PLL has Clock Lock (Output PLL) - new input pin		nput
	D5	R/O	LOCK - Cypress PLL has Clock Lock (Input PLL)		nput
	D4	R/O	EVM Type 4		nput
	D3	R/O	EVM Type 3		nput
	D2	R/O	EVM Type 2		nput
	D1	R/O	EVM Type 1		nput
	D0	R/O	EVM Type 0		nput
16	D7-D0		Board Controls - new Register for Output PLL		
	D2		CTLH30 - spare		
	D1		CTLH29 - Digital PLL 4F1 Skew Control, Cypress 994		L/H merged with tristate below for 2nd Output PLL
	D0		CTLH28 - Digital PLL 4F0 Skew Control, Cypress 994		
17	D7-D0		Board Controls - new Register for Output PLL		
	D7		CTLH27 - Digital PLL 3F1 Skew Control, Cypress 994		
	D6		CTLH26 - Digital PLL 3F0 Skew Control, Cypress 994		
	D5		CTLH25 - Digital PLL 2F1 Skew Control, Cypress 994		
	D4		CTLH24 - Digital PLL 2F0 Skew Control, Cypress 994		
	D3		CTLH23 - Digital PLL 1F1 Skew Control, Cypress 994		
	D2		CTLH22 - Digital PLL 1F0 Skew Control, Cypress 994		
	D1		CTLH21 - Digital PLL OutputMode,Cypress 994		
	D0		CTLH20 - Digital PLL Fs,Cypress 994		
18	D7-D0		Board Controls - new Register for Output PLL		
	D2	RW	CTT30 - spare		
	D1	RW	CTT29 - Digital PLL 4F1 Skew Control, Cypress 994 (inv, 1 to enable)		CTT[9] : 48 : output : LVTTL
	D0	RW	CTT28 - Digital PLL 4F0 Skew Control, Cypress 994 (inv, 1 to enable)		CTT[8] : 68 : output : LVTTL
19	D7-D0		Board Controls - new Register for Output PLL		

Table B.1. Register Description (continued)

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION	PIN
	D7	R/W	CTT27 - Digital PLL 3F1 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[7] : 94 : output : LVTTL
	D6	R/W	CTT26 - Digital PLL 3F0 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[6] : 179 : output : LVTTL
	D5	R/W	CTT25 - Digital PLL 2F1 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[5] : 54 : output : LVTTL
	D4	R/W	CTT24 - Digital PLL 2F0 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[4] : 73 : output : LVTTL
	D3	R/W	CTT23 - Digital PLL 1F1 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[3] : 71 : output : LVTTL
	D2	R/W	CTT22 - Digital PLL 1F0 Skew Control, Cypress 994 (inv, 1 to enable)	CTT[2] : 110 : output : LVTTL
	D1	R/W	CTT21 - Digital PLL OutputMode,Cypress 994 (inv, 1 to enable)	CTT[1] : 63 : output : LVTTL
	D0	R/W	CTT20 - Digital PLL Fs,Cypress 994 (inv, 1 to enable)	CTT[0] : 59 : output : LVTTL

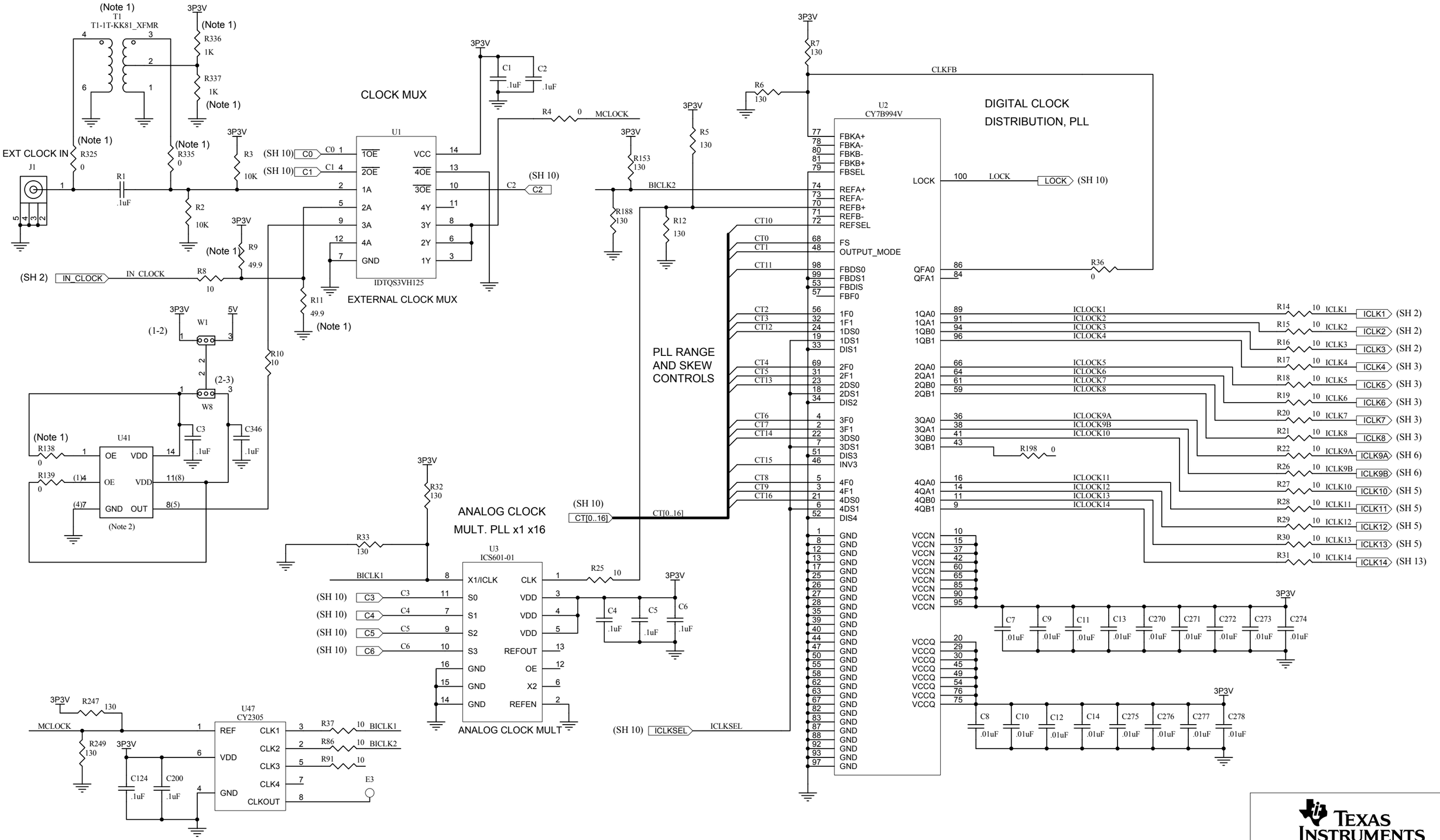
Appendix C MEMORY FPGA REGISTER DEFINITION (USED WITH TEXT USER INTERFACE)

Table C.1. Register Description

AD-DRESS	DataBit	READ/WRITE	DESCRIPTION		PIN
0	D15-D0	RO	Electronic ID/Rev Control PLD x0020		
1	D15-D0		Control /Status Register		
	D15	R/W	spare		
	D14	R/W	1' Force Sync		
	D13	R/W	1' Valid Command		
	D12	R/W	Memsize - '1' 1Mbyte. '0' 512K, affects RAM Chip Select[2]		
	D11	R/W	SyncSel x2 -	[0]ExtSync, [1]CableSync, [2]fromMasterSync, [3]ForceSync	
	D10	R/W	SyncSel x1		
			InputMemFPGA	[0]ExtSyncInput, [1] DigInSync Input, [2] NA, [3] ForceSync	
			OutputMemFPGA	[0] NA, [1] DIMM Sync, [2] from InMemFPGA Sync, [3] Force Sync	
	D9	R/W	TestRd - ReadMemBus, Memory Off, read data from mem-bus write to data read reg.		
	D8	R/W	TestWr - WriteMemBus, Memory Off, output data from write register to membus		
	D7	R/W	ClrBits - '1' for self clearing cycle		
	D6	R/W/C	PLDBlockWrite - mode control to block fill from current start address to end address		
	D5	R/W	Sync Invert - Cable or External Sync Inversion '1'		
	D4	R/W/C	PLDWrite - mode control to write to a single address, unless NextCyc is '1'		
	D3	R/W/C	PLDRead - mode control to read from a single address, unless NextCyc is '1'		
	D2	R/W/C	DIMMWrite - Record Mode, with SyncSel, records block of data (once through clear bit set), 4address adv mode		
	D1	R/W/C	DIMMRead - Playback Mode, with SyncSel generates Digital data from memory to bus, 4 addr advance mode		
	D0	R/W	RESETN - (inv) Memory Sequencer reset		
2	D15-D0	R/W	Start Address Register A15-A0		
3	D7-D0	R/W	Start Address Register A23 -A16		
			A23-A16, note, with 512K SRAM 1bank, A17,16; with (2) 512KSRAMs - A18(bank), A17,16 selects with 1M SRAMS, 1 bank A18, 17, 16		
			select; (2 banks) A19(bank) A18..16 selects		
4	D15-D0	R/W	DMA Count [15..0]		
5	D7-D0	R/W	DMA Count [23..16]		
6	D15-D0	R/W	Data Written by Sequencer to Memory or Memory Port (Test Mode) D15..0		
7	D15-D0	R/W	Memory Write Data D31..16		
8	D3-D0	R/W	Memory Write Data D35 .. 32 (SP3, Sp2, SP1, SYNC)		

Table C.1. Register Description (continued)

ADDRESS	DataBit	READ/WRITE	DESCRIPTION	PIN
9	D15-D0	R/O	Data Read by Sequencer from Memory, or in Test Mode from Memory Port D15..0	
10	D15-D0	R/O	Read Memory Port Data D31..D16	
11	D3-D0	R/O	Read Memory Port Data D35..32 (SP3,SP2, SP1, SYNC)	
12	D15-D0	R/O	MA[15..0] - Memory Address	
13	D15-D0	R/O	BANKSEL[1..0], MATCHEND, .. MA[20..16]	
14	D15-D0	R/O	End Counter Cnt[15..0]	



TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Engineer: J. SETON	Title: GC101 EVM		
Drawn By: Y. DEWONCK	DOCUMENTCONTROL #		REV: D
FILE:	DATE: 23-May-2005	SIZE:	SHEET: 1 OF: 14

INDATA

J3
40PIN_IDC

ID[0..31]

ID15 ID14 ID13 ID12 ID11 ID10 ID9 ID8 ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0 SP1

R206–R216 47.5k
R217 ID6 47.5k
R226 ID5 47.5k
R227 ID4 47.5k
R228 ID3 47.5k
R229 ID2 47.5k
R230 ID1 47.5k
R231 ID0 47.5k
R232 47.5k

3P3V
(Note 1)
R24
47.5K
ISYNC

ECLK2
ECLK1
R184
0
(Note 1)
IN_CLOCK
IN_CLOCK (SH 1)
R185
0

J5
40PIN_IDC

ID31 ID30 ID29 ID28 ID27 ID26 ID25 ID24 ID23 ID22 ID21 ID20 ID19 ID18 ID17 ID16 SP2

R234–R241 47.5k
R342 ID22 47.5k
R343 ID21 47.5k
R344 ID20 47.5k
R345 ID19 47.5k
R346 ID18 47.5k
R347 ID17 47.5k
R348 ID16 47.5k
R349 47.5k
R350 47.5k

3P3V
R35
130
R34
130
ICLK1
ICLK1 (SH 1)
U4
SN74ALVTH16374

C15 C16 C17 C18 .1uF

48	1CLK	1 OE	1	C8	C8 (SH 10)
ID0 47	1D1	1Q1	2	IBD0	
ID1 46	1D2	1Q2	3	IBD1	
45	GND	GND	4		
ID2 44	1D3	1Q3	5	IBD2	
ID3 43	1D4	1Q4	6	IBD3	
42	VCC	VCC	7		
ID4 41	1D5	1Q5	8	IBD4	
ID5 40	1D6	1Q6	9	IBD5	
39	GND	GND	10		
ID6 38	1D7	1Q7	11	IBD6	
ID7 37	1D8	1Q8	12	IBD7	
ID8 36	2D1	2Q1	13	IBD8	
ID9 35	2D2	2Q2	14	IBD9	
34	GND	GND	15		
ID10 33	2D3	2Q3	16	IBD10	
ID11 32	2D4	2Q4	17	IBD11	
31	VCC	VCC	18		
ID12 30	2D5	2Q5	19	IBD12	
ID13 29	2D6	2Q6	20	IBD13	
28	GND	GND	21		
ID14 27	2D7	2Q7	22	IBD14	
ID15 26	2D8	2Q8	23	IBD15	
25	2CLK	2 OE	24	C8	

IBD[0..15] IBD[0..15] (SH 5)
INBUS

EXT SYNC IN
J4
3P3V
R41
(Note 1)
49.9
R42
49.9

3P3V
R46
130
R45
130
ICLK2
ICLK2 (SH 1)
U7
SN74ALVTH16374

C25 C26 C27 C28 .1uF

48	1CLK	1 OE	1	C8	
ID16 47	1D1	1Q1	2	IBD16	
ID17 46	1D2	1Q2	3	IBD17	
45	GND	GND	4		
ID18 44	1D3	1Q3	5	IBD18	
ID19 43	1D4	1Q4	6	IBD19	
42	VCC	VCC	7		
ID20 41	1D5	1Q5	8	IBD20	
ID21 40	1D6	1Q6	9	IBD21	
39	GND	GND	10		
ID22 38	1D7	1Q7	11	IBD22	
ID23 37	1D8	1Q8	12	IBD23	
ID24 36	2D1	2Q1	13	IBD24	
ID25 35	2D2	2Q2	14	IBD25	
34	GND	GND	15		
ID26 33	2D3	2Q3	16	IBD26	
ID27 32	2D4	2Q4	17	IBD27	
31	VCC	VCC	18		
ID28 30	2D5	2Q5	19	IBD28	
ID29 29	2D6	2Q6	20	IBD29	
28	GND	GND	21		
ID30 27	2D7	2Q7	22	IBD30	
ID31 26	2D8	2Q8	23	IBD31	
25	2CLK	2 OE	24	C8	

IBD[16..31] IBD[16..31] (SH 5)

EXT CABLE SYNC MUX

3P3V
C19
.1uF

U5
IDTQS3VH125

(SH 10) C10	C10	1	1OE	VCC	14	
(SH 10) C9	C9	4	2OE	4OE	13	U5_13 U5_13 (SH 3)
	RSYNC	2	1A	3OE	10	U5_10 U5_10 (SH 3)
	ESYNCI	5	2A	4Y	11	
(SH 3) U5_9	U5_9	9	3A	3Y	8	
(SH 3) OBSYNCOUT	OBSYNCOUT	12	4A	2Y	6	IBSYNC IBSYNC (SH 4, 5, 7)
	GND	7		1Y	3	

INBUS
3P3V
R351
4.75K
R352
4.75K
(Note 1)

3P3V
R44
130
R43
130
ICLK3
ICLK3
U8
SN74ALVTH16374

C20 C22 C23 C24 .1uF

48	1CLK	1 OE	1		
ISYNC 47	1D1	1Q1	2	RSYNC	RSYNC (SH 3)
46	1D2	1Q2	3		
45	GND	GND	4		
EXTSYNCIN 44	1D3	1Q3	5	ESYNCI	ESYNCI (SH 3, 8)
43	1D4	1Q4	6		
42	VCC	VCC	7		
41	1D5	1Q5	8		
40	1D6	1Q6	9		
39	GND	GND	10		
(SH 3) MASTERSYNC 38	1D7	1Q7	11		
37	1D8	1Q8	12		
36	2D1	2Q1	13		
SP[1..2] SP1 35	2D2	2Q2	14	IBSP1	
34	GND	GND	15		
SP2 33	2D3	2Q3	16	IBSP2	
R48 0 32	2D4	2Q4	17	IBSP3	
31	VCC	VCC	18	IBSP[1..3]	IBSP[1..3] (SH 5)
30	2D5	2Q5	19	IBSYNC	
29	2D6	2Q6	20		
28	GND	GND	21		
27	2D7	2Q7	22		
26	2D8	2Q8	23		
ICLK3 25	2CLK	2 OE	24	C8	

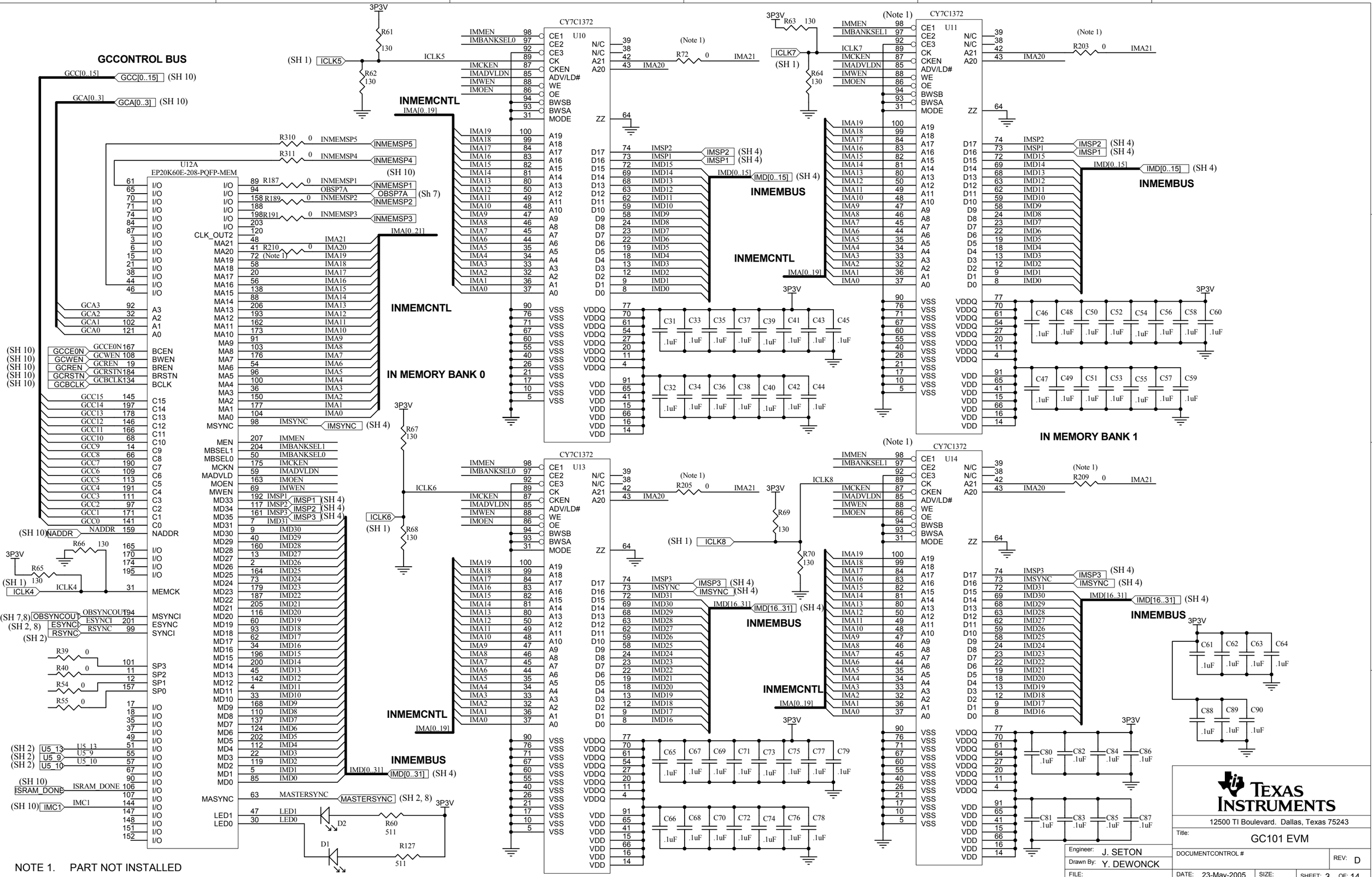
INDATA
INPLD
INBUS

J6
R47
10
EXT SYNC OUT

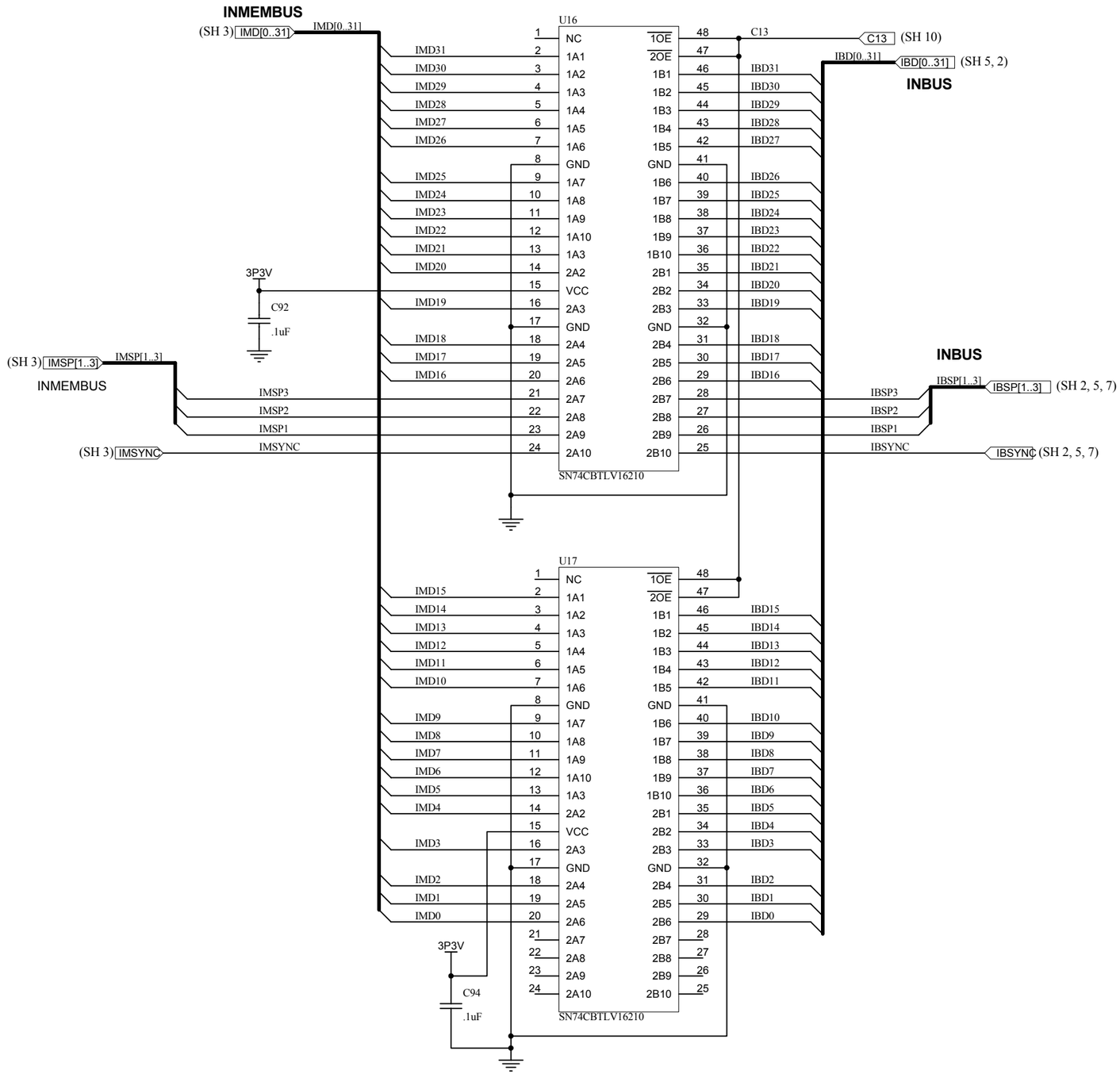
NOTE 1. PART NOT INSTALLED

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: GC101 EVM			
DOCUMENTCONTROL #			REV: D
Engineer: J. SETON			
Drawn By: Y. DEWONCK			
FILE:	DATE: 23-May-2005	SIZE:	SHEET: 2 OF: 14


GCCONTROL BUS
INMEMCNTL
IN MEMORY BANK 0
INMEMBUS
IN MEMORY BANK 1
CY7C1372
U10
U11
U13
U14
U12A
EP20K60E-208-PQFP-MEM
3P3V
(SH 10)
(SH 1)
(SH 4)
(Sh 7)
(SH 7,8)
(SH 2, 8)
(SH 2)
(Note 1)
ICLK5
ICLK6
ICLK7
ICLK8
IMA[0..19]
IMA[0..21]
IMD[0..15]
IMD[16..31]
GCC[0..15]
GCA[0..3]
NOTE 1. PART NOT INSTALLED
Engineer: J. SETON
Drawn By: Y. DEWONCK
FILE:
12500 TI Boulevard. Dallas, Texas 75243
Title: GC101 EVM
DOCUMENTCONTROL #
REV: D
DATE: 23-May-2005
SIZE:
SHEET: 3 OF: 14

INBUS TRISTATE MUX



Engineer:	J. SETON
Drawn By:	Y. DEWONCK
FILE:	

TEXAS INSTRUMENTS

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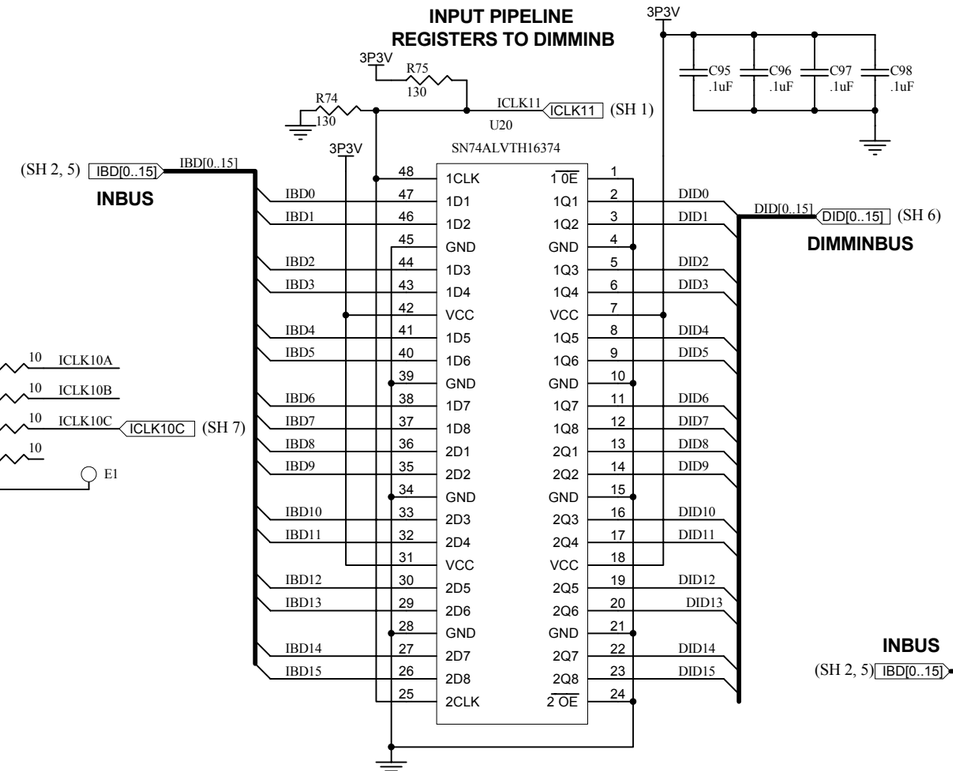
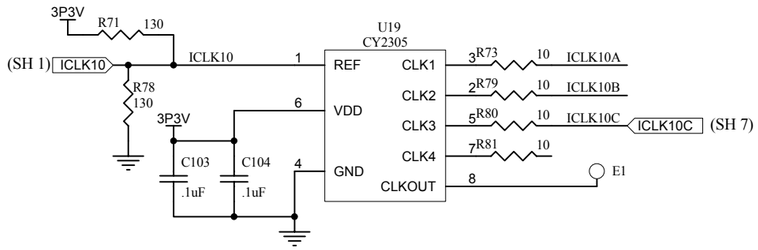
Title:	GC101 EVM		
DOCUMENTCONTROL #			REV: D
DATE: 23-May-2005	SIZE:	SHEET: 4	OF: 14

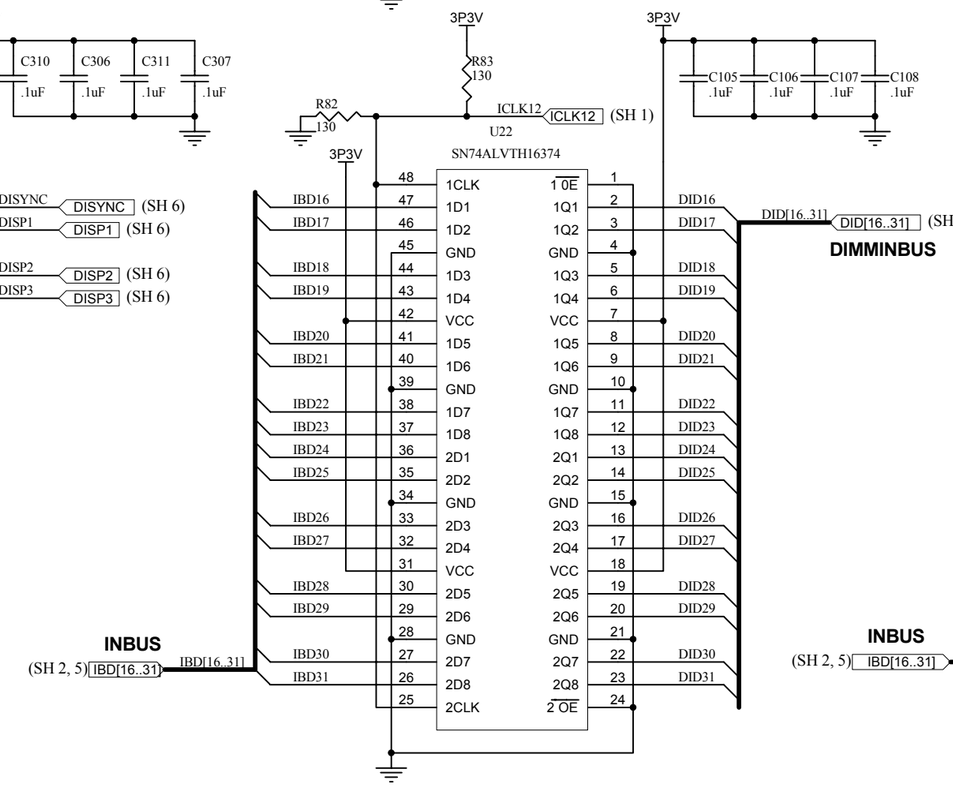
INPUT PIPELINE REGISTERS TO DIMMINB

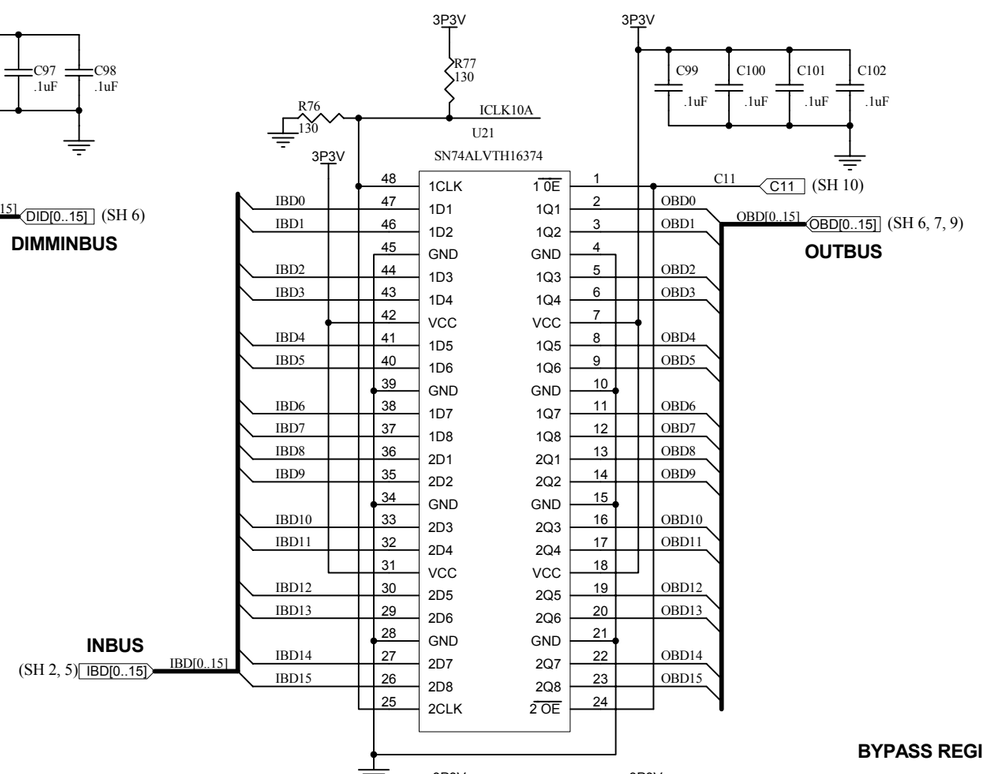


TEST MODE IN CLK BUFFER

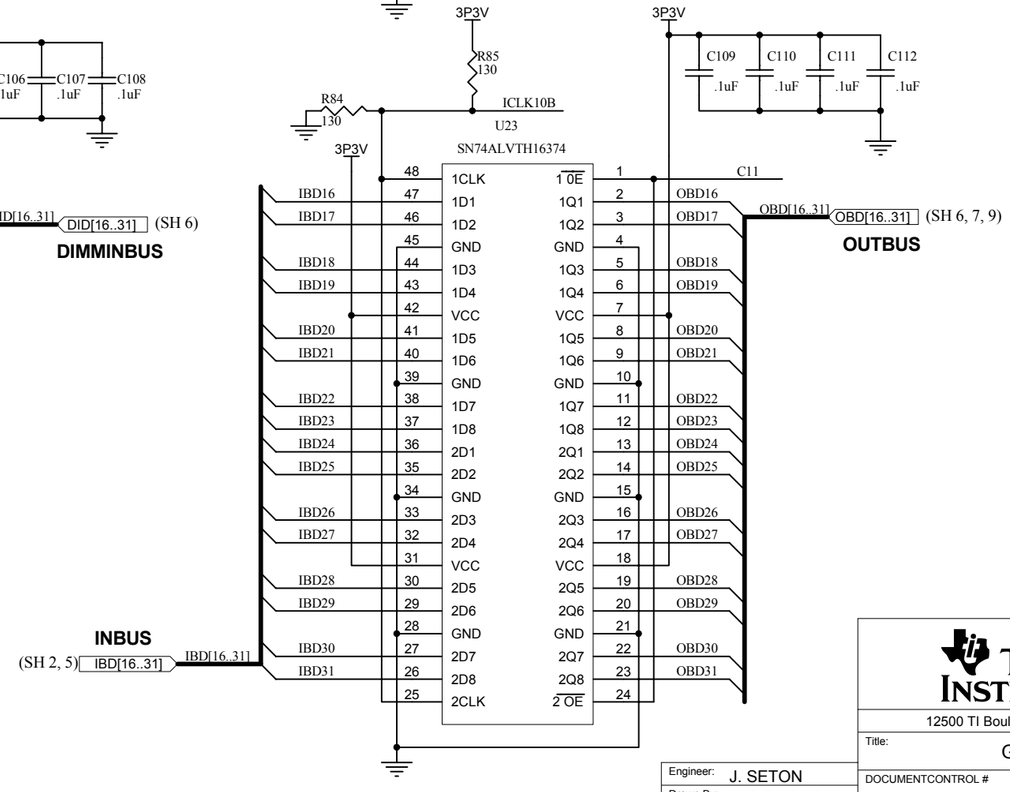


INBUS PIPELINE REGISTER TO DIMMBUS



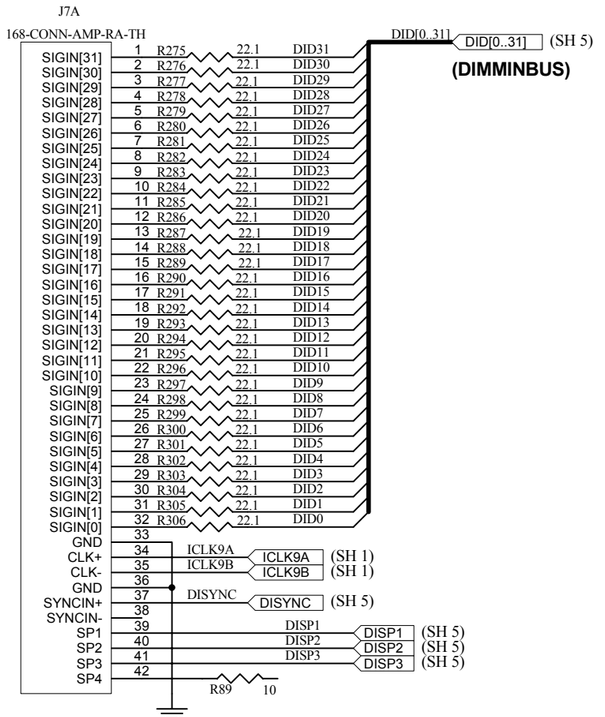


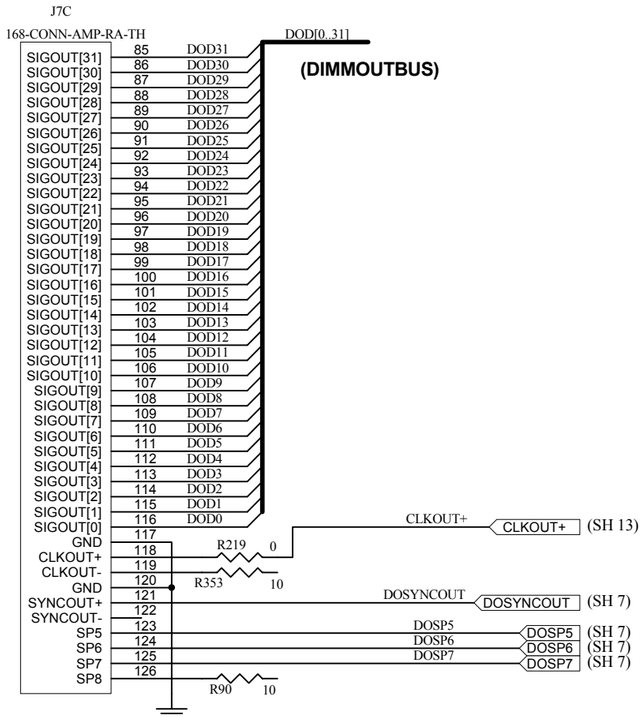
BYPASS REGISTERS FOR TEST



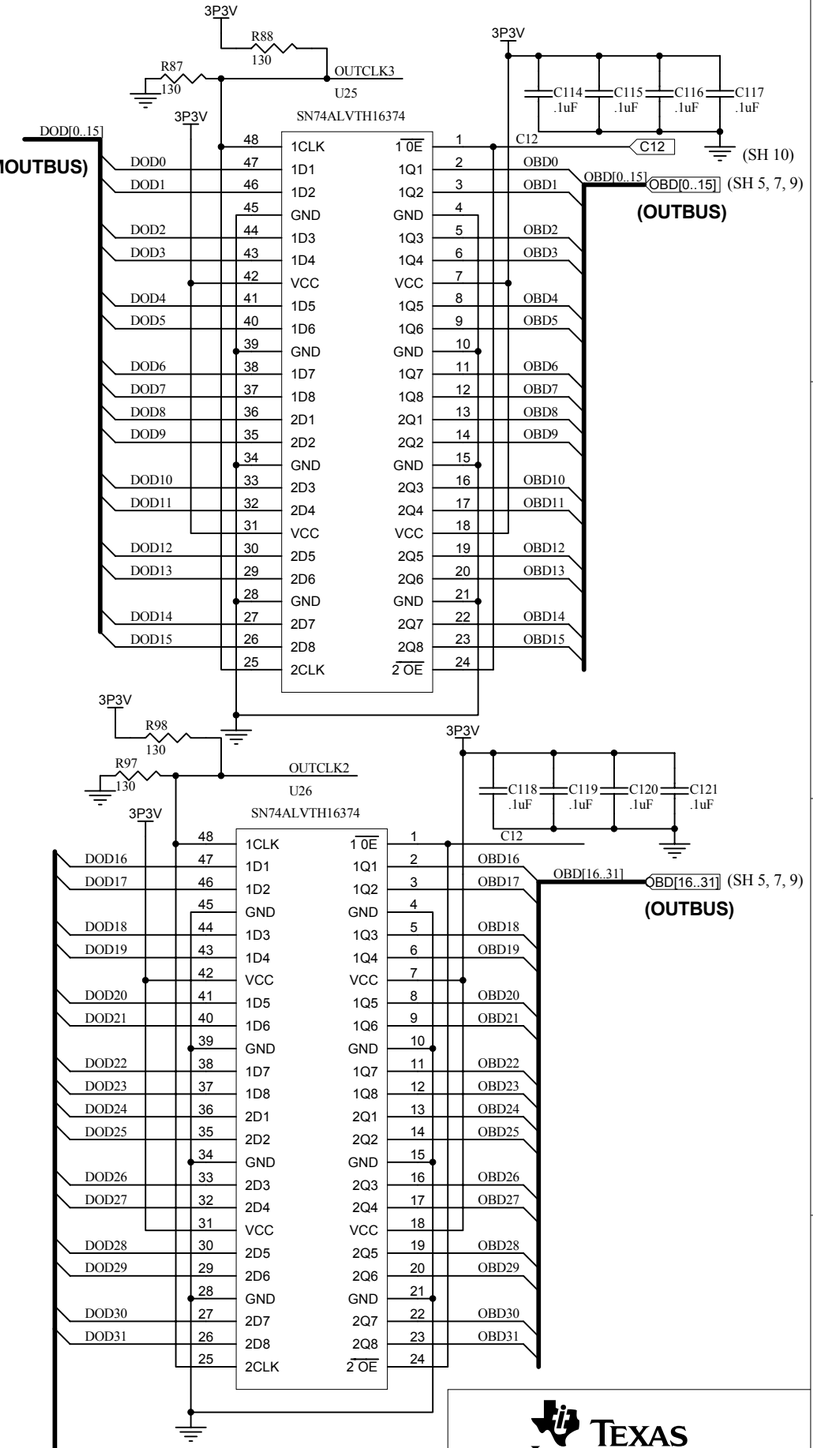
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

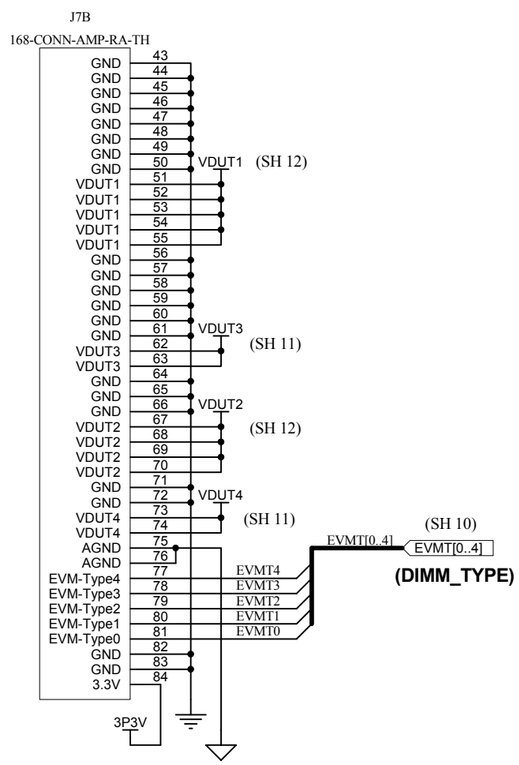
Title: GC101 EVM			
Engineer: J. SETON	DOCUMENTCONTROL #		REV: D
Drawn By: Y. DEWONCK			
FILE:	DATE: 23-May-2005	SIZE:	SHEET: 5 OF: 14

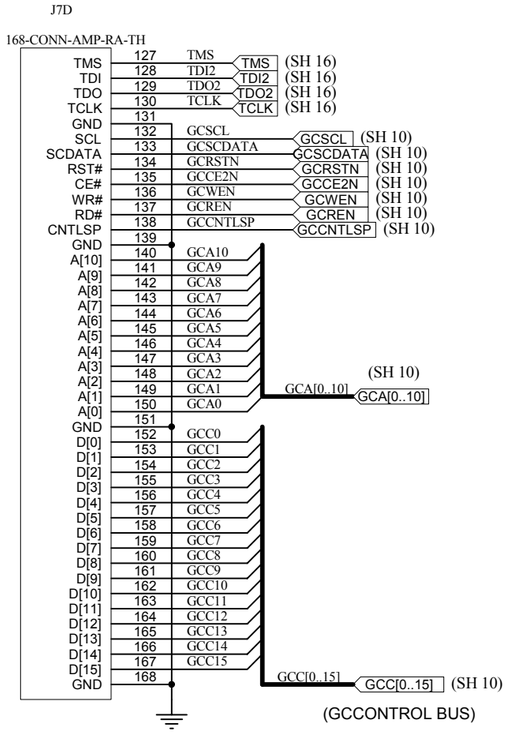




(DIMMOUTBUS)



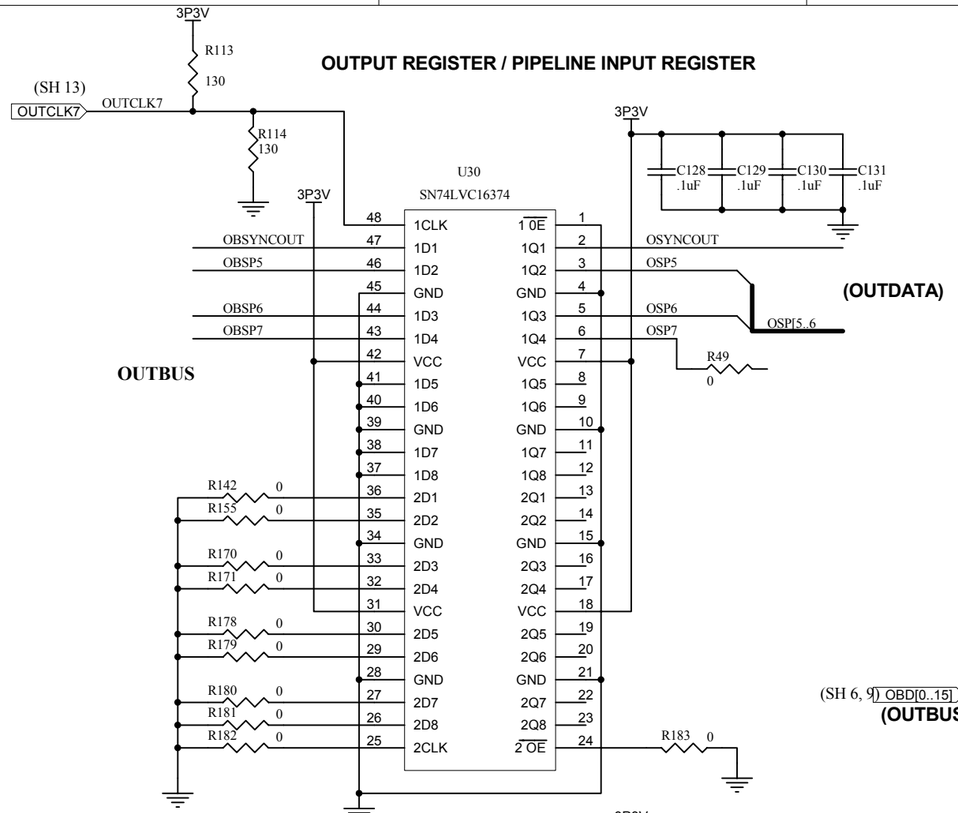


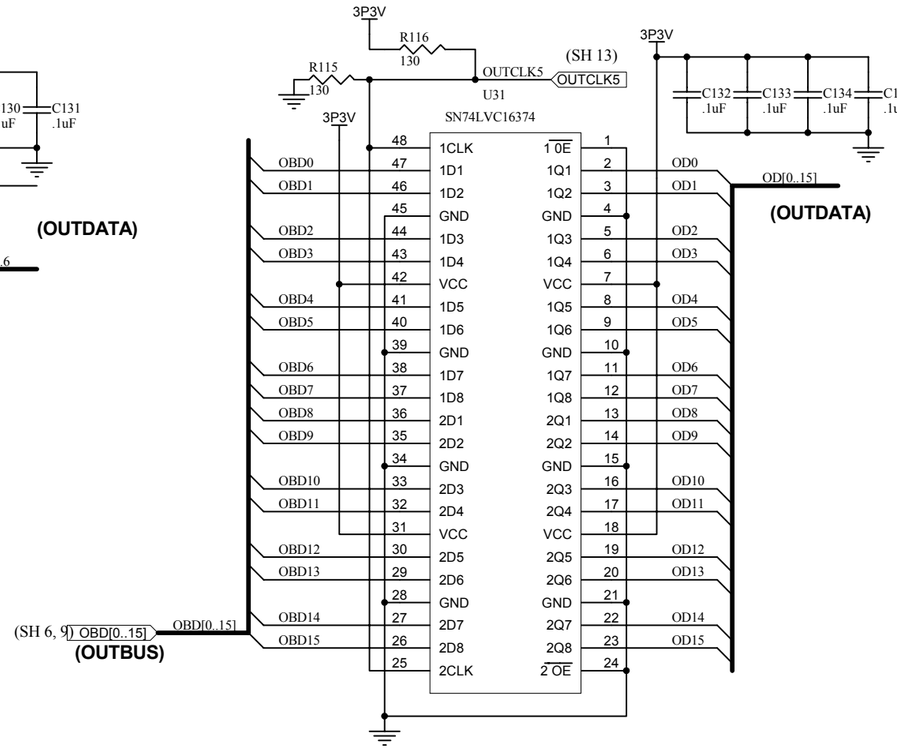


TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

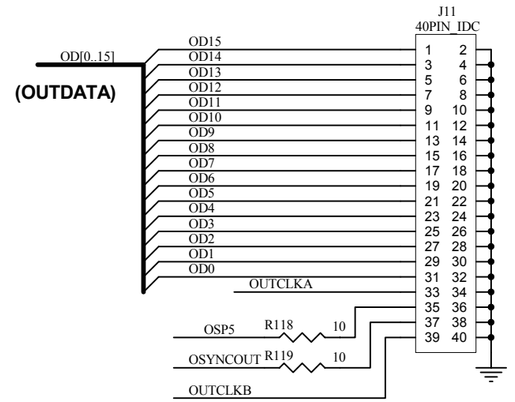
Title:	GC101 EVM
Engineer: J. SETON	
Drawn By: Y. DEWONCK	
FILE:	
DOCUMENTCONTROL #	REV: D
DATE: 23-May-2005	SIZE:
SHEET: 6 OF: 14	

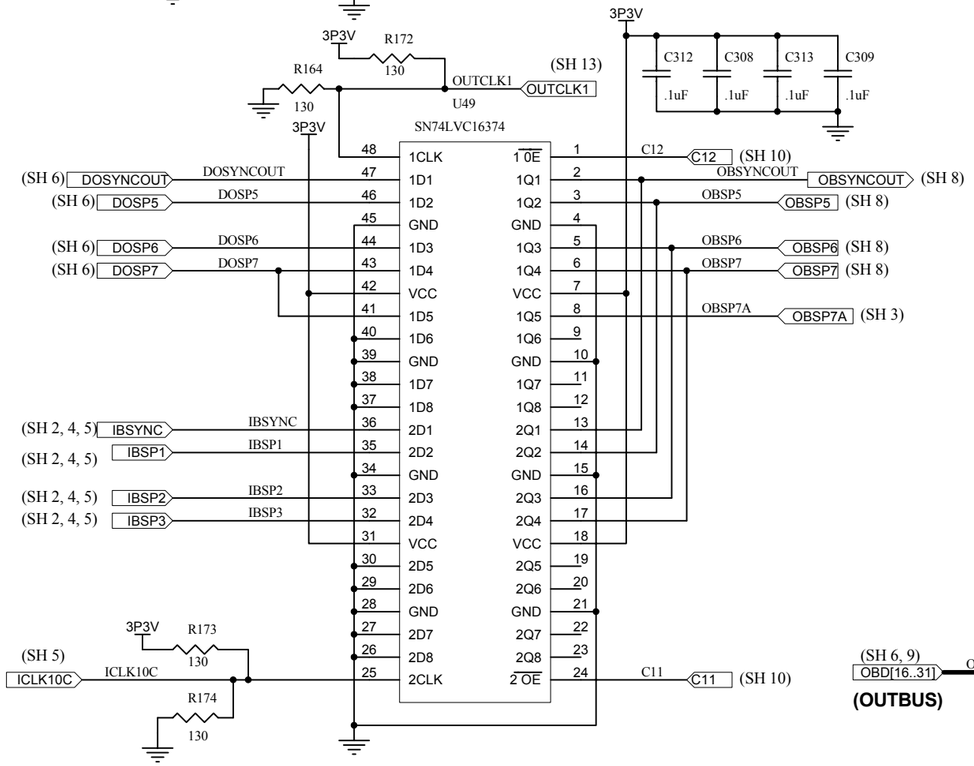
OUTPUT REGISTER / PIPELINE INPUT REGISTER

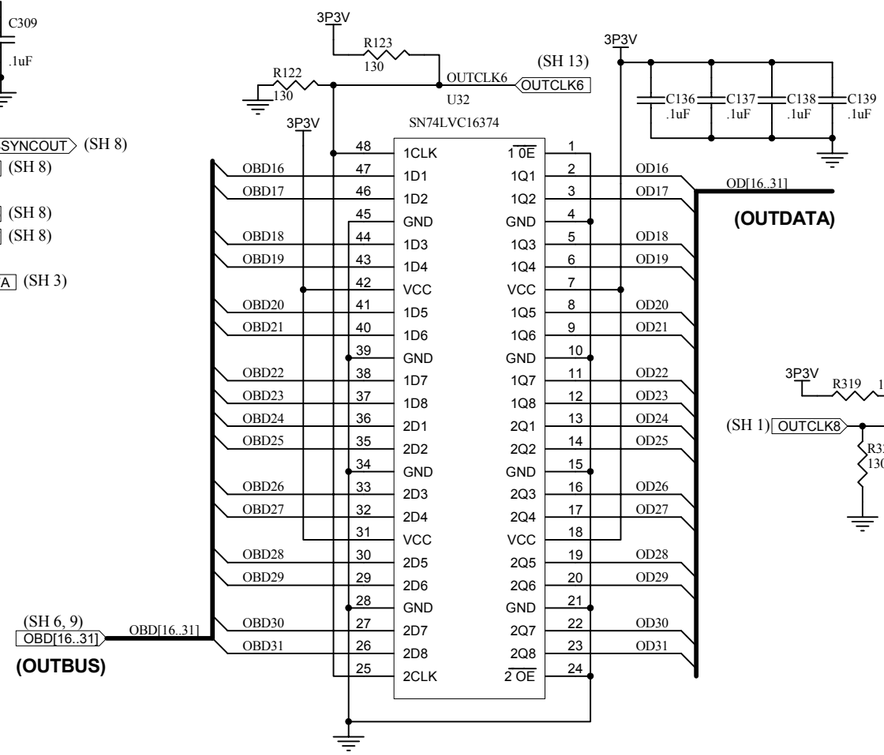


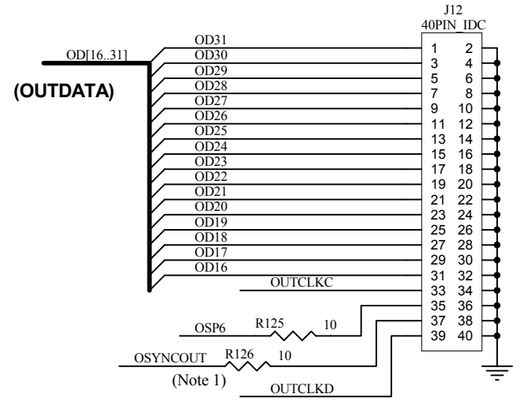


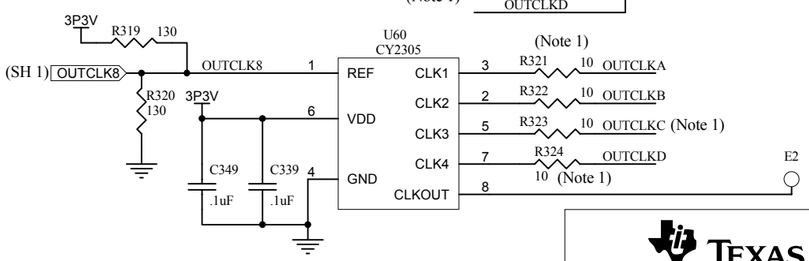
DIGITAL OUTPUT CONNECTORS







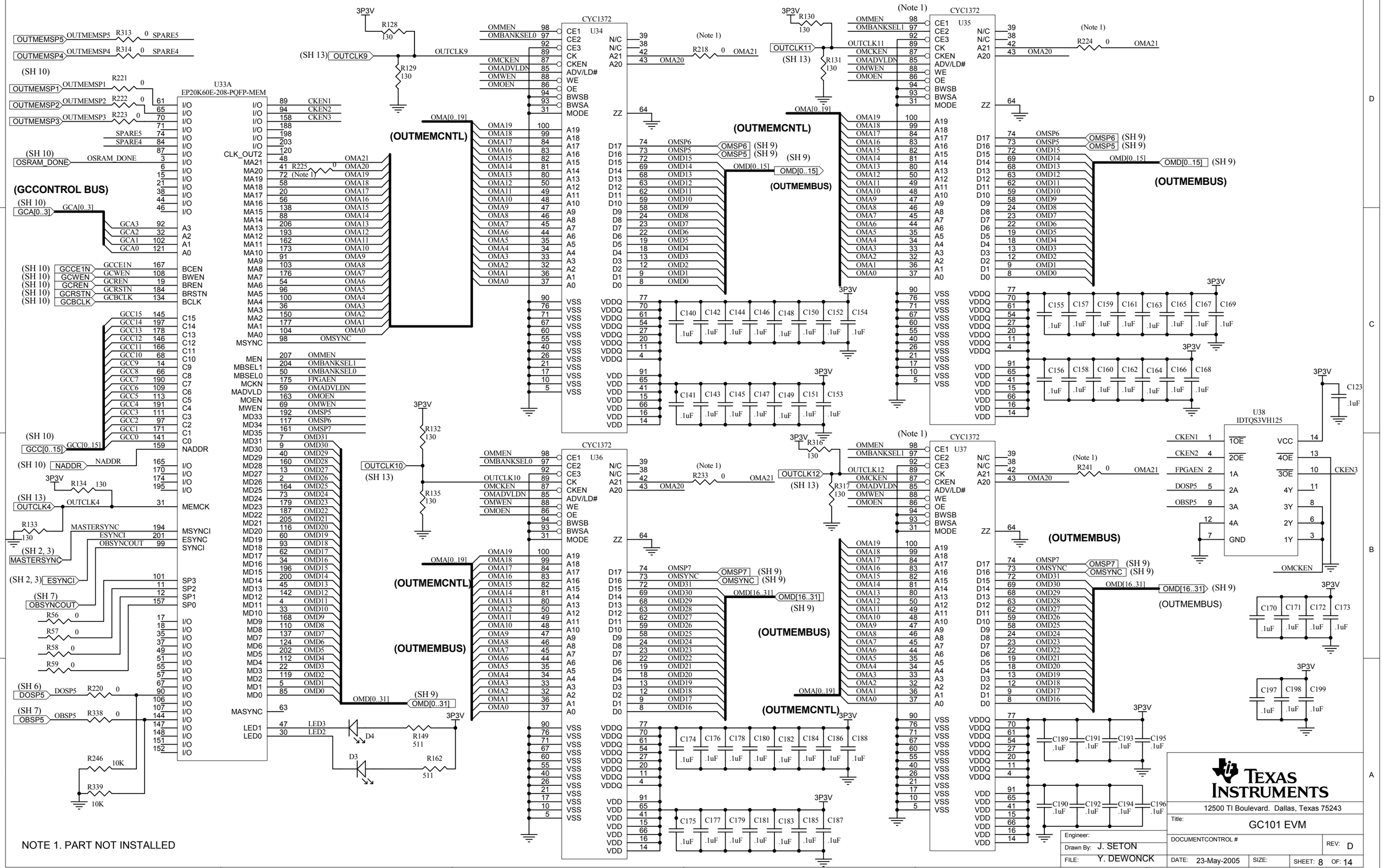


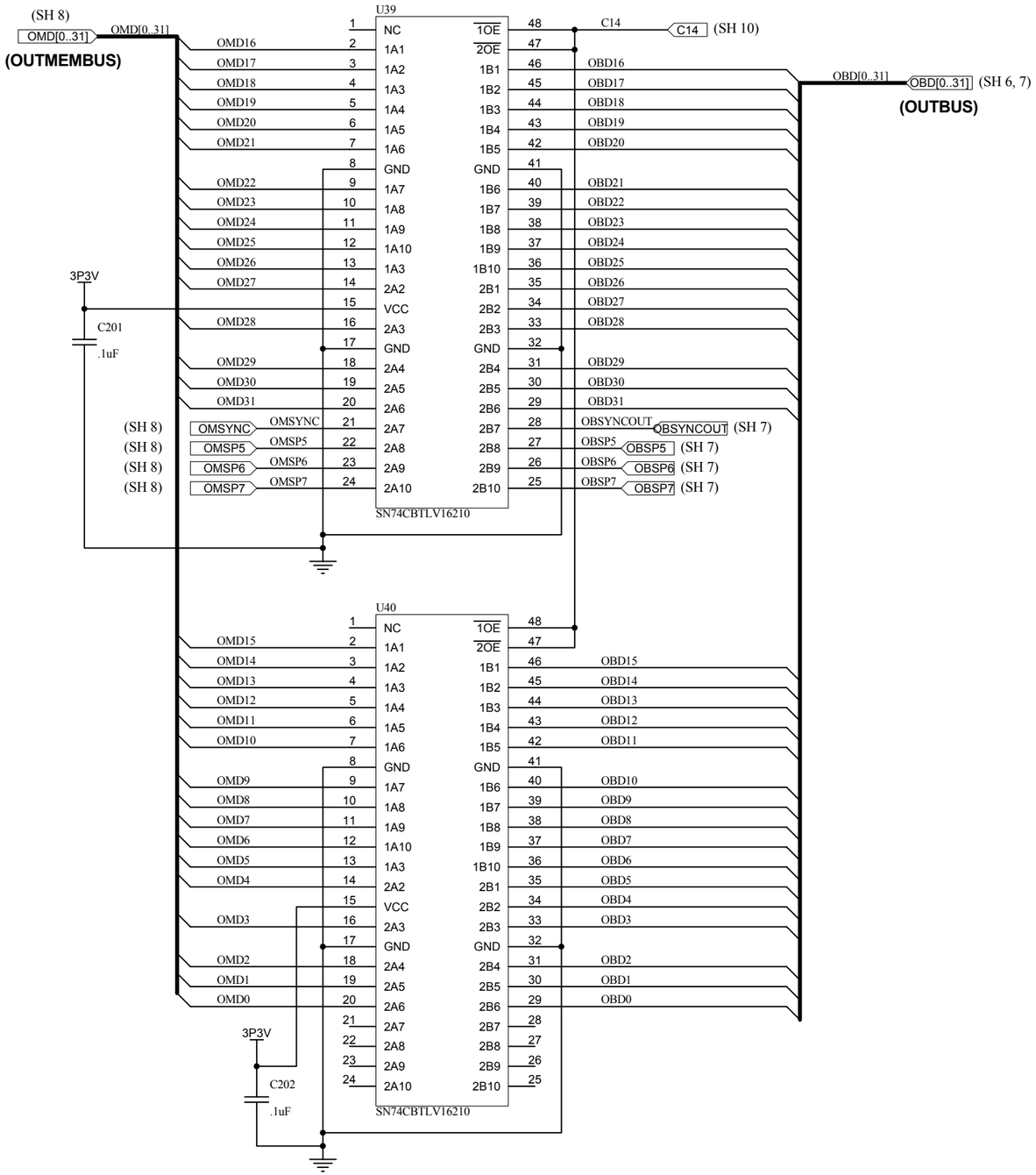


NOTE 1. PART NOT INSTALLED

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: GC101 EVM			
Engineer: J. SETON	DOCUMENTCONTROL #		REV: D
Drawn By: Y. DEWONCK			
FILE:	DATE: 23-May-2005	SIZE:	SHEET: 7 OF: 14


U33A
EP20K60E-208-PQFP-MEM
U34
U35
U36
U37
CYC1372
(OUTMEMCNTL)
(OUTMEMBUS)
(GCCONTROL BUS)
IDTQS3VH125
U38
3P3V
OUTCLK9
OUTCLK10
OUTCLK11
OUTCLK12
OUTCLK4
OSRAM_DONE
MASTERSYNC
ESYNCI
OBSYNCOUT
OMCKEN
OMADVLDN
OMWEN
OMOEN
OMMEN
OMBANKSEL0
OMBANKSEL1
MEMCK
MSYNCI
ESYNC
SYNCI
NADDR
GCC[0..15]
GCA[0..3]
OMA[0..19]
OMD[0..15]
OMD[16..31]
OMSP5
OMSP6
OMSP7
OMSYNC
OMA20
OMA21
OMSYNC
MASYNC
LED0
LED1
DOSP5
OBSP5
FPGAEN
CKEN1
CKEN2
CKEN3
(Note 1)
(SH 9)
(SH 10)
(SH 13)
(SH 2, 3)
(SH 6)
(SH 7)
NOTE 1. PART NOT INSTALLED
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: GC101 EVM
DOCUMENTCONTROL #
REV: D
Engineer:
Drawn By: J. SETON
FILE: Y. DEWONCK
DATE: 23-May-2005
SIZE:
SHEET: 8 OF: 14



Engineer:	J. SETON
Drawn By:	Y. DEWONCK
FILE:	

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: GC101 EVM			
DOCUMENTCONTROL #			REV: D
DATE: 23-May-2005	SIZE:	SHEET: 9	OF: 14

EPP PORT TO LOCAL BUS BRIDGE CONTROLLER

BRIDGE CONTROLLER OSCILLATOR

U9 — 40.0 MHz

PC_EPPBUS

U45A EP20K60E-208-PQFP-CNTL

U44 SN74LVC161284

J14 — DB25F-RA

VCABLE POWER SELECT

Cable side output buffer operating voltage

TRISTATE CONTROL MUXES

(GCCONTROL_BUS)

SPARE CONTROL IO

U58 SN74LVC2G14

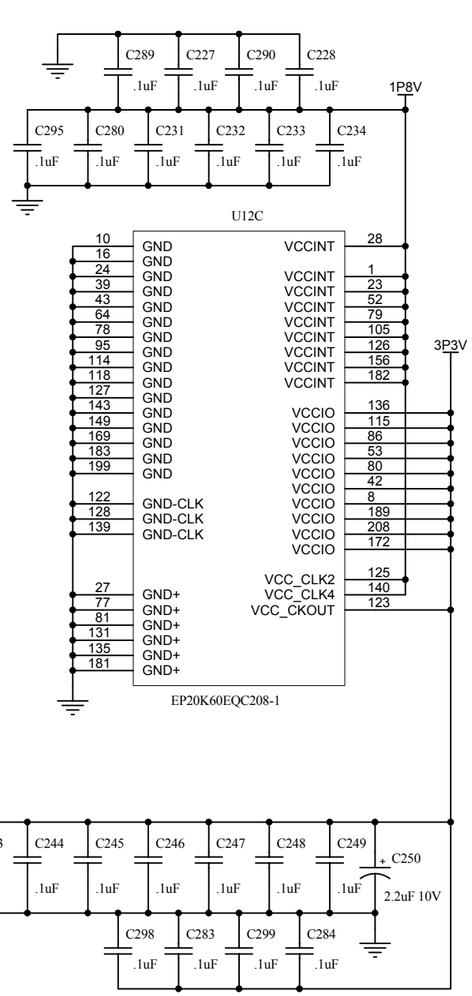
J15 IDH Header

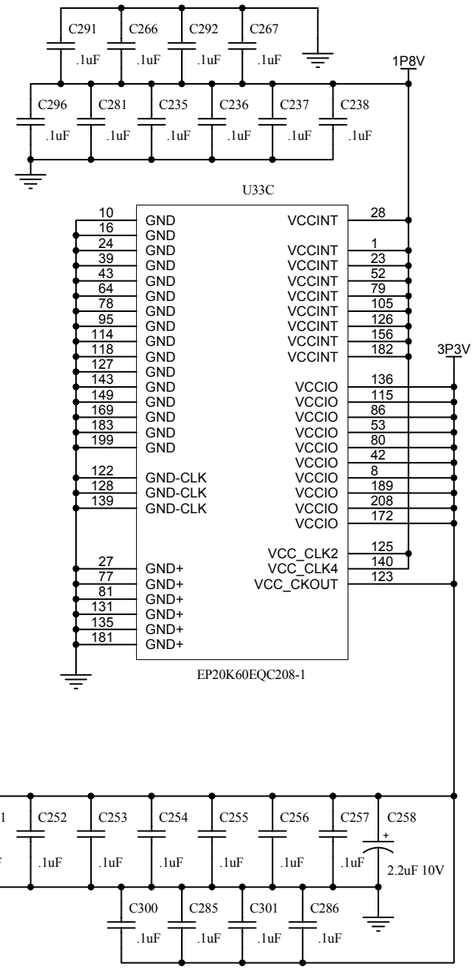
J10 26 PIN_IDH

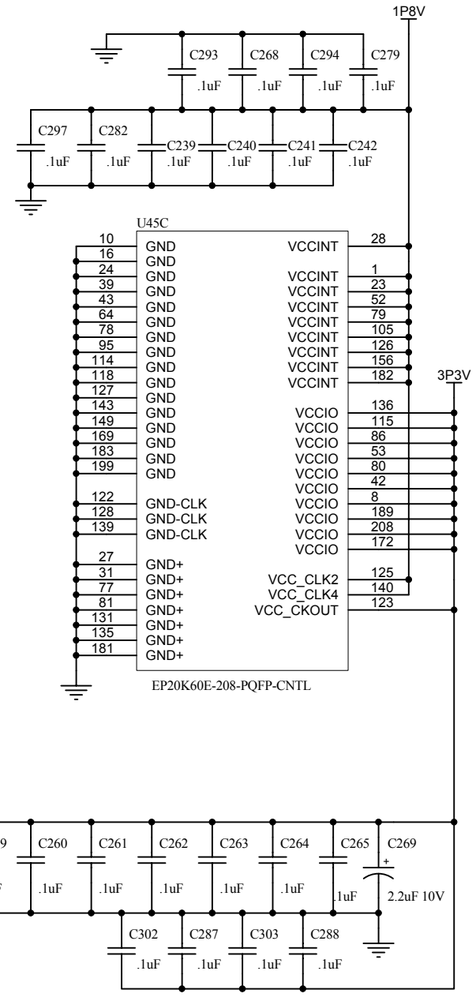
NOTE 1. PART NOT INSTALLED

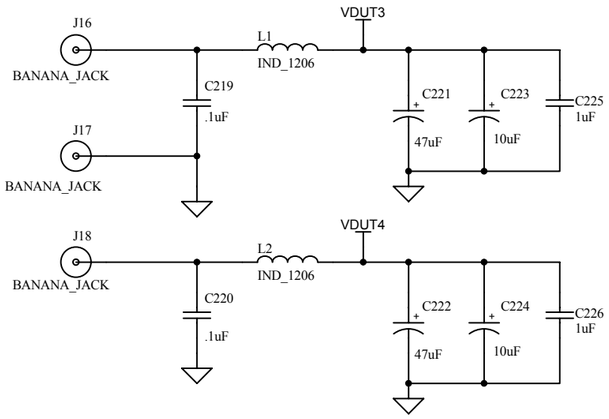
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

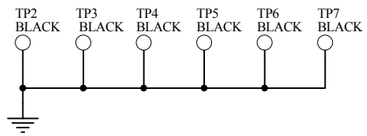
Title:	GC101 EVM
Engineer:	J. SETON
Drawn By:	Y. DEWONCK
FILE:	
DOCUMENTCONTROL #	
REV:	D
DATE:	23-May-2005
SIZE:	
SHEET:	10 OF: 14

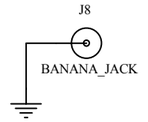










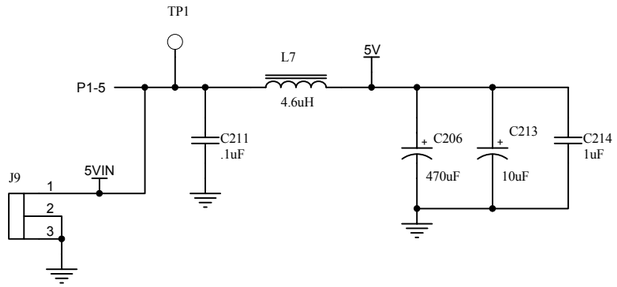


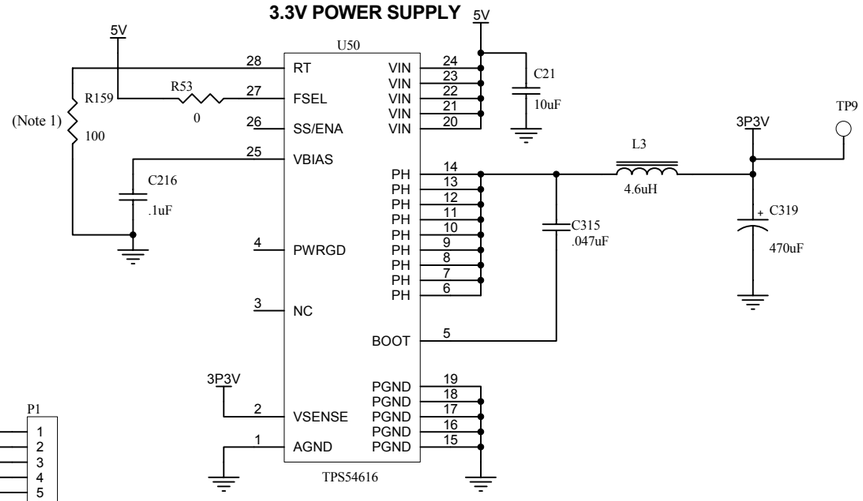
TEXAS INSTRUMENTS

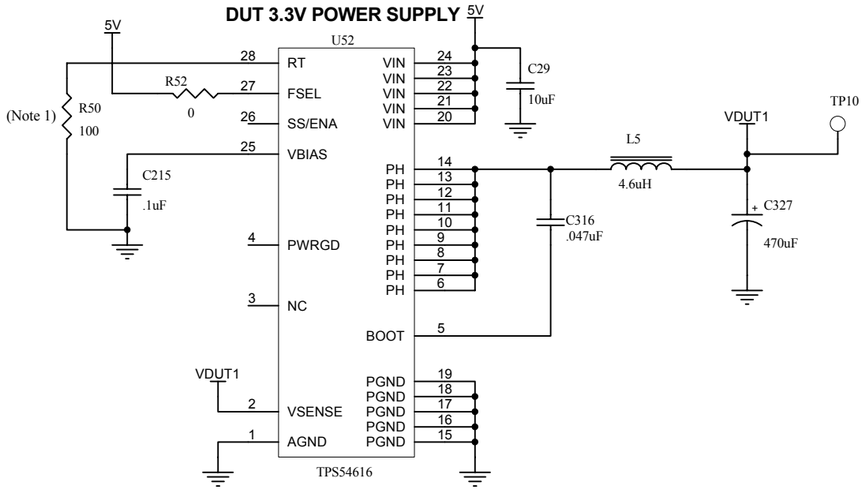
12500 TI Boulevard. Dallas, Texas 75243

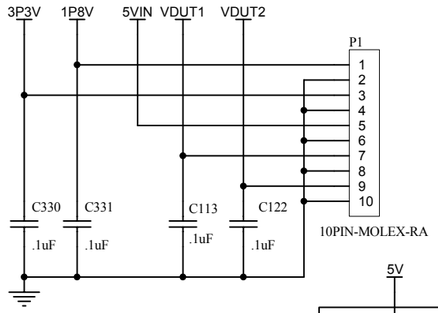
Title: GC101 EVM

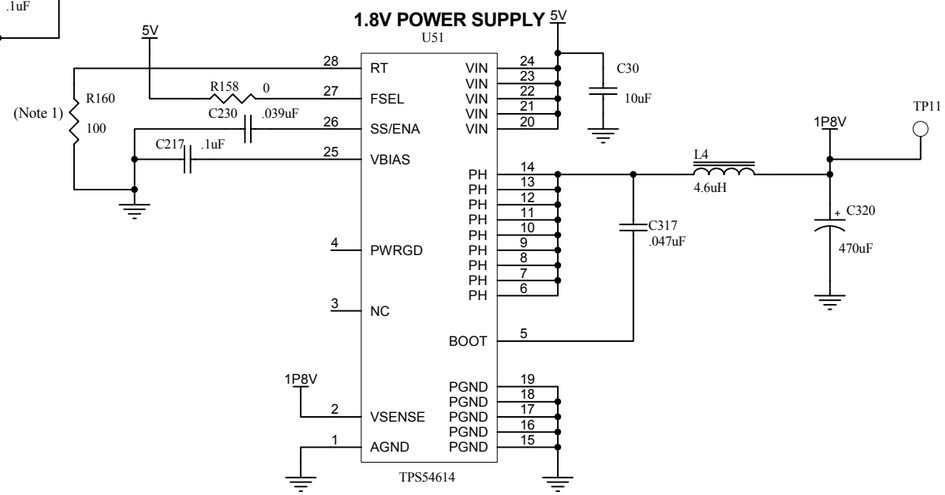
Engineer: J. SETON	DOCUMENTCONTROL #		REV: D
Drawn By: Y. DEWONCK	DATE: 23-May-2005	SIZE:	SHEET: 11 OF: 14
FILE:			

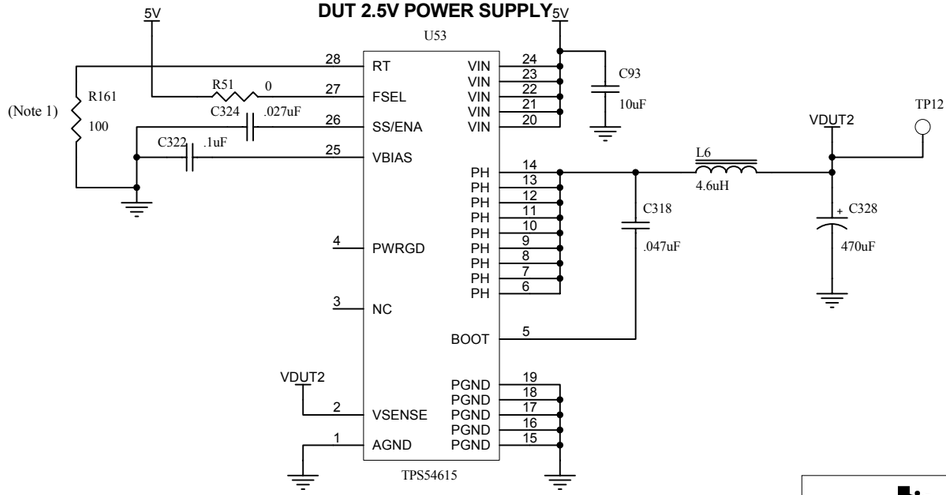












NOTE 1. PART NOT INSTALLED

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: GC101 EVM			
Engineer: J. SETON	DOCUMENTCONTROL #		REV: D
Drawn By: Y. DEWONCK	DATE: 23-May-2005	SIZE:	SHEET: 12 OF: 14
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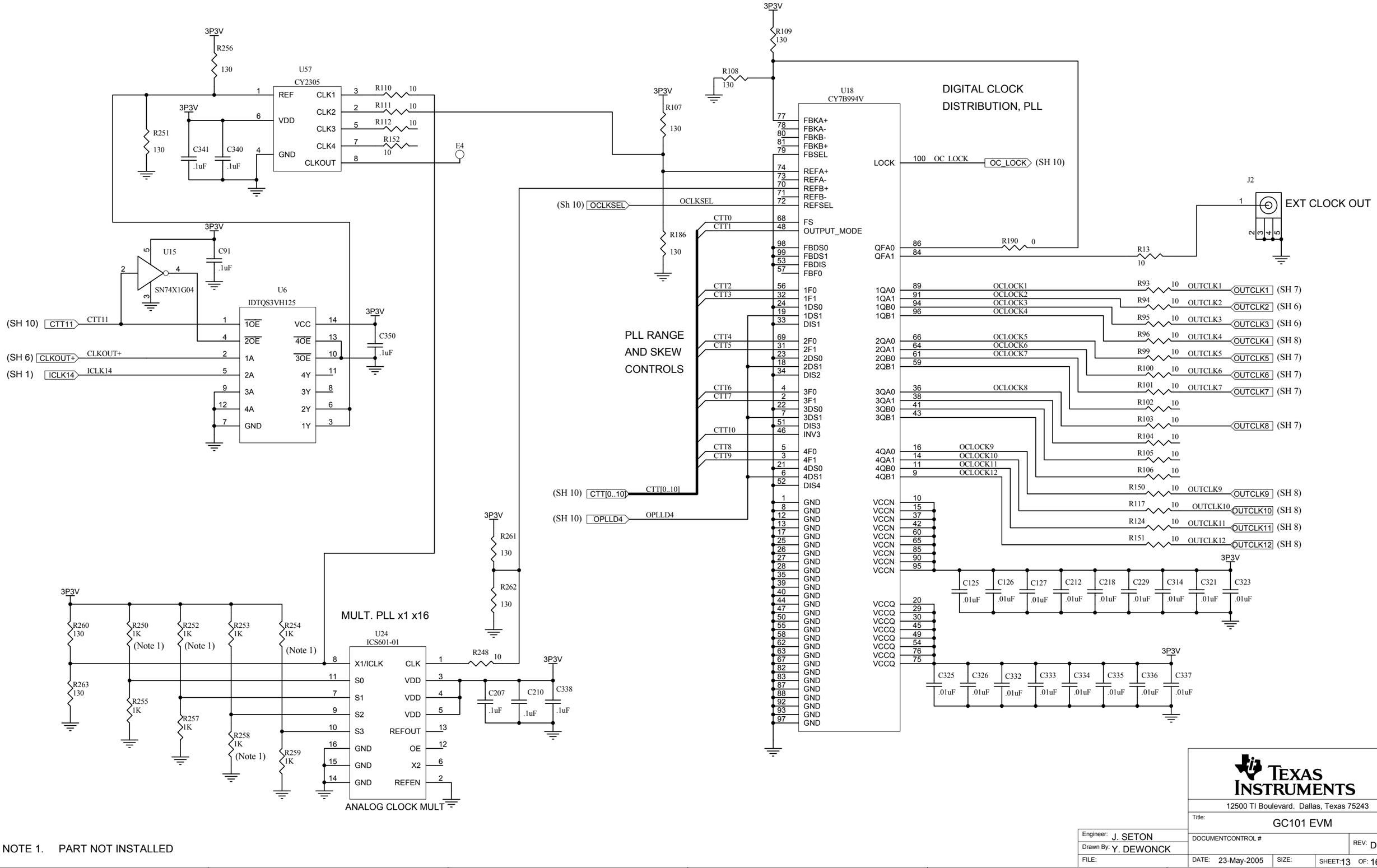
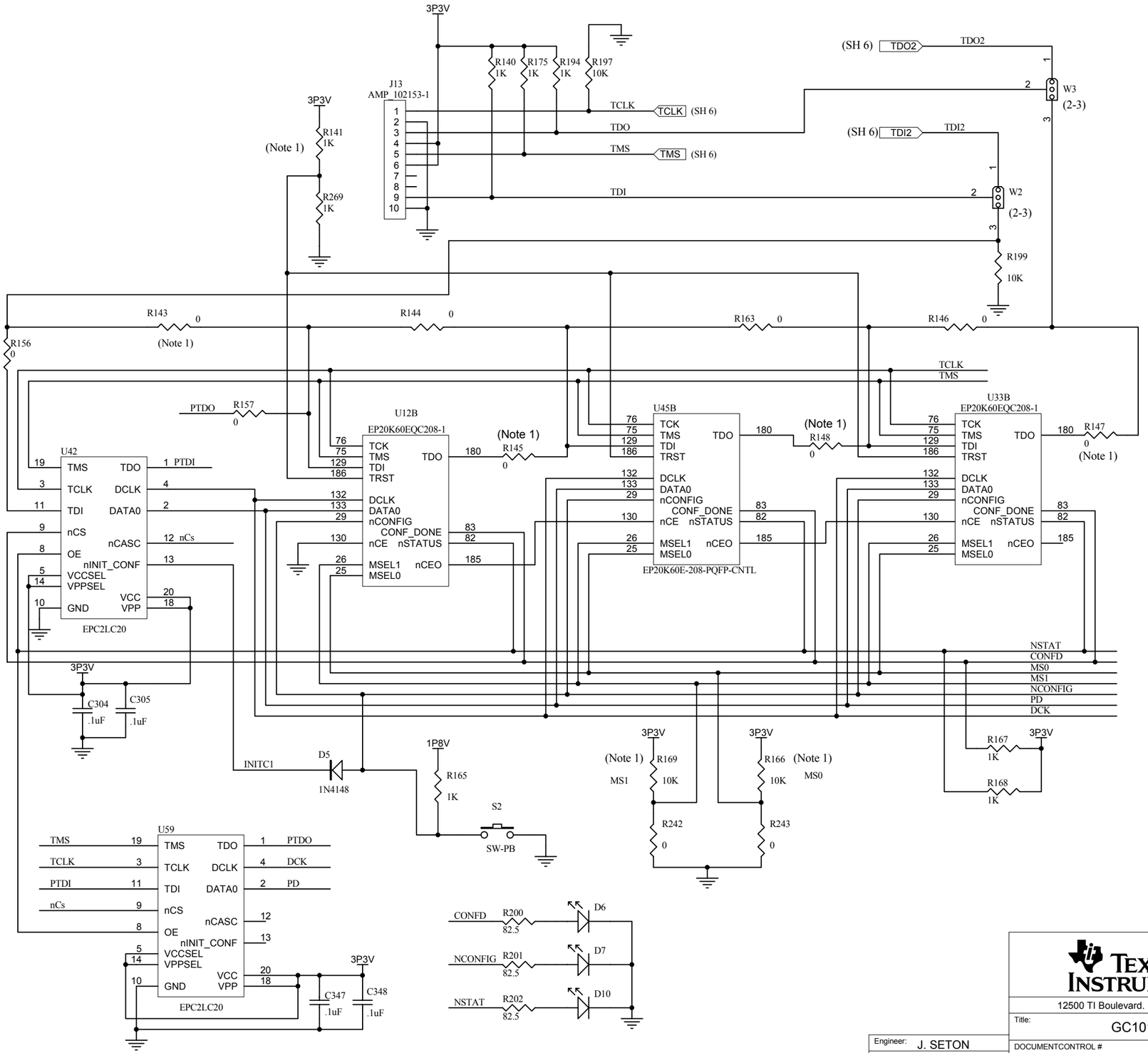

3P3V
R256
130
U57
CY2305
REF
VDD
GND
CLK1
CLK2
CLK3
CLK4
CLKOUT
R110 10
R111 10
R112 10
R152 10
R251
130
C341 .1uF
C340 .1uF
E4
U15
SN74X1G04
C91 .1uF
U6
IDTQS3VH125
1OE
2OE
3OE
4OE
1A
2A
3A
4A
1Y
2Y
3Y
4Y
VCC
GND
C350 .1uF
(SH 10) CTT11
(SH 6) CLKOUT+
(SH 1) ICLK14
R109
130
R108
130
R107
130
R186
130
U18
CY7B994V
DIGITAL CLOCK
DISTRIBUTION, PLL
PLL RANGE
AND SKEW
CONTROLS
(Sh 10) OCLKSEL
(SH 10) CTT[0..10]
(SH 10) OPLLD4
FBKA+
FBKA-
FBKB-
FBKB+
FBSEL
REFA+
REFA-
REFB+
REFB-
REFSEL
FS
OUTPUT_MODE
FBDS0
FBDS1
FBDIS
FBF0
1F0
1F1
1DS0
1DS1
DIS1
2F0
2F1
2DS0
2DS1
DIS2
3F0
3F1
3DS0
3DS1
DIS3
INV3
4F0
4F1
4DS0
4DS1
DIS4
GND
LOCK
OC_LOCK
(SH 10)
QFA0
QFA1
1QA0
1QA1
1QB0
1QB1
2QA0
2QA1
2QB0
2QB1
3QA0
3QA1
3QB0
3QB1
4QA0
4QA1
4QB0
4QB1
OCLOCK1
OCLOCK2
OCLOCK3
OCLOCK4
OCLOCK5
OCLOCK6
OCLOCK7
OCLOCK8
OCLOCK9
OCLOCK10
OCLOCK11
OCLOCK12
R190 0
R13 10
J2
EXT CLOCK OUT
R93 10 OUTCLK1 (SH 7)
R94 10 OUTCLK2 (SH 6)
R95 10 OUTCLK3 (SH 6)
R96 10 OUTCLK4 (SH 8)
R99 10 OUTCLK5 (SH 7)
R100 10 OUTCLK6 (SH 7)
R101 10 OUTCLK7 (SH 7)
R102 10
R103 10 OUTCLK8 (SH 7)
R104 10
R105 10
R106 10
R150 10 OUTCLK9 (SH 8)
R117 10 OUTCLK10 (SH 8)
R124 10 OUTCLK11 (SH 8)
R151 10 OUTCLK12 (SH 8)
VCCN
VCCQ
C125 C126 C127 C212 C218 C229 C314 C321 C323 .01uF
C325 C326 C332 C333 C334 C335 C336 C337 .01uF
R261
130
R262
130
MULT. PLL x1 x16
U24
ICS601-01
X1/ICLK
S0
S1
S2
S3
CLK
VDD
REFOUT
OE
X2
REFEN
R248 10
C207 C210 C338 .1uF
R260 130
R263 130
R250 1K (Note 1)
R255 1K
R252 1K (Note 1)
R257 1K
R253 1K
R258 1K (Note 1)
R254 1K (Note 1)
R259 1K
ANALOG CLOCK MULT
NOTE 1. PART NOT INSTALLED
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243
Title: GC101 EVM
Engineer: J. SETON
Drawn By: Y. DEWONCK
FILE:
DOCUMENTCONTROL #
REV: D
DATE: 23-May-2005
SIZE:
SHEET: 13 OF: 16



NOTE 1. PART NOT INSTALLED

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Engineer: J. SETON	Title: GC101 EVM		
Drawn By: Y. DEWONCK	DOCUMENTCONTROL #		REV: D
FILE:	DATE: 23-May-2005	SIZE:	SHEET: 14 OF: 14