Section 2

Useful Things to Know About Amplifiers, When Transmitting High-Speed Signals

Dynamic Range Considerations in High Performance Amplifier Channels

This section is a collection of previously published high performance amplifier design ideas and issues - updated and corrected where necessary.

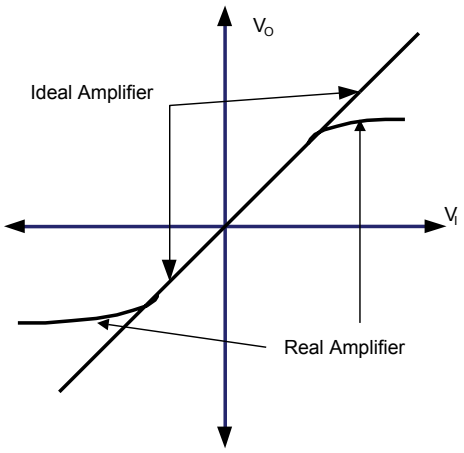
Topics Covered

- **Loop gain and distortion dependence**
- **New current feedback amplifiers**
- **New voltage feedback amplifier topologies**
- **Input & output noise calculations**
- **Component selection for low noise design in high-speed amplifiers**
- **Predicting closed loop frequency response from open loop characteristics**
- **Spice modeling**

This section covers the areas of high-speed amplifiers that are commonly mis-understood or not fully optimized for high-speed design.

Ideal vs Real Amplifier

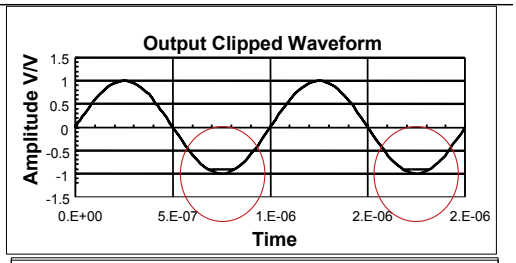
- Ideal amplifiers have no limitations or distortion; perfectly linear transfer function with no output limits.
- Real amplifiers have finite output voltage/current and a non-linear transfer function
- Distortion is measured by applying one or two spectrally pure input signals and measuring the power at the harmonics.

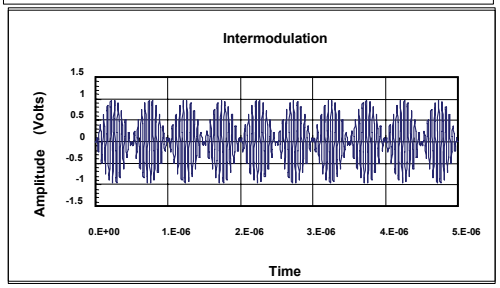


Distortion is a term used broadly when discussing amplifiers. Non-linear distortion occurs when a signal passes through a high-speed amplifier that has a non-linear V_I vs. V_O transfer characteristic. An example of non-linear behavior is shown in the figure where the straight line (an ideal op amp) deviates slightly from perfect linearity.

Types of Distortion

- Distortion will occur when the output signal is limited by non-linearity. Output clipping is normally not considered a valid signal condition - so rarely specified.
- Single tones only produce harmonic distortion, whereas multitones produce Intermodulation distortion.
- Some passive components have non-linear effects, such as hysteresis in transformers, or dielectric absorption in capacitors. These are normally not considered as part of amplifier distortion.





Measuring distortion is done by looking at the spectrum of a signal with a spectrum analyzer and observing the second, third, fourth, etc, of the fundamental harmonics with respect to the amplitude of the fundamental. The results can be specified as a %, ppm, dBm, or dBc. TI generally provides the distortion plots in % or dBc. There are typically a range of test conditions shown that will allow the customer to predict his/her performance.

A 2-tone intermodulation test waveform is shown in the lower figure above. Third order non-linearities in the amplifier transfer function will generate distortion power at frequencies that can be very close to the original input frequencies. This is a particularly difficult issue since those cannot typically be filtered out.

Harmonic Distortion Analysis using a Polynomial Approximation to the Amplifier Transfer Function

$$V_o = k_o + K_1 V_I + k_2 V_I^2 + k_3 V_I^3 ..... + k_n V_I^n$$

Substituting an input sine wave for Vi.

$$V_o = k_o + k_1 V_p \sin\omega t + k_2 V_p^2 \sin^2 \omega t + k_3 V_p^3 \sin^3 \omega t$$

Using the following trigonometric identities $\sin^2 \omega t = \frac{1-\cos 2\omega t}{2}$ and $\sin^3 \omega t = \frac{3\sin\omega t - \sin 3\omega t}{4}$

Vo can be written as ⇨

$$V_o = k_0 + k_1 V_p \sin\omega t + k_2 V_p^2 \frac{1-\cos 2\omega t}{2} + k_3 V_p^3 \frac{3\sin\omega t - \sin 3\omega t}{4}$$

$$V_o = \left(k_o + \frac{k_2 V_p^2}{2}\right) + \left(k_1 V_p + \frac{3k_3 V_p^3}{4}\right)\sin\omega t - \frac{k_2 V_p^2}{2}\cos 2\omega t - \frac{k_3 V_p^3}{4}\sin 3\omega t$$

Important Result ⇨ **V_o (spectrally) ≅ dc term + input frequency + 2nd harmonic + 3rd harmonic**

Distortion is produced due to the non-linearity's of the transfer function. In general, the transfer characteristics can be expressed in the form of a polynomial equation:

For applications where the transfer function has sharp non-linearities, such as in signal clipping circuits, the polynomial will have a large number of terms but in many practical cases the gain changes gradually and only a few terms are needed to represent the results.

For ideal amplifiers k_o, k_2, k_3, etc are ideally zero but in reality they will have small but finite values. The value of the coefficients rapidly drops as the order of the term increases and for small changes it is generally not included if those terms are above 3rd order.

Harmonic distortion is the generation of harmonics by the amplifier when it is excited by a single sinusoid. It's model will include terms up to the 3rd order with $V_I = V_p \sin\omega t$.

The spectral output can be simplified to the input frequency plus a dc voltage, plus the 2nd harmonic, plus the 3rd harmonic.

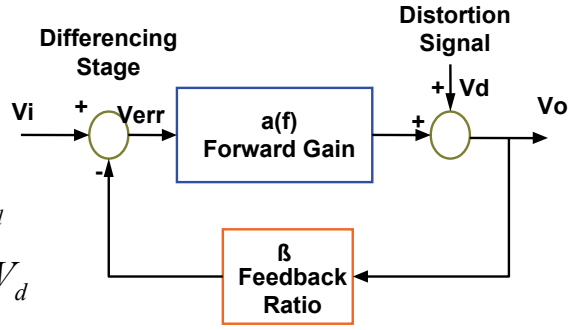
Distortion Analysis using Negative Feedback with Distortion modeled only as an Output Stage Distortion

$$V_o = a(f) \cdot V_{err} + V_d$$

$$V_{err} = V_i - \beta \cdot V_o$$

$$V_o = a(f) \cdot V_i - a(f) \cdot \beta \cdot V_o + V_d$$

$$(1 + a(f) \cdot \beta) V_o = a(f) \cdot V_i + V_d$$



Assuming a(f) · β >>1 $\Longrightarrow$ $V_o \cong \frac{V_i}{(\beta)} + \frac{V_d}{(a(f) \cdot \beta)}$

where a(f) · ß = Loop Gain. **Output stage non-linearities are corrected by loop gain**.

This slide shows that the effect of loop gain is to reduce the distortion due to the amplifier non-linearity introduced at the output stage. It has no effect on noise or distortion at the amplifier input.

As will be shown in the Layout Section, placement of the decoupling capacitors next to the device is critical in having the shortest path to the load. This is particularly important for even order harmonic suppression to maintain a balanced ground return current from the load through the de-coupling capacitors.

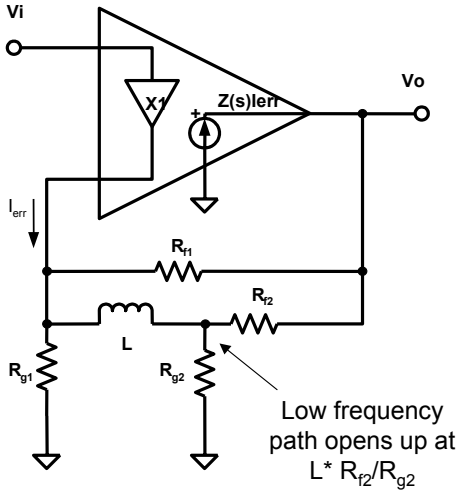
Distortion Reduction using Negative Feedback

- **All op amps act to correct the intrinsic non-linearity of the output stage using Loop Gain.**
  - **For Voltage feedback, the Loop Gain is the open loop voltage gain divided by the noise gain (at the test frequency)**
  - **For Current feedback, the Loop Gain is the open loop transimpedance gain divided by the feedback impedance (at the test frequency)**
- **It is possible to use external L's & C's to increase the op amp loop gain at low frequencies to improve distortion at low frequencies while retaining good closed loop stability.**
  - **For more information on this subject, see application note http://focus.ti.com/lit/an/slyt027/slyt027.pdf**

Loop Gain Shaping to Improve Low Frequency Distortion for Current Feedback

$$\frac{V_o}{V^+} = \left(1+\frac{R_{f1}}{R_{g1}}\right)\frac{\dfrac{s+\left(R_{f2}\|R_{g2}\right)+\left(R_{f1}\|R_{g1}\right)}{L}}{s+\dfrac{R_{f1}+R_{f2}}{L\left(1+R_{f2}/R_{g2}\right)}}$$

$$1+\frac{R_{f1}}{Z(s)}\left[\frac{s+\dfrac{R_{f2}}{L\left(1+R_{f2}/R_{g2}\right)}}{s+\dfrac{R_{f2}+R_{f1}}{L\left(1+R_{f2}/R_{g2}\right)}}\right]$$

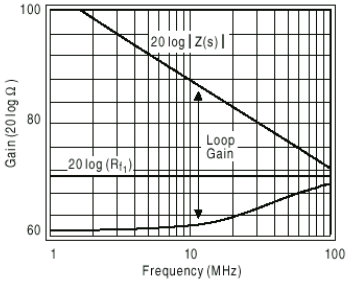


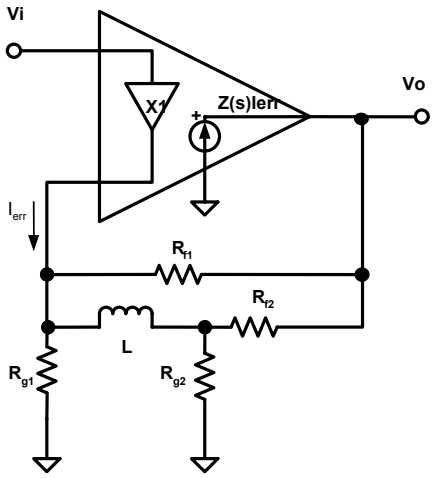
Since the loop gain can reduce the distortion in amplifiers, loop shaping can be used to improve the distortion at low frequencies. Taking the feedback loop and altering the response through the use of inductors and resistors is a way to improve the loop response at lower frequencies. The technique shown above can can give >55dBm intercepts at lower frequencies but does give a poor frequency response flatness.

A typical circuit to increase the low closed-loop gain settings uses a parallel second feedback path to shape the low frequency noise gain. The coupling inductor is set to remove this parallel feedback path before the unity loop gain crossover frequency (where the Z(s) = R_{f1}) with approximately 60 degrees phase margin. At low frequencies the gain is set by the parallel combination of the two Rg resistors. At high frequencies, the inductor has isolated this second feedback loop to give a gain of 1+Rf1/Rg1. The feedback impedance at low frequencies is the parallel combination of the two feedback Rf resistors, while at high frequencies it increases to equal just $R_{f1.}$ As the frequency goes from low to high the zero/pole pair for the signal path and feedback impedance shapes the response.

Increased Loop Gain at Low Frequencies will Improve SFDR in CFB Amps

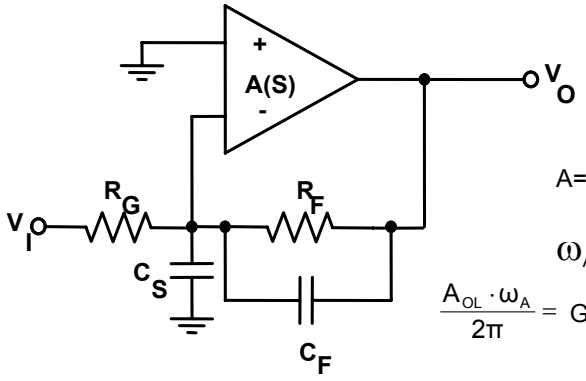
Typical Loop Gain (shaping) Enhancement Shown Below.
20*Log|Z(s)| is the frequency dependent Open loop transimpedance gain while the lower curve is the frequency dependent feedback impedance.





The graph shows increased loop gain at low frequency, while maintaining high frequency stability.

Compensation Technique for Non-Unity Gain Stable Voltage Feedback Op Amps



$$A(s) = \frac{A_{OL} \cdot \omega_A}{s + \omega_A}$$

A= Open Loop Gain

ω_A= Radian Dominant Pole

$\frac{A_{OL} \cdot \omega_A}{2\pi}$ = Gain Bandwidth Product (GBW) Hz

$$NG = 1 + \frac{R_f}{R_g}$$

Developed in "Unique Compensation Technique Tames High-Bandwidth Voltage-Feedback Op Amps", EDN, August 1st, 1997, pp133-150

One of the best ways to design for a low noise application is to use a high-gain part like an OPA847 and loop-shape the part's closed-loop response for better distortion and lower noise at the lower frequencies. This is done by compensation through the use of capacitors to shape the response to maintain stability.

Here the open-loop response Aol is altered by ω_A pole and zero, therefore altering the gain bandwidth product.

Unity gain stable op amps are generally plagued with higher noise and/or lower slew rate as compared to their de-compensated counterparts.

Op amps require compensation for stability. Unity gain requires the most compensation. Two basic techniques used to internally compensate an amplifier are emitter degeneration and dominant pole capacitance.

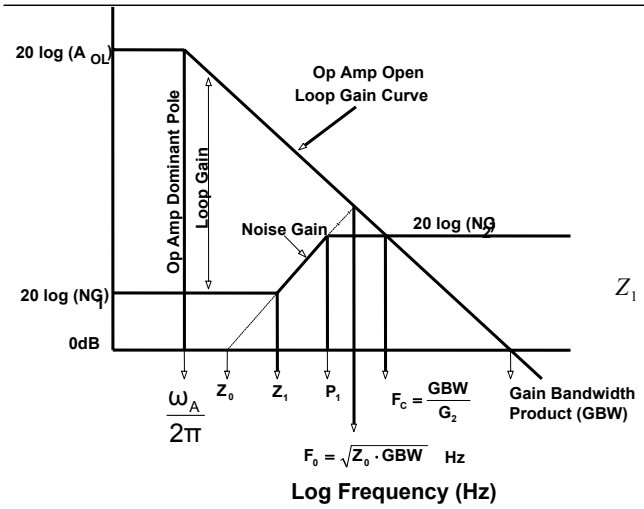
Emitter degeneration adds Johnson noise.

Dominant pole capacitance reduces the slew rate.

Using less compensation or de-compensating the op amp allows for lower noise and higher slew rate. Without external compensation, higher gain operation is required for stability.

The following outlines a simple technique for external compensation for such amplifiers.

Bode Analysis Compensation for Low Gain Circuit with High-Gain Amp



$$NG_1 = 1 + \frac{R_F}{R_G}$$

$$NG_2 = 1 + \frac{C_S}{C_F}$$

$$Z_0 = \frac{1}{R_F(C_F + C_S)2\pi}$$

$$Z_1 = \frac{1}{(R_F \parallel R_G)(C_F + C_S)2\pi} = NG_1 \cdot Z_0$$

$$P_1 = \frac{1}{R_F \cdot C_F \cdot 2\pi} = NG_2 \cdot Z_0$$

Putting the equation in the standard form for a second order system allows one to simplify the results in terms of ω_A and Q. Selecting the correct cutoff frequency by solving for the values at a particular Q helps one pick initial results. Once this is done simulating the results shows how the expected results

$$\frac{V_O}{V_I} = \frac{-\frac{A_{OL} \cdot \omega_A}{(C_F + C_S)R_G}}{s^2 + s\left[\frac{\omega_A}{C_F + C_S}\left(C_F(A_{OL} + 1) + C_S\right) + \frac{1}{(R_F \parallel R_G)(C_F + C_S)}\right] + \frac{\omega_A}{C_F + C_S}\left(\frac{A_{OL} + 1}{R_F} + \frac{1}{R_G}\right)}$$

With some simplifications:

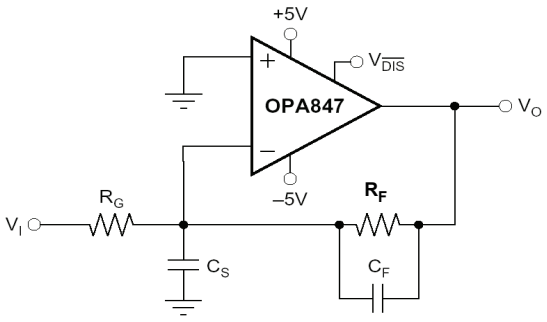
$$\frac{V_O}{V_I} \approx \frac{-\frac{R_F}{R_G}\omega_O{}^2}{S^2 + S\frac{\omega_O}{Q} + \omega_O{}^2}$$

where $-\frac{R_F}{R_G} =$ DC Signal Gain

$$\omega_O \approx \sqrt{\frac{A_{OL} \cdot \omega_A}{R_F(C_F + C_S)}}$$

$$Q \approx \frac{\omega_O}{\frac{A_{OL} \cdot \omega_A}{1 + \frac{C_S}{C_F}} + \frac{1 + R_F/R_G}{R_F(C_S + C_F)}}$$

Final Results with External Compensation



$$NG_1 = 1 + R_F/R_G$$

$$\mathbf{NG_2 = 12}$$

$$f_{-3dB} \cong \sqrt{Z_O \bullet GBP}$$

$$C_F = \frac{1}{2\pi R_F Z_O NG_2}$$

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1 - \frac{NG_1}{NG_2}\right) - \sqrt{1 - 2\frac{NG_1}{NG_2}}\right]$$

$$C_S = (NG_2 - 1)C_F$$

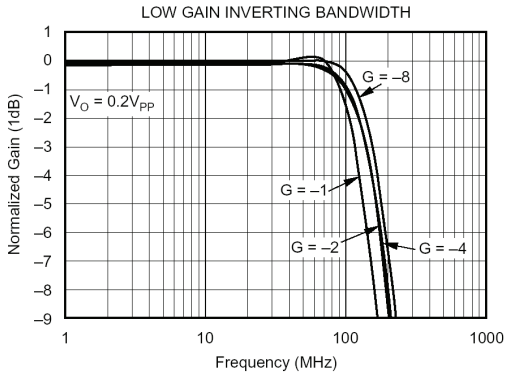
Considering only the noise gain (which is the same as the non-inverting signal gain) for the circuit shown, the low frequency noise gain (NG_1) is set by the resistor ratio, while the high-frequency noise gain (NG_2) is set by the capacitor ratio. The capacitor values set both the transition frequencies and the high-frequency noise gain. If the high-frequency noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp, and the noise gain pole (set by $1/R_FC_F$) is placed correctly, a very well controlled 2nd-order low-pass frequency response results.

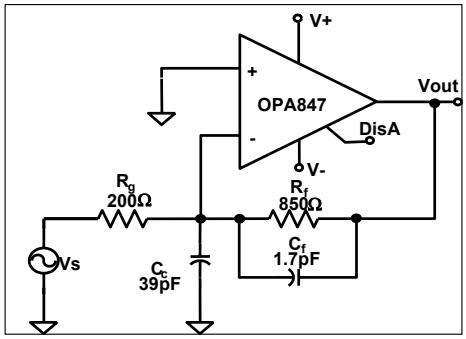
To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain (NG_2), which should be greater than the minimum stable gain for the part selected (the OPA847 is used here).

The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain (NG_1). Using only these two gains and the GBP for the OPA847 (3900MHz), solve for Z_O, C_S and C_F to set the component values.

Example Simulation Using OPA847

- **Design equations in the OPA847 data sheet**
- **Low Frequency gain set to -850/200 = -4.25 (12.6dB). This is far below minimum stable gain of 12.**
- **High frequency noise gain is 1 + 39pF/1.7pF = 24 gives stable response.**

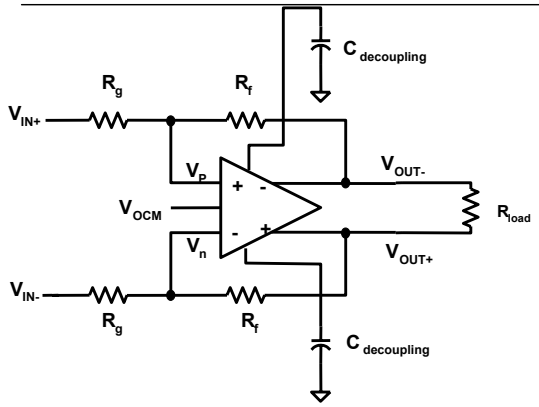




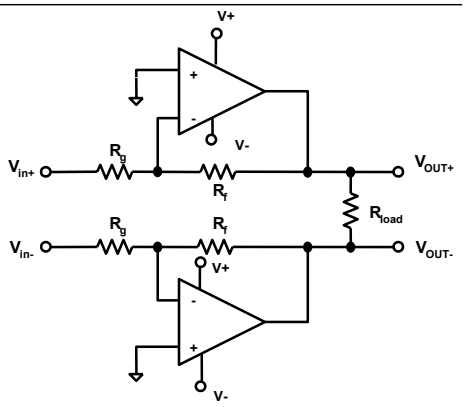
Apply the theory to an OPA847, allows us to design a low gain of –4.25 with a flat response in excess of 100MHz.

This technique will work from an inverting gain of -1 to almost any gain below the nominal gain, allowing the designer to benefit from the low noise and low distortion features of the decompensated amplifier in almost any application.

Configurations for Differential Circuits



Single Chip Differential THS series - This is essentially an inverting input differential I/O configuration with internal common mode feedback



Two Op Amps can also provide a Differential I/O with the common mode provided as an input bias. Used for AC coupled input conditions.

If an application needs low distortion and is AC coupled, then the differential configuration of two single ended amplifiers can provide a high performance solution.

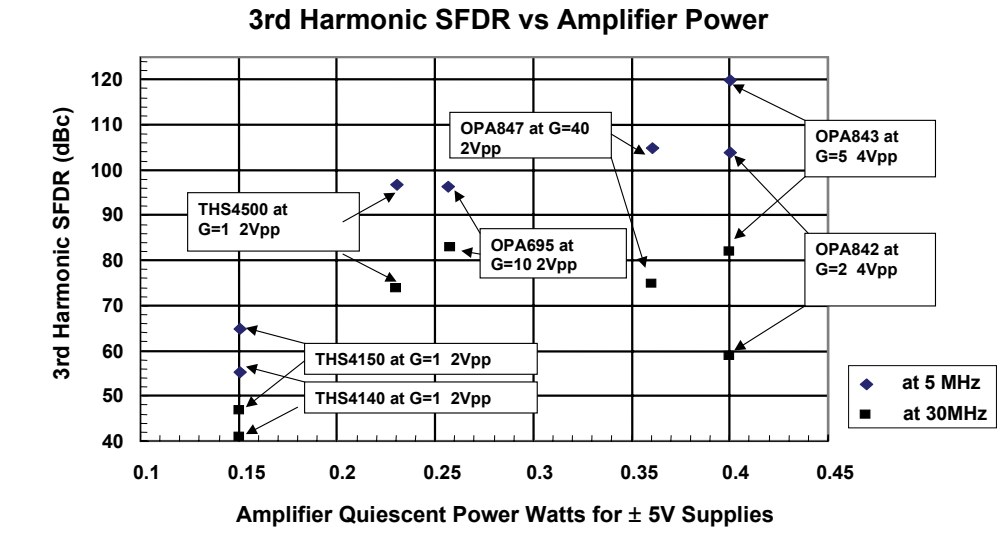
If the application is DC coupled and needs low distortion, then the fully differential amplifier provides an alternative high performance solution with the ability to adjust the common mode voltage, and the ability to convert single ended to fully differential signals.

Some parts are either dedicated differential I/O parts or have differential output distortion plots where two op amps have been configured in a differential I/O circuit with either non-inverting or inverting input mode selected.

Here, the 2nd harmonics are much lower and only 3rd SFDR again is considered. The parts plotted at their specified nominal differential gain setting with the differential load > 400ohms.

Again, as gain goes up or load goes down, these SFDR numbers will generally get worse.

Differential 3rd Harmonic SFDR



Since the 2nd Harmonic is pretty much eliminated in a differential amplifier, plotting the 3rd Harmonic SFDR vs Amplifier Power for Differential Configurations is useful to better understand the performance trade-offs of using these circuits.

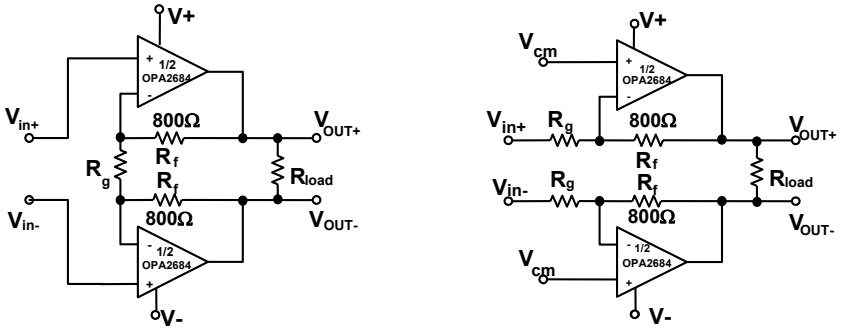
The plot shows the amplifiers at their preferred gain settings at two different frequencies. At 5MHz and higher gains one can reach higher SFDR with OPA84X series. At lower gains and lower voltage swings the differential THS4500 provides good results for lower amplifier power. This degrades as the output voltage swing is increased or the gain is increased.

Using loop gain shaping techniques can improve the distortion at lower gains and frequencies. More will be discussed in the ADC interface section.

Distortion Reduction using Differential Circuits.

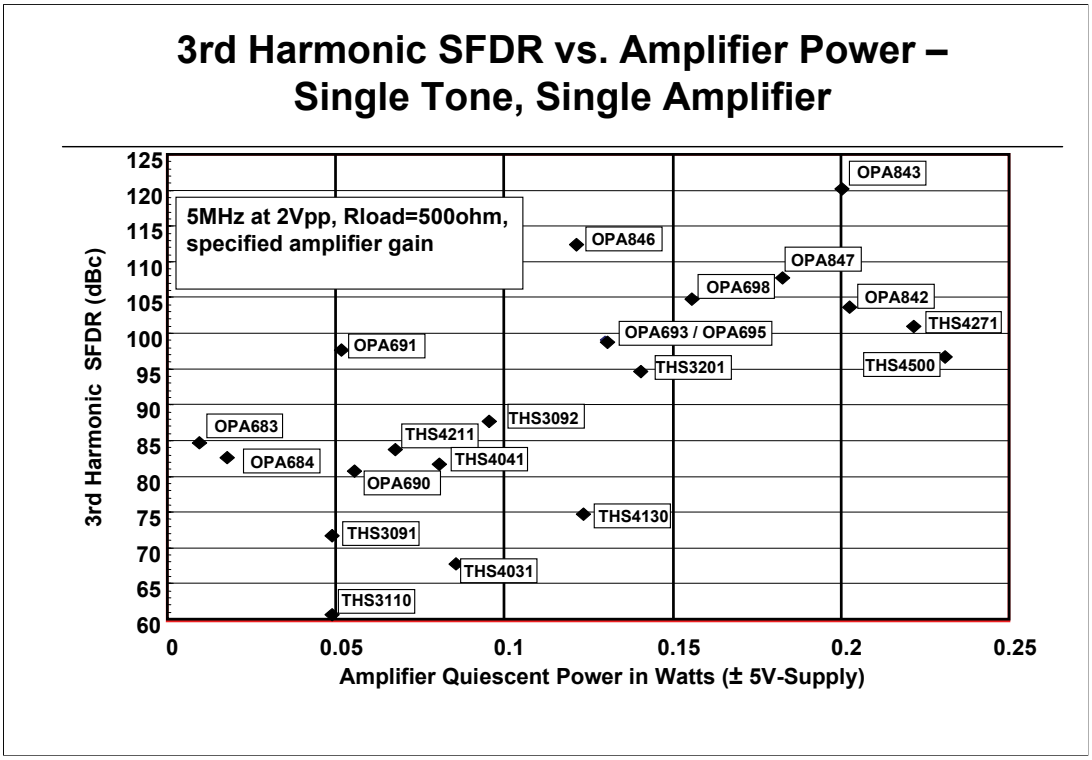
- **While most single op amps specify both 2nd and 3rd harmonic distortions, the even order terms (2nd, 4th, 6th) can be greatly reduced by using differential I/O architectures. This removes the 2nd order terms (even if the data sheet shows mediocre performance) leaving the 3rd's as the remaining limit to SFDR.**

Can do either non-inverting or inverting input structures.



Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog to Digital Converter (ADC) input interface or line driver applications. Two basic approaches are non-inverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless – the noninverting and inverting terminology applies to where the input is brought into the circuit.

The inverting configuration provides a lower noise than the non-inverting configuration. The common mode voltage is set by applying a reference to the Vcom for the inverting input configuration. Generally used where the signal is differential and common mode voltage is set for an ADC converter input interface.



Selecting high-speed amplifiers for low distortion, and ignoring the 2nd since it will be suppressed by the differential I/O design, we can pick a low distortion amplifier based upon its power for ± 5 volts.

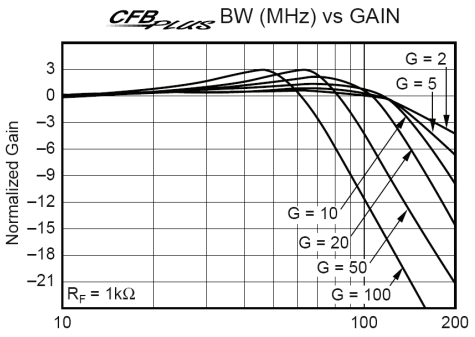
This graph plots SFDR vs the amplifiers quiescent power for ±5V supplies. For extremely low power applications the OPA683, OPA684, and OPA691, which are current feedback amplifiers, provide the best SFDR for the 50mW range.

As power becomes less of an issue then in the 150 to 200mW range the OPA846, OPA847, OPA698, and OPA843 provide some of the lowest SFDR parts for a large range of applications and gain bandwidths.

New Current/Voltage Feedback Amplifiers

New CFB$_{plus}$ Design (OPA683/OPA684)

- **Using a closed loop input buffer stage allows the total quiescent power for the amplifier to be reduced significantly while holding a nearly constant bandwidth over a wide gain range.**
- **The OPA684 (1.8mA/ch) and OPA683 (0.95mA/ch) are the first two amplifier products to use this. The plot shows the SSBW vs. gain setting for the OPA684 using a fixed Rf = 1kΩ.**



The output of the OPA684 sets a new standard in current feedback performance for low-power and incredible equivalent gain bandwidth. Delivering a full ±4V p-p swing on ±5V supplies, with an output current to support driving low impedance loads of 100Ω, demanding line driver applications can be supported. A minimal output headroom requirement is complemented by a similar 1.2V input stage headroom giving exceptional capability for single +5V operation.

With a low 1.8mA supply current that is precisely trimmed at 25°C it provides low drift over temperature and supply ranges. For gain ranging from 1 to 20, these devices maintain a constant bandwidth, allowing multi-stage designs where the bandwidth is important.

1st Order CFB Circuit Model, Showing CFB*plus* Closed Loop Input buffer

$$I_{error} = I_g - I_f$$

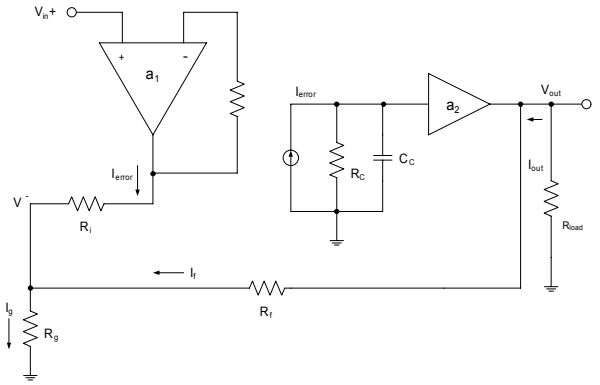
$$I_{error} = \frac{V^-}{R_g} - \frac{V_{out} - V^-}{R_f}$$

$$V_{out} = I_{error}\left(\alpha_2 \cdot Z(s)\right) - I_f$$

$$V^- = \alpha_1 \cdot V_{in} - I_{error} \cdot R_i$$

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1\left(1+\frac{R_f}{R_g}\right)}{1+\frac{R_f + R_i\left(1+\frac{R_f}{R_g}\right)}{\alpha_2 \cdot Z(s)}} = \frac{\alpha_1 NG}{1+\frac{R_f + R_i NG}{\alpha_2 \cdot Z(s)}}$$

$$NG = \left(1+\frac{R_f}{R_g}\right) \qquad Z(s) = \frac{R_c}{sR_cC_c + 1}$$



Current Feedback amplifiers offer very stable performance over a wide gain range with high slew rate vs. quiescent power.

In doing this, it gives up DC precision and will have higher output noise at low gain settings than comparable voltage feedback devices.

In theory, the bandwidth and stability are controlled with the feedback resistor value

To a first order, bandwidth should not change with gain setting.

The following slide repeats the transfer function analysis for current feedback.

The ideal transfer function is simply the numerator: = α_1*(1+Rf/Rg).

The denominator shows the non-ideal, frequency response determining elements. The loop gain is the critical term and is given by –

$$LoopGain = \frac{Z(s)}{R_f + R_i \cdot \left(1+\frac{R_f}{R_g}\right)} = \frac{\text{internal forward transimpedance}}{\text{feedback transimpedance}}$$

Z(s) rolls off with frequency similar to the open loop voltage gain of a voltage feedback op amp. Where it has rolled off in magnitude to equal the denominator, loop gain x-over occurs and the closed loop response will start to roll off.

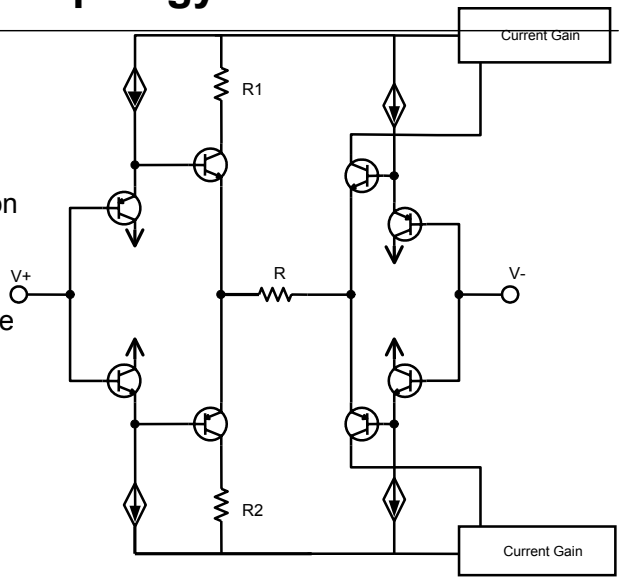
The nominal target sum of Rf + Ri*(1+Rf/Rg) can be held constant over gain setting by adjusting Rf. This first order correction works well for low Ri. However, at low total amplifier powers, Ri can get very large.

High-Slew Rate Voltage Feedback Input Stage Topology

• This is a high transconductance input stage - simply converts the external delta V across the inputs to a current in R - then passes it on to what is essentially a current feedback gain and output stage.

•OPA690 family is a good example

- •300Mhz GBW Product
- •Unity Gain Stable
- •Slew Rate 1800V/usec
- •Supply Current = 5.5mA
- •En = 5.5nV/√Hz



Classic tradeoff for unity gain stable voltage feedback op amp are input noise and slew rate.

Lower input stage degeneration gives lower noise but needs higher compensation cap which, for standard input stage topologies, reduces slew rate.

Higher input stage degeneration allows lower comp. Cap with some increase in slew rate (usually only with high quiescent current) but will increase the noise voltage

New input stage topology greatly extends slew rate with low quiescent power but again does increase the input noise voltage.

Input and Output Noise Calculations

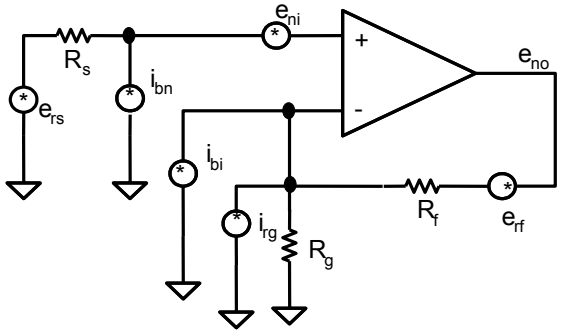
Noise Analysis for any Op Amp

$$e_{no}^2 = \left[(e_{rs}NG)^2 + (i_{bn}R_sNG)^2 + \left((e_{ni}NG\right)^2 + (i_{bi}R_f)^2 + (i_{rg}R_f)^2 + e_{rf}^2\right]$$

$$e_{no}^2 = \left[e_{ni}^2 + (i_{bn}R_s)^2 + 4kTR_s\right]\cdot NG^2 + \left[(i_{bi}R_f)^2 + (4kTR_f)\cdot NG\right]$$

4kT=16.4E-21 J at T = 298 °C

$$NG = 1 + \frac{R_f}{R_g}$$



See Application Note sboa066a "Noise Analysis for High Speed Op Amps"

This is the general analysis circuit for op amp output noise including all noise sources. It is important to remember that the specs in a data sheet do not include the total noise due to the external components. Therefore vendors can mislead one to believe their part is lower noise when in fact they are required to use large resistors possibly giving higher overall noise even if the input voltage noise for the op amp itself is quite low.

Noise can be a very confusing issue. Some points to keep in mind.

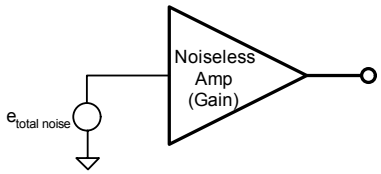
The only noise that can be measured is at the output of the amplifier.

Input referred noise is simply the output noise divided by the gain back to the input that you care about - could be the non-inverting input, inverting input, or the input of a prior stage.

Output noise power is made up of the sum of numerous noise contributors. Often, one or two of these are clearly dominant and swamp out all others. This leads to simplified noise equations that drop out terms - leading to much confusion. General equations should include a fairly complete model even if some terms are often (but not necessarily always) negligible.

Non-Inverting Input Referred Total Noise

- **Dividing the total output noise by the non-inverting gain yields an input referred noise term (e_i).**



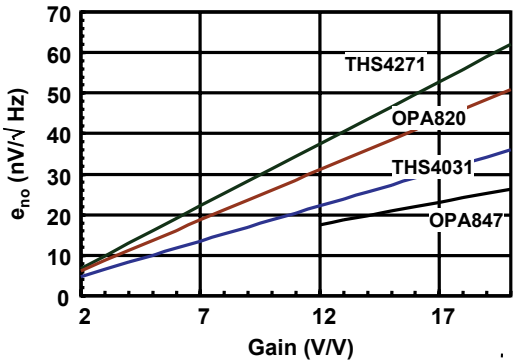
$$e_i = \sqrt{e_{ni}^2 + (i_{bn}R_s)^2 + 4kTR_s + \left(\frac{i_{bi}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}}$$

- **Where NG = 1 + Rf/Rg = Noise Gain**
  - This shows that, as gain increases, the input referred noise approaches just those terms physically present at the non-inverting input. Conversely, at low gains, the total input referred noise can be dominated by the terms at inverting input - this is commonly the case for current feedback op amps.

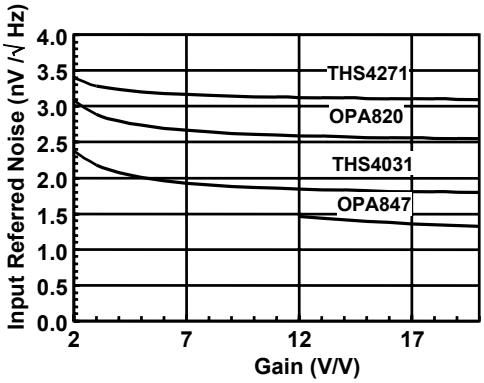
For any particular amplifier, the gain and feedback resistors selected will give a dominant term in the expression above. Picking a high feedback resistor value will increase noise quickly if you are not careful.

Voltage Feedback Non-Inverting Amplifier Noise

Total output noise is plotted, holding fixed feedback resistor of 402 O. Noise voltage increases with gain. The OPA847 minimum gain is12.



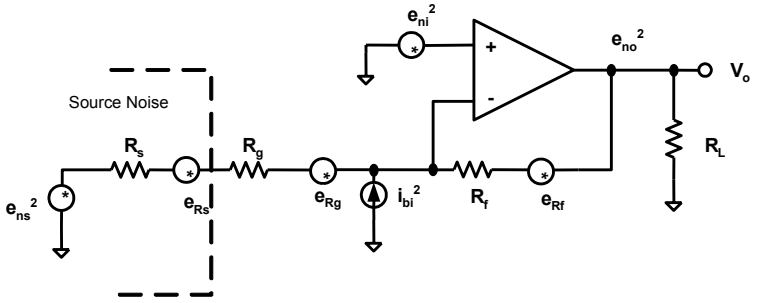
The output noise is divided by the gain to show that minimum input referred noise occurs at higher gain. Using the amplifiers in inverting mode will reduce the total input referred noise.



Non-inverting amplifiers configuration although is the most common is not necessarily the circuit which gets the lowest noise. The plots here show that as the gain is increased the overall output noise goes up. As you increase the gain, the input referred noise minimum will occur at higher gains, since the output noise is divided by the Noise Gain.

The THS4271, OPA820, and THS4031 are unity gain stable parts with very low noise input referred noise. To get better low noise one would have to use a high gain amp like the OPA847 in an inverting configuration with the loop gain shaping compensation discussed earlier.

Inverting Amplifier Noise Model with Input Matching



$$e_{no} = \sqrt{e_{ni}^2 \cdot NG^2 + 4kT\left(\left(R_s + R_g\right)\|R_f\right) + \left(i_{bi}R_f\right)^2 + e_{ns}^2\left(NG - 1\right)^2}$$

$$NG = 1 + \frac{R_f}{R_s + R_g}$$

$4kT = 16.0 \times 10^{-21} J \rightarrow @\, T = 290^{\circ}K$

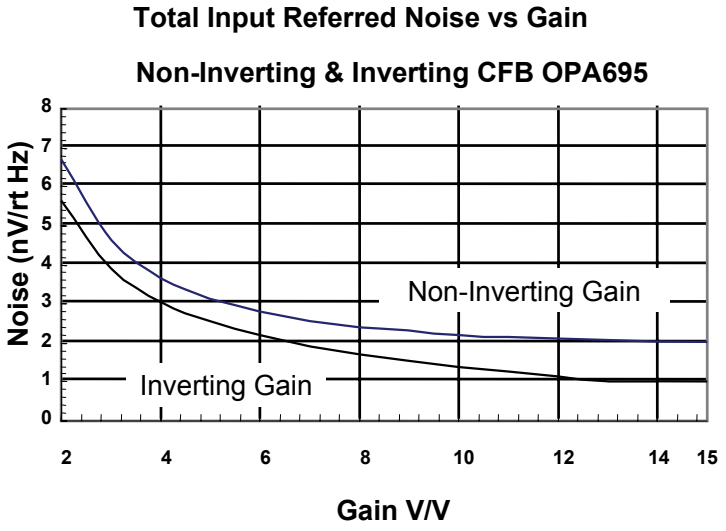
T = Temperature

Dividing the total output noise by the inverting gain will mathematically develop an input noise that, if this term were placed at the input of a noiseless amplifier of the same gain - you would get the same total output noise.

This is particularly useful for low input voltage noise parts when $R_g = R_s$. Total input referred noise in this case can be very low. (OPA695 and OPA847 are good examples).

Current Feedback Noise

- CFB Amps at high gains have low input referred noise
- Inverting CFB Amps will have even lower noise then non-inverting configuration
- This also true of Voltage Feedback Amps



One of the most mis-understood concepts of current feedback amps is the noise. It is generally believed that CFB amps are more noisy than VFB; this is not true as is shown in the slide. As the gain is increased the total input referred noise decreases. This phenomenon is also true in Voltage Feedback, but remember when trying to reach high bandwidths the VFB amp bandwidth is decreasing as you increase the gain.

For a given bandwidth, a CFB amp can achieve a low noise design. Just like the VFB the CFB inverting configuration will achieve a lower input referred noise than non-inverting.

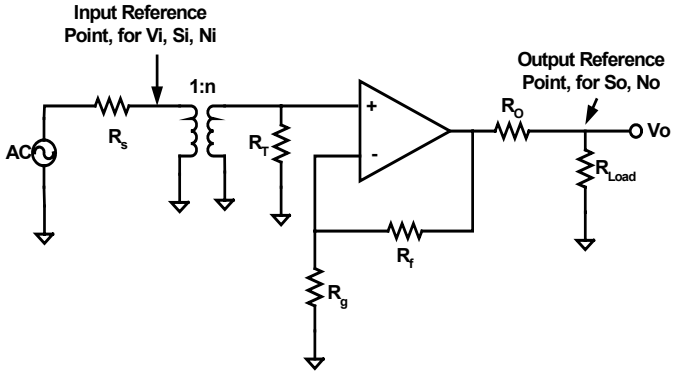
One Possible way to reduce the noise figure is to use a transformer

$$\frac{S_i}{S_o} = \frac{V_i^2 / R_s}{\left(\frac{n \cdot NG \cdot V_i}{2}\right)^2 / R_o} = \frac{4}{(n \cdot NG)^2}\frac{R_o}{R_s}$$

$$\frac{N_o}{N_i} = \frac{(n \cdot NG)^2 R_s}{4R_o} \cdot \frac{2KT + i_n^2 n^2 \frac{R_s}{4} + \frac{e_n^2}{n^2 R_s}}{KT}$$

$$\frac{S_i}{S_o}\frac{N_o}{N_i} = \left[2 + \frac{i_n^2 n^2 \frac{R_s}{4} + \frac{e_n^2}{n^2 R_s}}{KT}\right]$$

$$\mathrm{NF} = 10\mathrm{Log}\left[2 + \frac{\left(i_n n \frac{R_s}{2}\right)^2 + \left(\frac{e_n}{n}\right)^2}{KTR_s}\right]$$



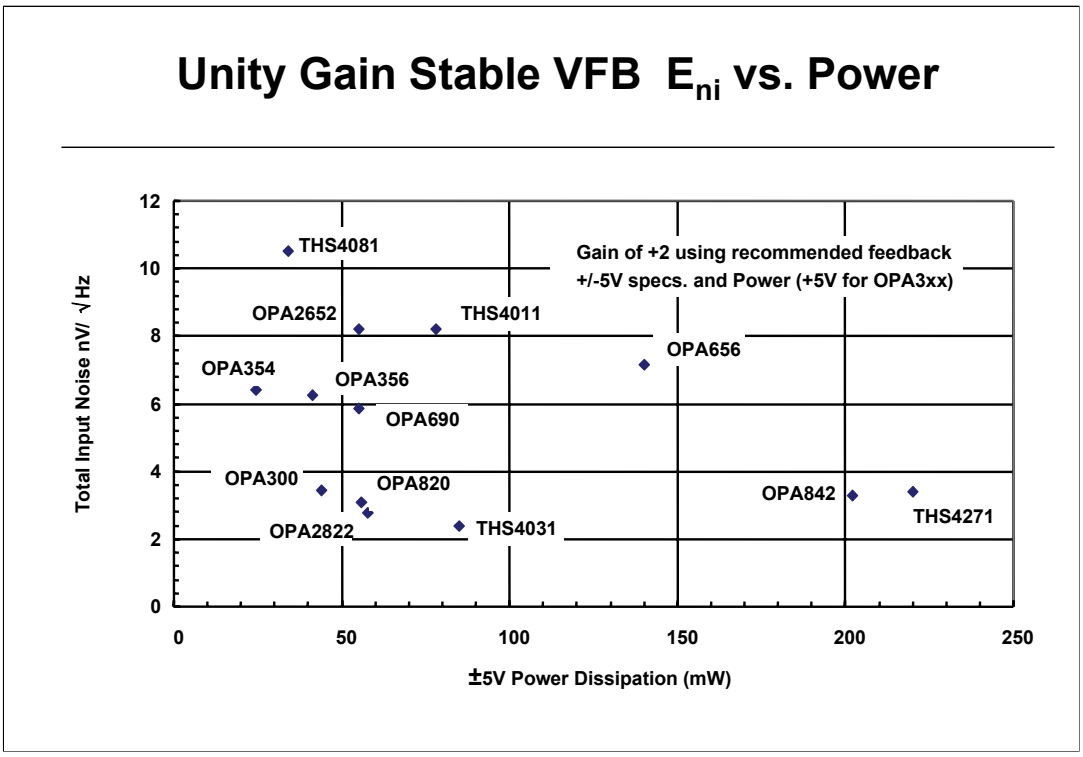
$$NG = 1 + \frac{R_f}{R_g}$$

This is for Rt = n^2*Rs

$$4kT = 16.0 \times 10^{-21} J$$

$$T = \text{Temperature} = 290K$$

A very common way of dealing with noise and impedance matching is through the use of transformers. This circuit can improve the Noise Figure for the design.



Unity gain stable and low noise is one of the hardest specs to design a high-speed amplifier. In the 50mW range there are many parts to select from starting with low noise bipolar parts OPA2822 or OPA820. Just slightly higher noise is CMOS amplifiers OPA35X series with noise in the 4 to 6 nV range.

As you apply more power then OPA842 and THS4271 provide good parts for low gain and low noise applications offering much lower distortion.

The following tables compute the total input referred voltage noise using different gain settings and the recommended resistor values for a range of high speed voltage feedback parts.

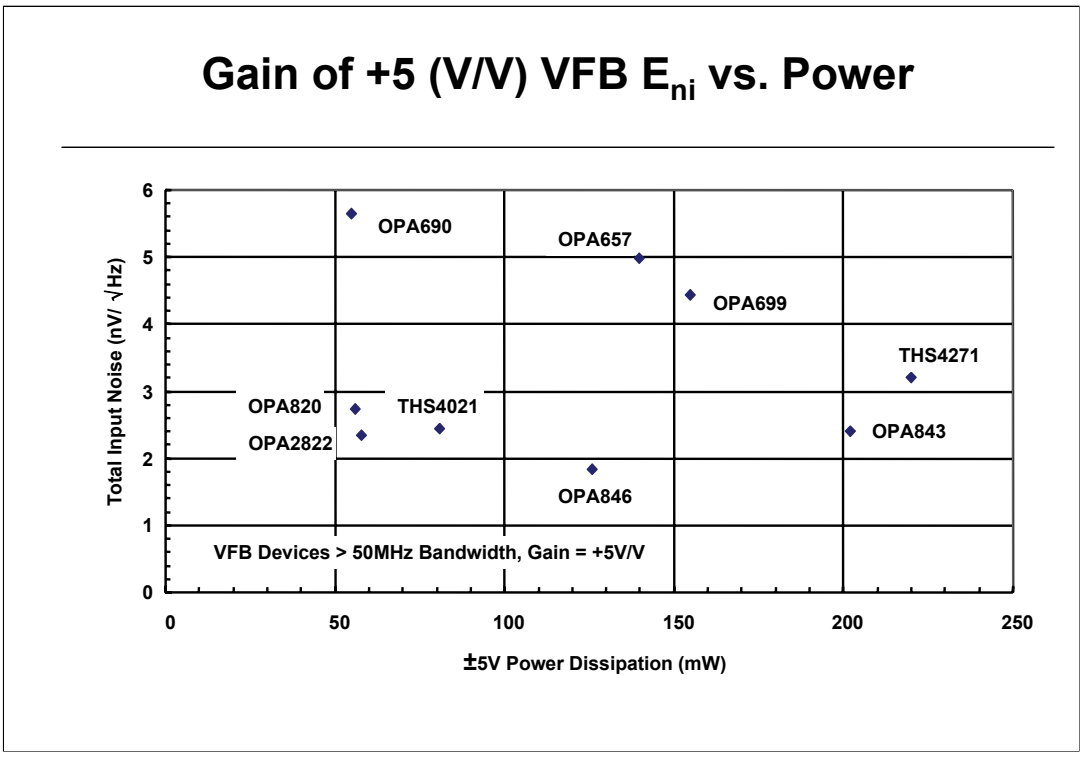
Many of these parts have multi-channel versions not shown

These are plotted vs. quiescent power. Some of the higher power parts, with low noise, also have very low distortion.

Parts are selected for each plot to be stable at the gain shown for the plot and to also have >50MHz closed loop bandwidth at the gain shown.

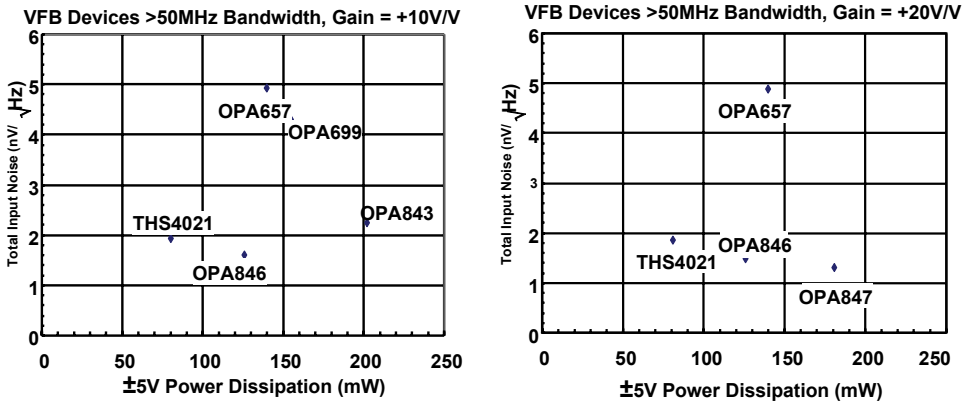
Quiescent power is typical supply current time 10V total voltage across the parts.

The OPA3xx parts use their maximum rated 5V supply - many of the other parts can also run on +5V only cutting their power in half with a slight increase noise.



Few parts are available that give >50MHz bandwidth at a gain of 5V/V. However, the total input referred noise is lower at these higher gains.

Gain of +10/+20 (V/V) E_{ni} vs. Power



Once again the two plots show ± 5V parts at gains of 10 and 20 V/V and how they stack up in terms of power vs input referred noise. The OPA656 and OPA657 are JFET input amplifiers yet have reasonable voltage noise.

The OPA and THS are bipolar input stages with varying bandwidths. They show that to achieve the lowest input noise, a higher total power dissipation is required.

Equivalent Noise Bandwidth

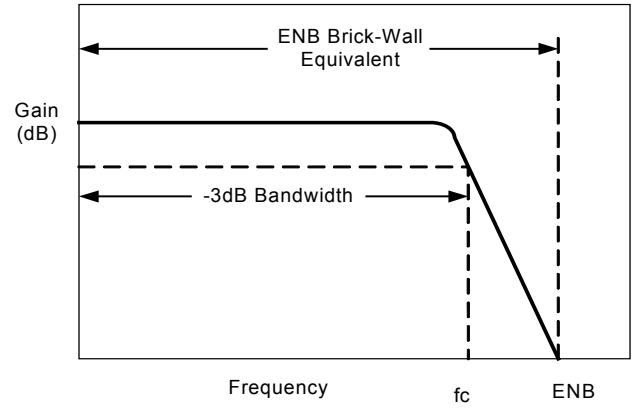
$$e_{rms} = \sqrt{\int_0^{\infty} T(f)^2 \cdot e_{in}^2 \cdot df}$$

$$T(f) = \frac{1}{1 + j(2\pi fRC)}$$

$$e_{rms} = e_{in} \cdot \int_0^{\infty} \frac{1}{\sqrt{1 + (\frac{f}{f_C})^2}} df$$

$$f_C = \frac{1}{2\pi RC}$$

Filter Order	ENB
1	1.57 x f_c
2	1.11 x f_c
3	1.05 x f_c



As an example: For the OPA847 at gain of 20 the input referred integrated noise assuming a single pole response would be -

$$1.2\text{nV} \times \sqrt{1.57 \times 350\,\text{E}6} = 28.13\,\mu\text{V}(\text{RMS})$$

The discussion so far has computed the total input referred spot noise for the op amp. An integrated noise is often of more interest. This is calculated by multiplying the the spot noise times the square root of the Noise Power Bandwidth (NPBW).

The Noise Power Bandwidth is that rectangular frequency span that will produce the same integrated noise power as the actual frequency response shape - the filter orders shown above are assumed to be a post filter to the amplifier stage. The table shows the relationship from the -3dB cutoff frequency to the noise power bandwidth. The 2nd and 3rd order ratios are assuming a maximally flat Butterworth filter.

Going from Open-Loop to Closed Loop Performance

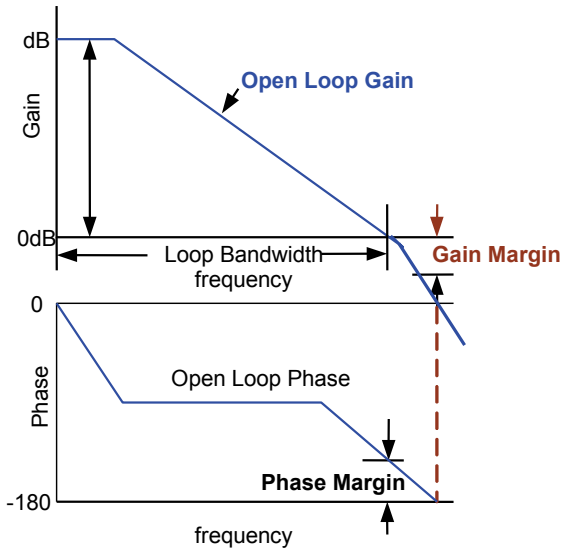
Bode Analysis for Op Amp Loop Gain

◆ The plot is a first order plot in magnitude with the phase for higher order poles shown.

◆ Phase margin is measured from the point in frequency where the 1/f (feedback factor) equals the open loop gain. (0dB or unity gain VFB shown here)

◆ This phase is subtracted from 180 degrees.

◆ Gain margin is measured from 180 degrees and is the difference from zero dB (magnitude).



The above plot helps to show the basics of bode analysis. In reality every amplifier has 2nd order poles or higher that determine the actual phase margin of the amplifier.

Most Individual high speed op amps are designed and characterized for a particular gain, load, and feedback network.

Many factors will influence the final frequency response seen in the application.

- Load and particularly any parasitic C on the output pin
- Noise gain for VFB and feedback impedance for CFB.
- Gain setting
- Source impedance for inverting configurations.

The nominal design point for most high speed amplifiers is to achieve a maximally flat Butterworth response to get a good compromise between bandwidth and pulse response.

Changing the noise gain (VFB) or feedback impedance (CFB) can dramatically change this closed loop response.

The open loop gain and phase curves allow a means of predicting the results - the simulation macromodels mimic this response giving good predictive results in simulation as well.

Computing Closed Loop Response from the Phase Margin

Amplifier stability and phase margin are generally reviewed in terms of Φ_m and ω_n. As amplifiers are viewed more often in the time domain then in the frequency domain. Therefore one can associate ringing in the time domain to stability in the frequency domain.

$$Peaking(dB) = 20 \cdot Log\left(\frac{Q}{\sqrt{1-\left(\frac{1}{2Q}\right)^2}}\right)$$

Φ_m = Phase margin in degrees
(at Φ_m = 65.54°, $Q = 0.707$)

$$\Phi_m = \tan^{-1}\left[\frac{1}{\sqrt{\sqrt{Q^4+0.25}-0.5}}\right]$$

$$\frac{V_o(t)}{V_o} = 1 - \frac{e^{-\left(\frac{\omega_n * t}{2Q}\right)}}{\sqrt{1-\left(\frac{1}{2Q}\right)^2}} * \sin\left[\omega_n * \sqrt{\left(1-\left(\frac{1}{2Q}\right)^2\right)} * t + \arccos\left(\frac{1}{2Q}\right)\right]$$

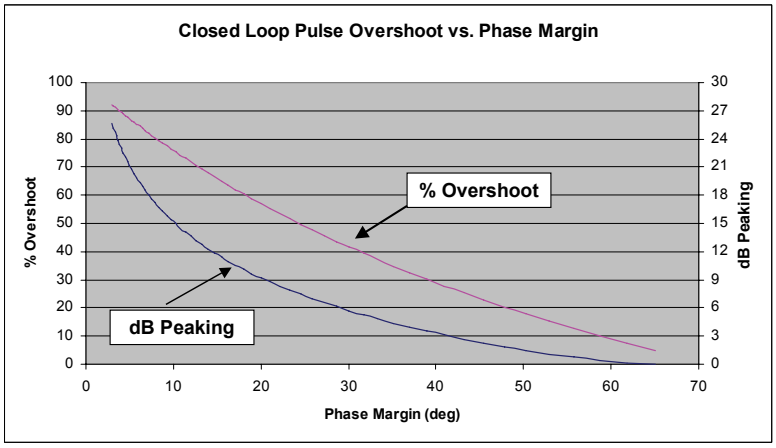
The method starts by laying the noise gain or feedback transimpedance line for the application on top of the open loop gain curve **(SEE PREVIOUS SLIDE FOR CURVES).**

Where that line intersects the Open Loop gain the loop gain has dropped to one and the phase margin can be read by projecting to the phase curve at this frequency. Using that, and the following equation, the Q for the closed loop response can be estimated.

As the noise gain or feedback impedance changes, both the W_o and Q for the closed loop response will change. The peaking for the closed loop response is controlled only by Q, but recognize the W_o will also increase greatly as the noise gain or feedback impedance is reduced

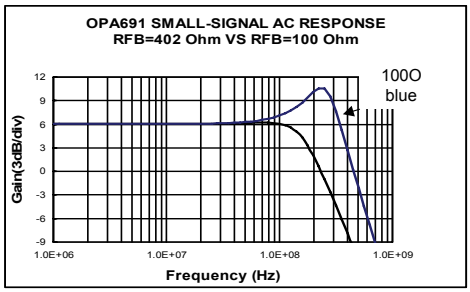
Relationship of Peaking and % Overshoot to Phase Margin

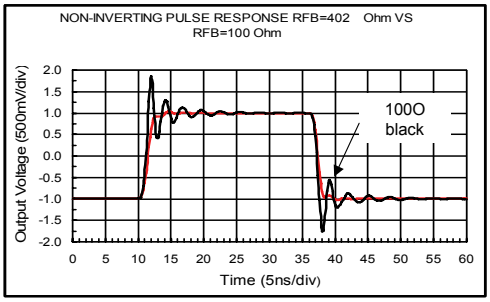
The closed loop response will have a peaking in the SSBW and/or a pulse overshoot that can be related to the phase margin.



The releationship to a time step overshoot is equivalent to the frequency domain peaking. In the time domain it is not unusual to have overshoot which is post-filtered before processed. While in frequency domain applications one is probably more concerned about flat magnitude function.

Gain of +2V/V with nominal 402Ω and reduced 100Ω feedback resistors.





The actual part shows a little more peaking than predicted. The pulse response shows the high overshoot and ringing intrinsic to this higher Q operating point. If pulse response is of interest, this may not be the best solution.

However, if the application is frequency domain oriented, particularly with a post-filter to cut off the high output noise power bandwidth, this reduced feedback R will improve low frequency output noise and distortion and will be stable.

Here we can see peaking in the frequency plot relates to the overshoot in the time plot. A perfectly flat frequency response relates to no overshoot and better settling in the amplifiers time step.

This wideband current feedback op amp has a nominal feedback transimpedance design point to achieve a phase margin of 65.53° which will give a Q = .707 and a maximally flat Butterworth response.

That impedance is $R_f + R_i*(1+R_f/R_g)$ = 402 + 38*(1+402/402) = 478Ω. The open loop gain is 20*log|Z(s)|. To find loop gain cross-over (where the feedback impedance equals the open loop transimpedance) we need 20*log(478) = 53.6dB in ohms (for transimpedance).

Putting this line on the open loop gain curve gives us a 160Mhz intersection with a phase margin of 62°. It turns out that the closed loop F_o for this intersection is 1.414*160Mhz = 226Mhz.

Now reduce the feedback and gain resistor to 100ohms each to get a new feedback impedance = 100 + 38*2 = 176ohms (or 44.9dBΩ) with the same low frequency voltage gain

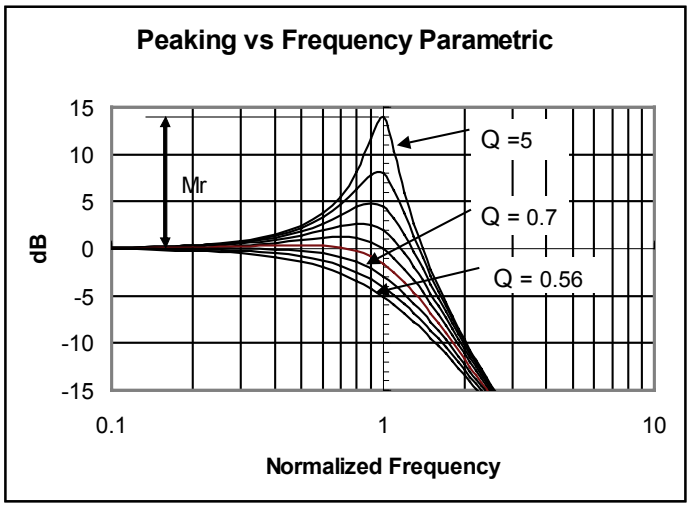
Putting that on the open loop transimpedance gain curve, intersects at 290Mhz with about 40° phase margin (Q = 1.36 and peaking should be 3.3dB).

Associating % Overshoot to Frequency Peaking

◆ Peaking in the frequency domain determines how stable the response is for an amplifier.

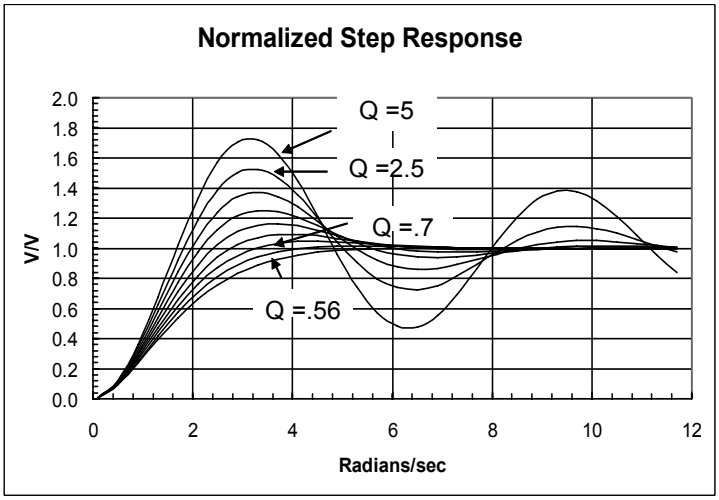
◆ Mr is the amount of peaking measure from zero dB

◆ Marginally stable system is a Q > 5



Associating % Overshoot to Frequency Peaking

- Overshoot relates to peaking and phase margin
- As Q reduces response peaks more giving greater overshoot and ringing.
- For best pulse response Q is less than 0.7



Spice Models

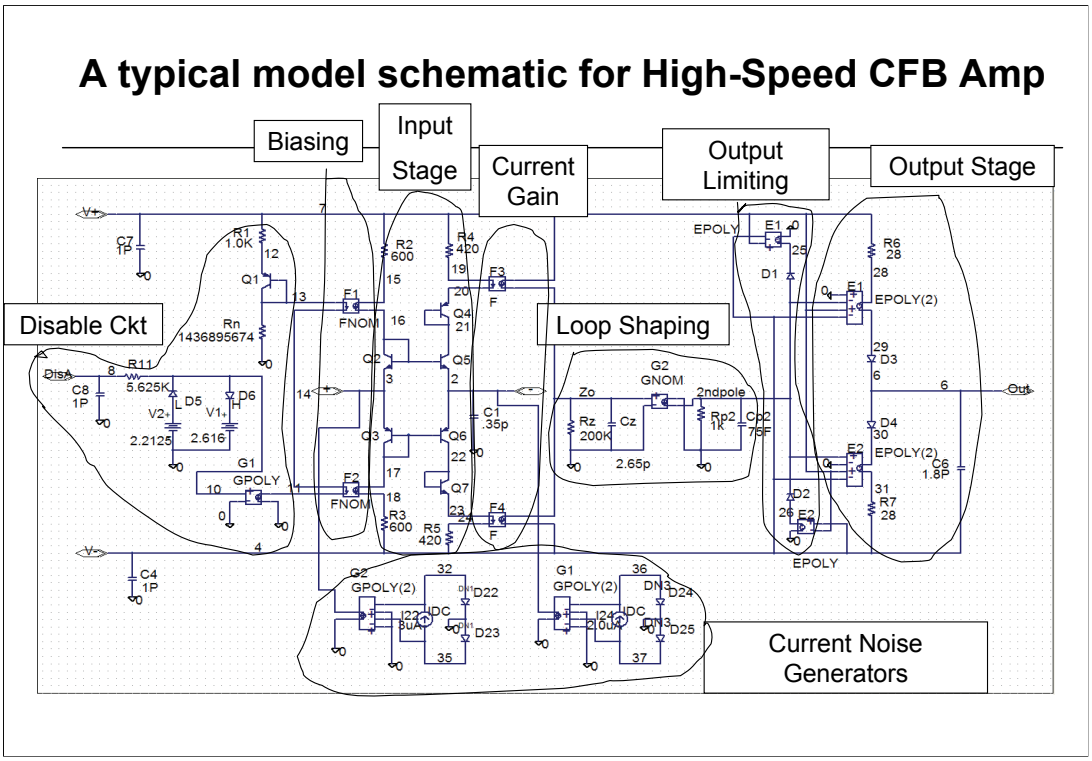
Simulation Models: What we model - and What is not modeled

- **Current**
  - Bias
  - Offset
  - Noise (1/f and flat band)
  - Output
  - Quiescent
- **Voltage**
  - CMIR
  - Output Saturation
  - Offset
  - Noise (1/f and flat band)
  - Supply Range
- Small Signal Frequency Response
- Slew Rate
- OPEN-LOOP Gain and Phase
- CMRR, PSRR
- Time Step (Rise and Fall Time)
- Input Impedances
- Output Impedances
- Special Functions (Disable, Limiting, etc)

What is Not Modeled!!!

- **2nd and 3rd Harmonic Distortion, Package Parasitic Components**
- **Temperature Variation, Process Variation**

Simulation Models designed and checked out in PSpice have small differences when using Spice 2.6G and 3.0F simulators. With small modifications the models will work on all versions of spice. Schematic capture programs vary, but all models are in net list sub-circuit (.subckt in Spice) and can be attached to a schematic symbol.



A typical CFB spice model tries to duplicate the functions within our high-speed amplifiers. The input stage provides many of the input spec related parameters. Current gain is provided equivalent to the full transistor model. Open loop transimpedance gain is done by a couple of poles, one for low frequency and the other for the 2nd order effect. In some cases the 2nd combination introduces a 3rd order pole to the feed forward path. Output liimiting controls the signal levels prior to the final output stage, therefore matches the saturation effects seen in a typical ampliifer. Finally the output stage reproduces the output impedance and current capabilities for the amplifier.

The disable circuit shuts down the amplifier similarly to the full transistor device. Finally the two circuits at the bottom allow current noise at the output of the amplifier to multiply by the external components. The voltage noise is created with the input transistors.