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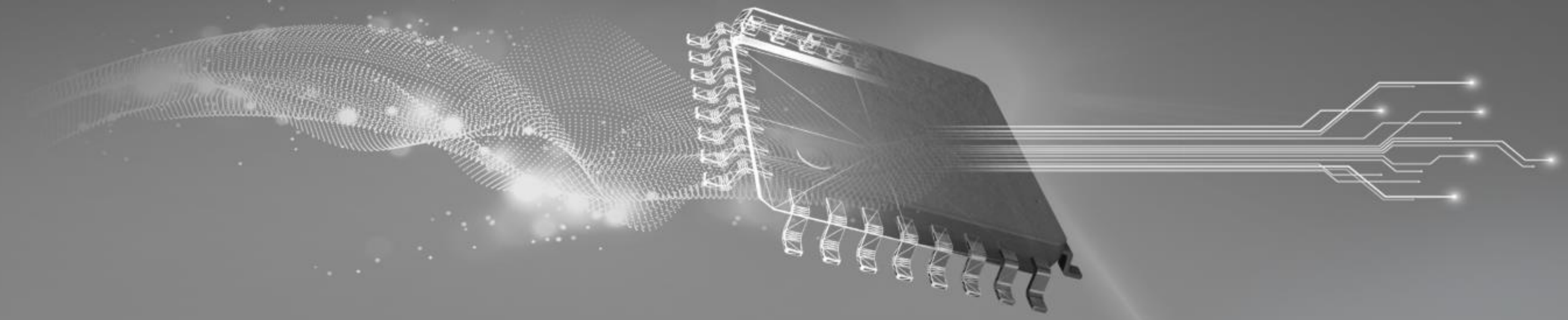


Influence of Layout on EMI performance of Buck-Boost Converters

Brigitte Hauke, APP, BMC-BCS

Agenda

- EMI Basics
- Basic Operation of a 4-Switch Buck-boost Converter
- Difference between Schematic and Real World Components
- Board Layout Rules and How to Review It

- Real world example with TPS63070

EMI BASICS

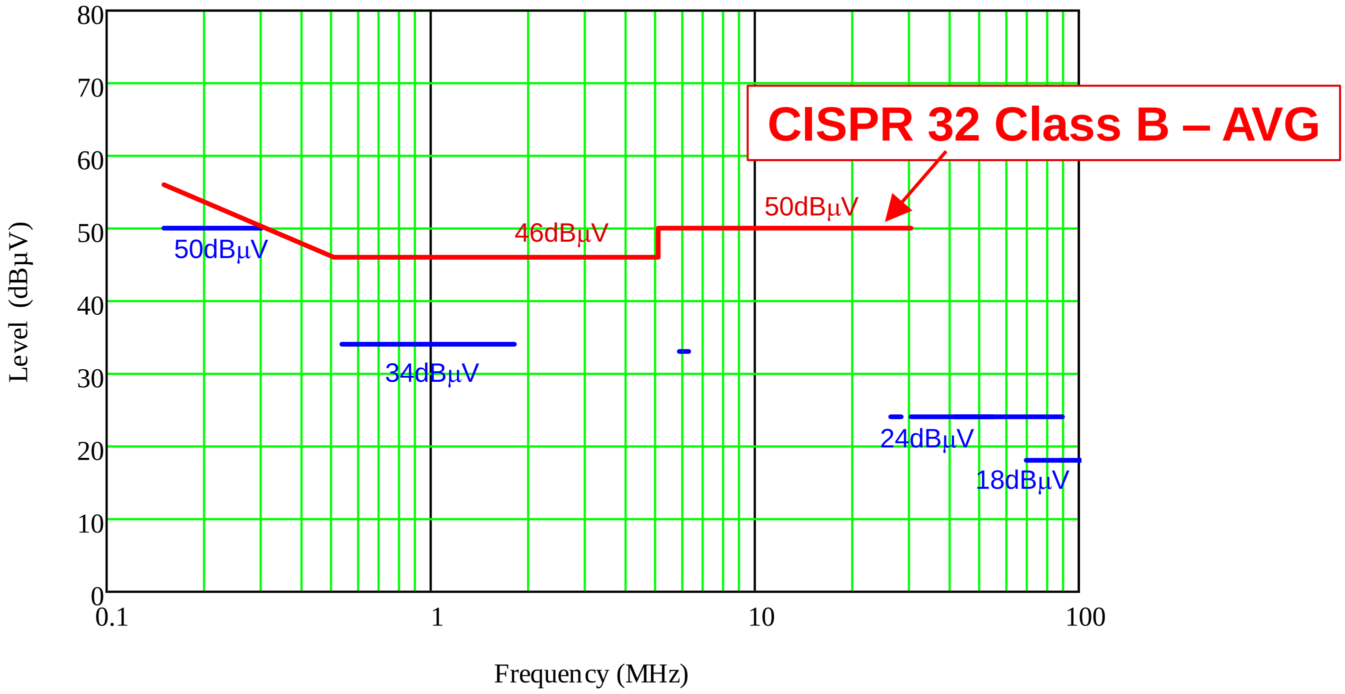
EMI Model

- EMI needs
  - Aggressor
  - Path
  - Susceptor
- Measured on Systems not components
  - All components can comply but system still does not comply
- DC/DC converter
  - Hot loops
  - Important nodes

Conducted and Radiated EMI

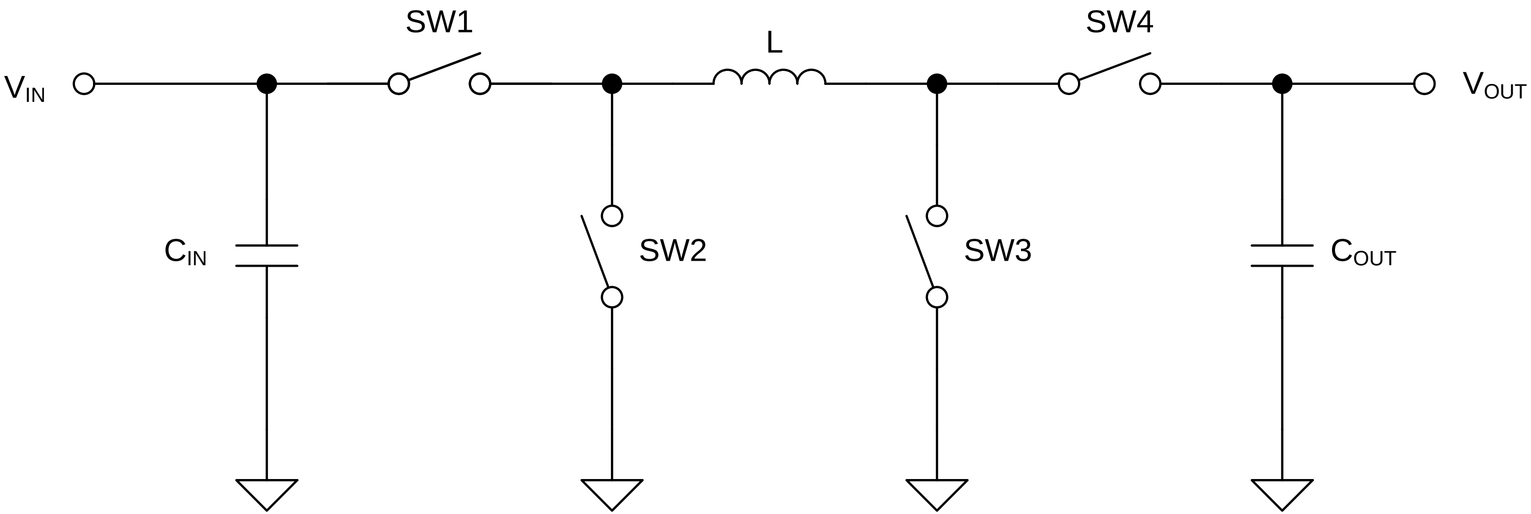
- Conducted EMI
  - Differential mode vs. common mode
  - Reference GND necessary (drives setup specification for compliance measurements)
  - Termination
  - Layout and Component selection important
  - 10kHz to 30MHz (automotive 108MHz)
- Radiated EMI
  - Primarily Layout Dependent
  - Shielding
  - Filtering
  - 30MHz to 1GHz
- Peak, Average or quasi-peak measurements

CISPR 32 (class B) vs. CISPR 25 (class 5) conducted EMI average limits

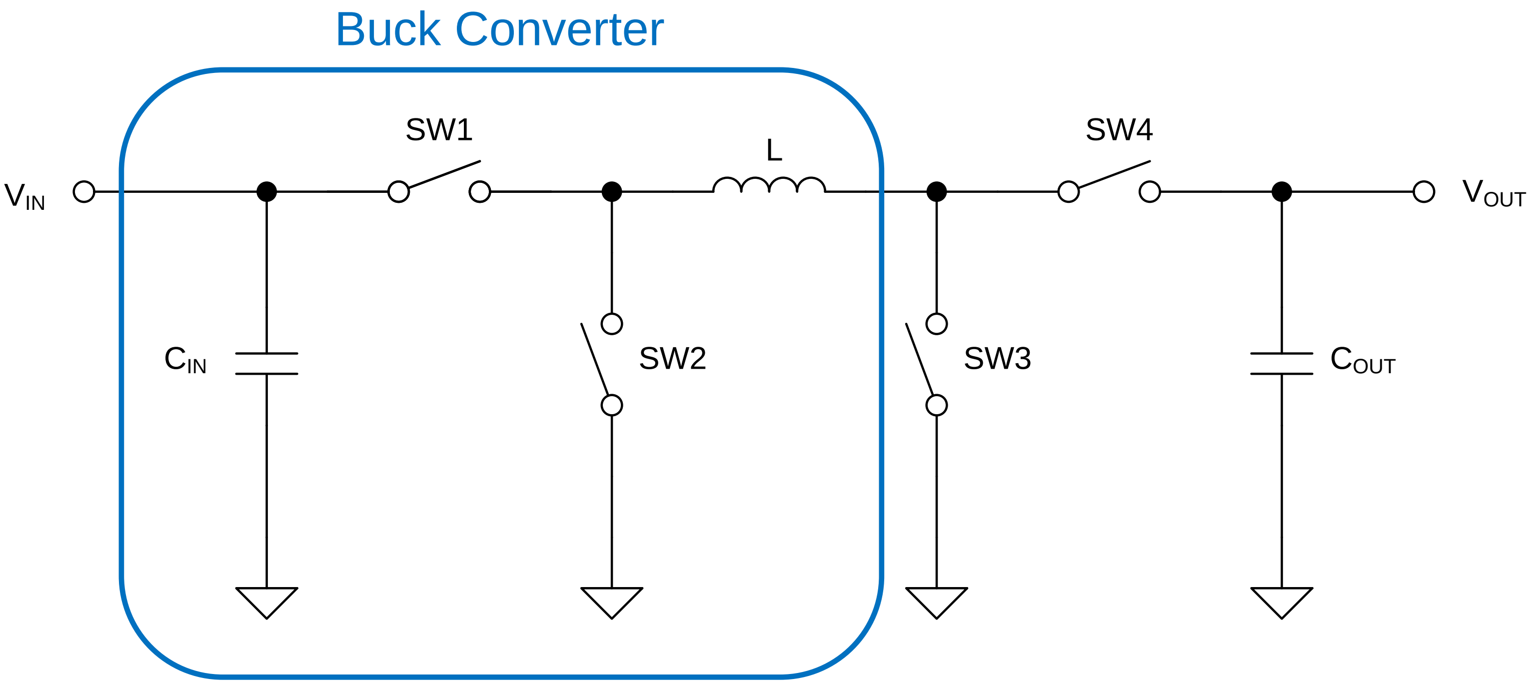


BASIC OPERATION OF A 4-SWITCH BUCK-BOOST CONVERTER

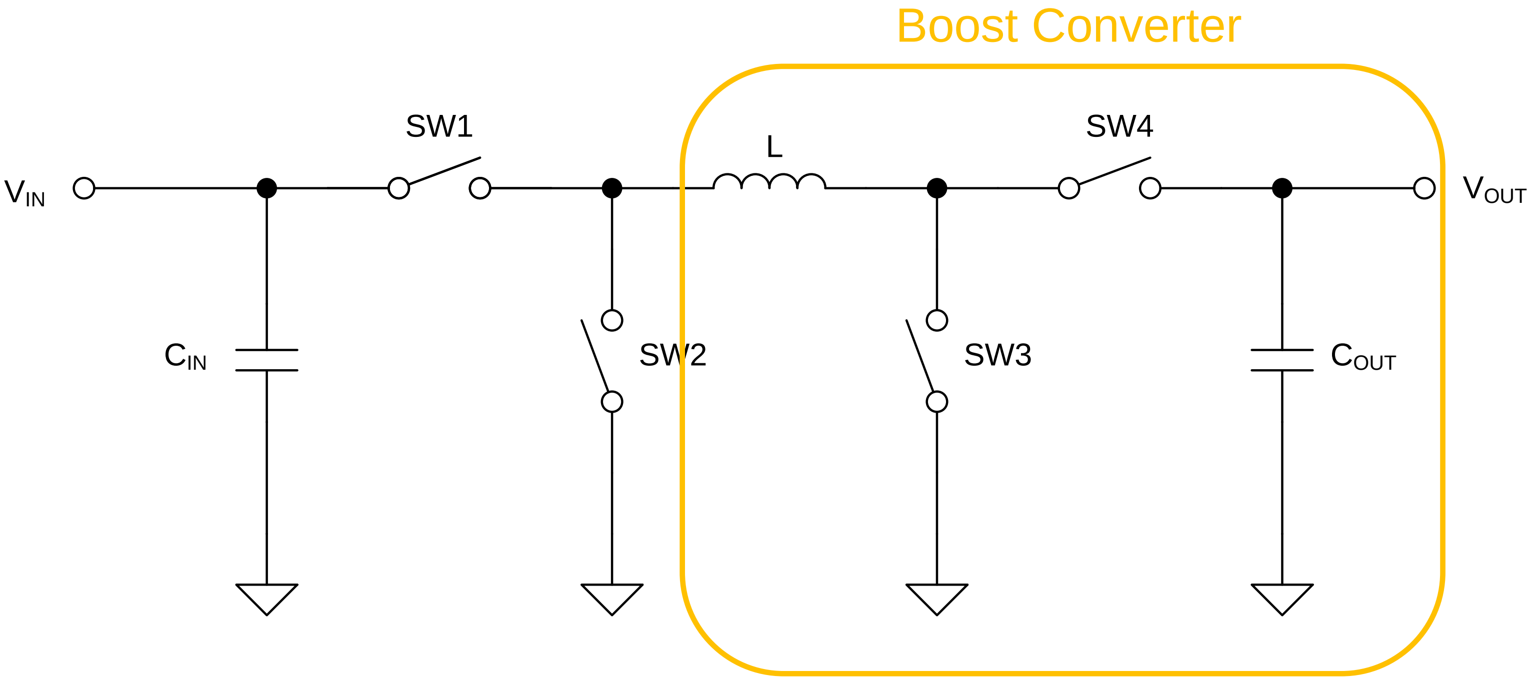
4-Switch Buck-boost Converter



4-Switch Buck-boost Converter

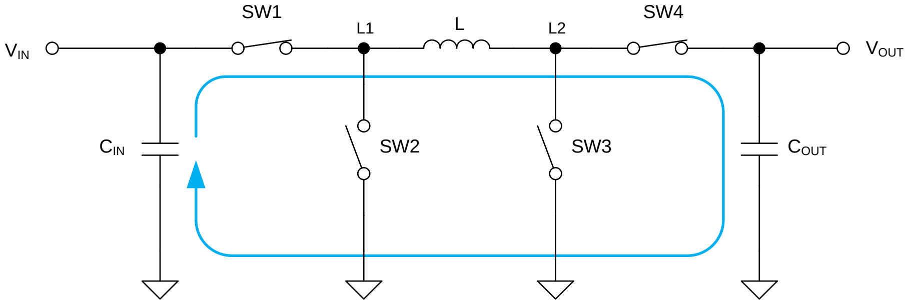


4-Switch Buck-boost Converter

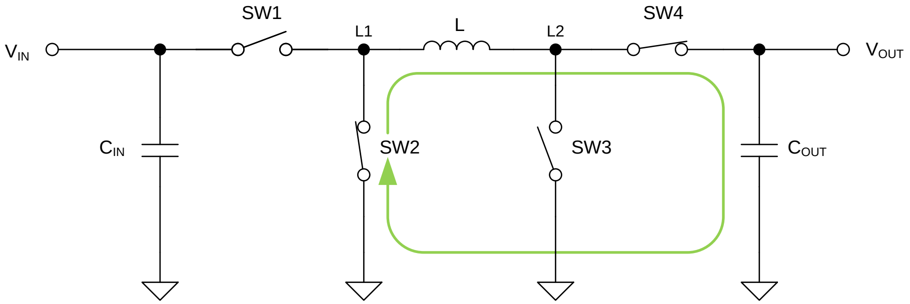


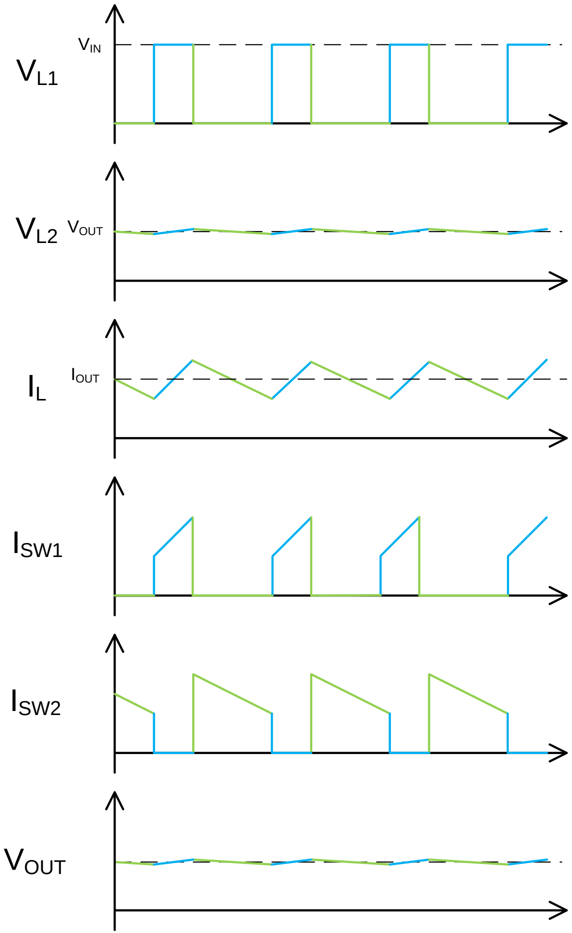
Buck Operation

Power Switch SW1 on



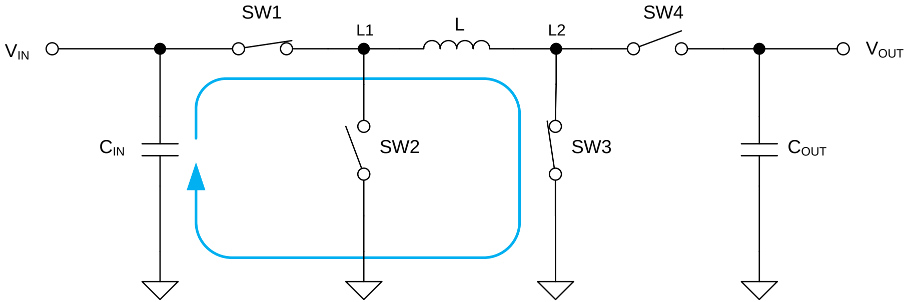
Power Switch SW1 off



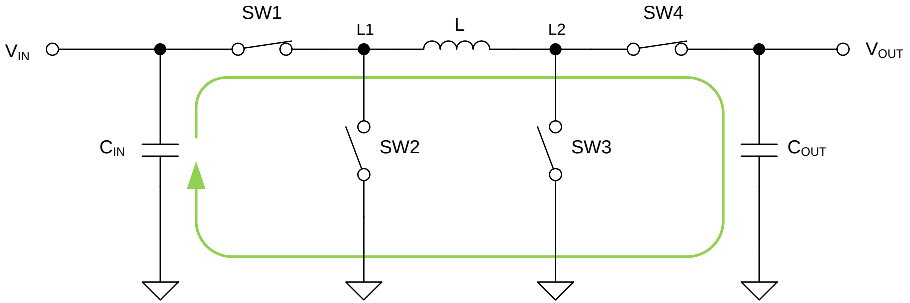


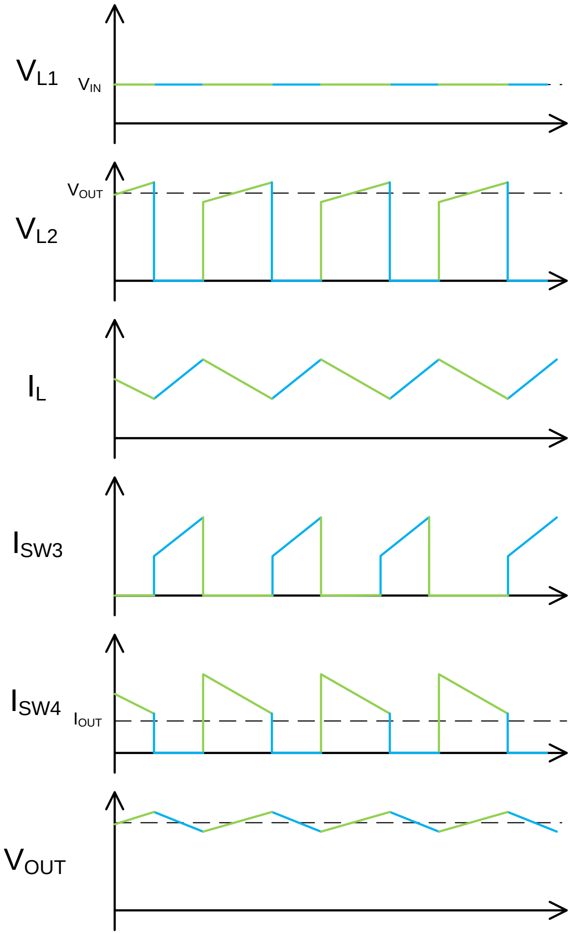
Boost Operation

Power Switch SW3 on



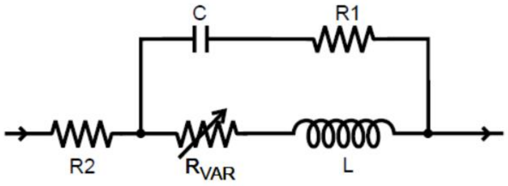
Power Switch SW3 off

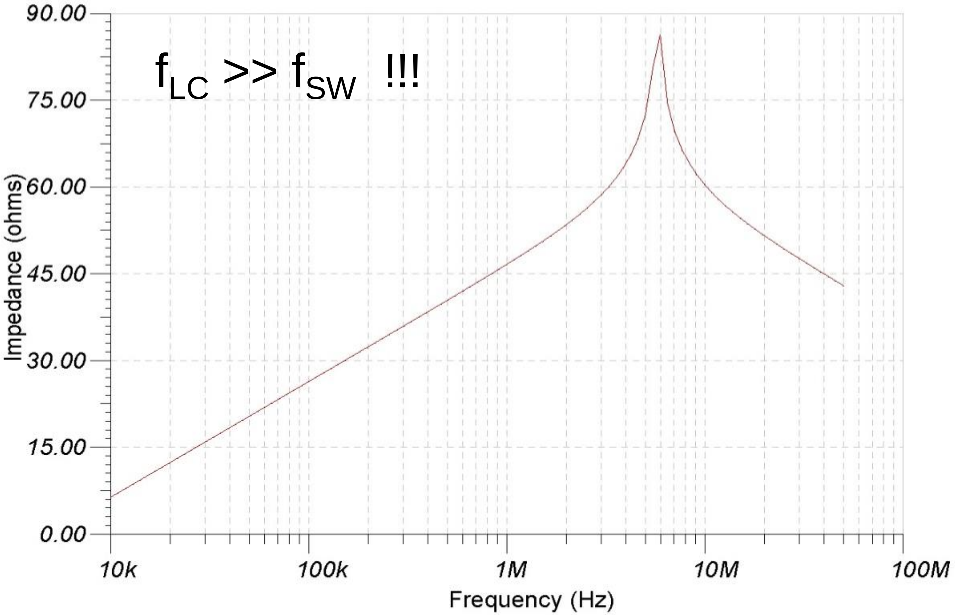




DIFFERENCE BETWEEN SCHEMATIC AND REAL WORLD COMPONENTS

Inductors – Parasitic Components



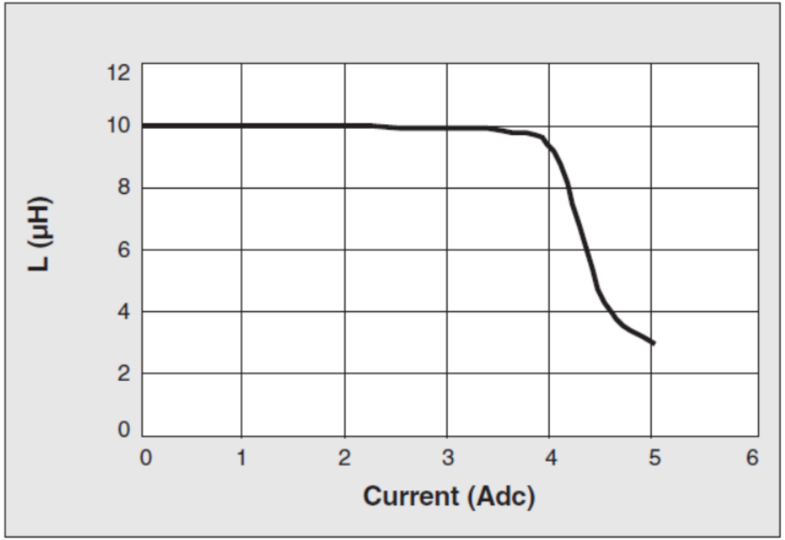


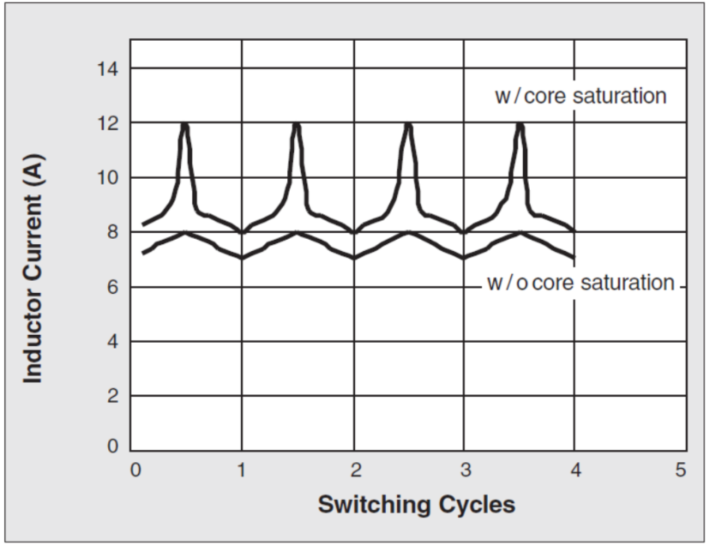
Real-world inductors

- parasitic capacitance causes ringing

Inductors – Saturation Current

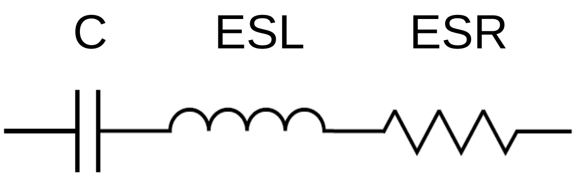
- Inductor current includes a DC component
- DC current biases core and can cause it to be saturated with magnetic flux
- **Saturated inductor** is not an inductor – it's a **piece of wire**





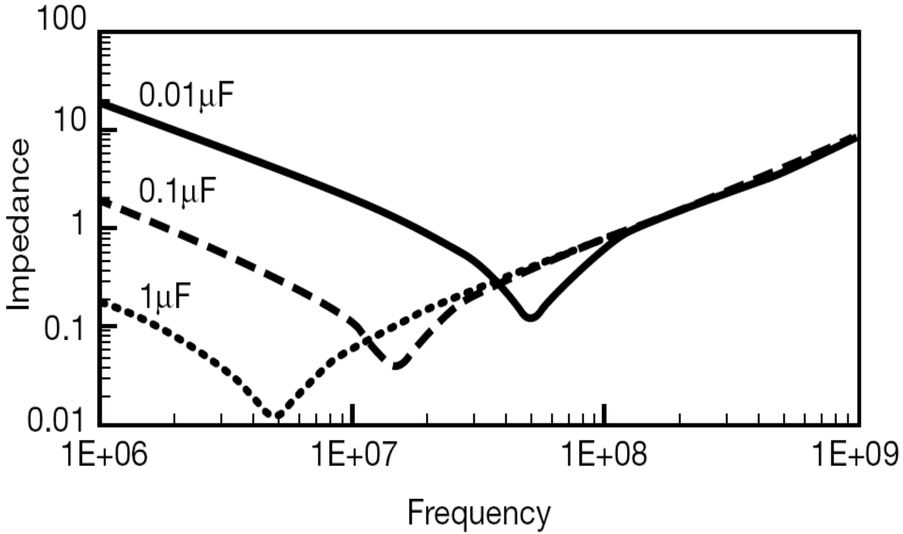
Source: Coilcraft

Frequency Behavior of Ceramic Capacitors

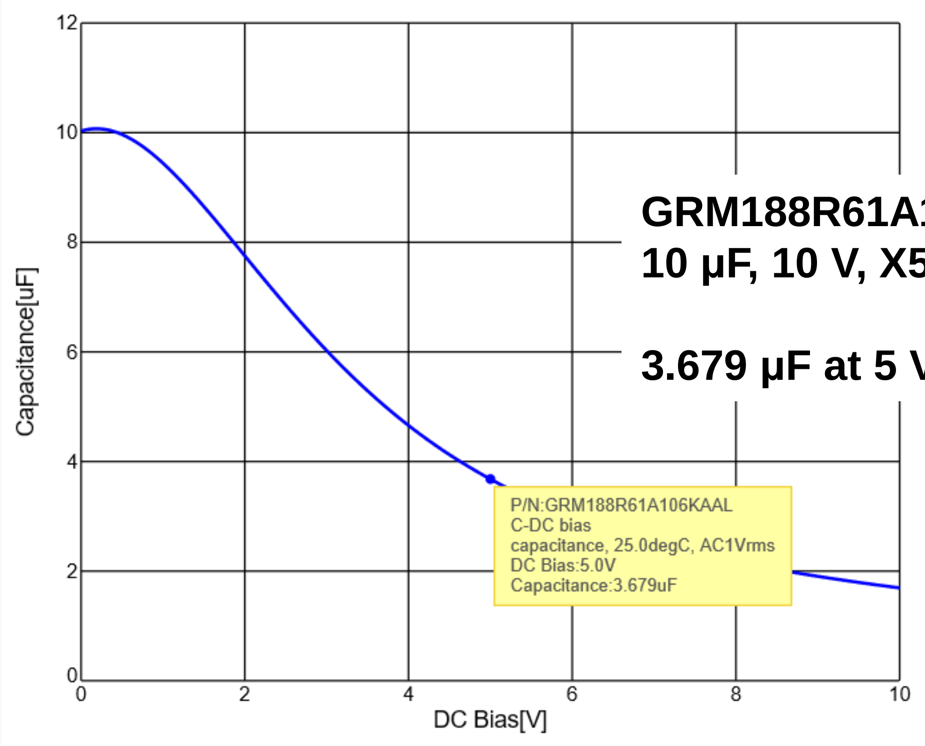


Resonance Frequency

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{ESL \cdot C}}$$



DC Bias Behavior of Ceramic Capacitors



GRM188R61A106KAAL
10 µF, 10 V, X5R, 1608M/0603

3.679 µF at 5 V

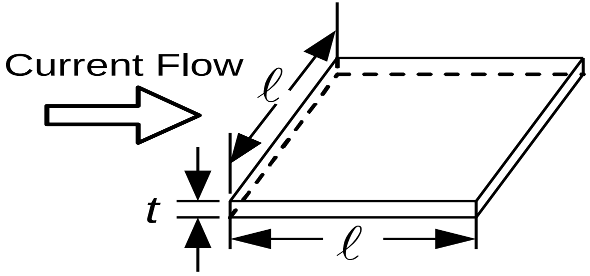
Source: muRata

Design for low EMI

- Starts with schematic
- Difference between schematic symbol and real world components
- **Line in schematic is impedance in real world**
- Current flows in loops!
- Help the layout person with good schematic drawings and hints for the important nodes and loops
- Additional hints for DC/DC converter design
  - High f caps
  - Input and output cap network instead of several times same cap
  - Shielded inductors

BOARD LAYOUT RULES AND HOW TO REVIEW IT

Count Squares to Estimate Trace Resistance



$$R = \frac{\rho \times \ell}{t \times \ell}$$

$$R = \frac{\rho}{t}$$

Copper resistivity is 0.264mΩ/cm at 25°C and doubles for 254°C rise

Thickness (mm)	mΩ per Square (25ºC)	mΩ per Square (100ºC)
0.0175	1.0	1.3
0.035	0.5	0.65
0.07	0.2	0.26

Stray Inductance and Stray Capacitance

- Most problems are caused by stray inductance and capacitance between:
  - Components and the ground plane
  - Tracks and the ground plane
  - Tracks and other tracks

Stray Inductance and Stray Capacitance

- Equations describing basic behavior of inductors and capacitors:

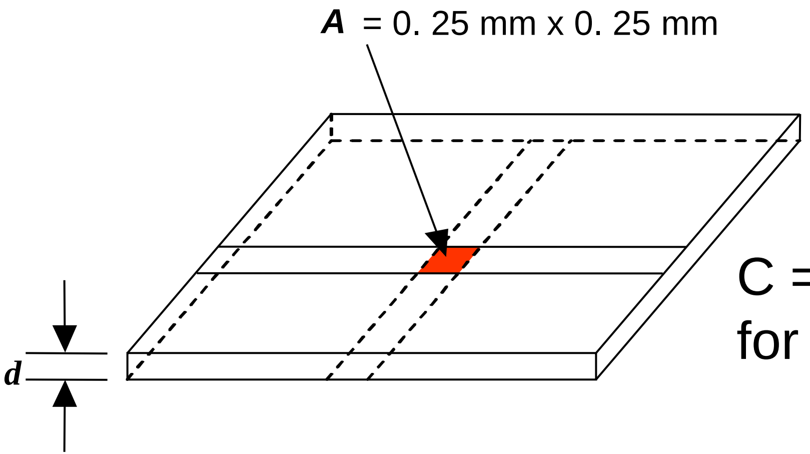
$$I = C\frac{dV}{dt} \qquad V = L\frac{dI}{dt}$$

- High slew-rate voltages across stray capacitance
=> **unwanted *currents***
- High slew-rate currents through stray inductance
=> **unwanted *voltages***
- Higher signal slew-rate
=> **greater impact of stray capacitance/inductance**
- Higher switching frequency
=> **higher signal slew-rate**

Calculating Stray Capacitance

The capacitance in *pF* between two parallel plates:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

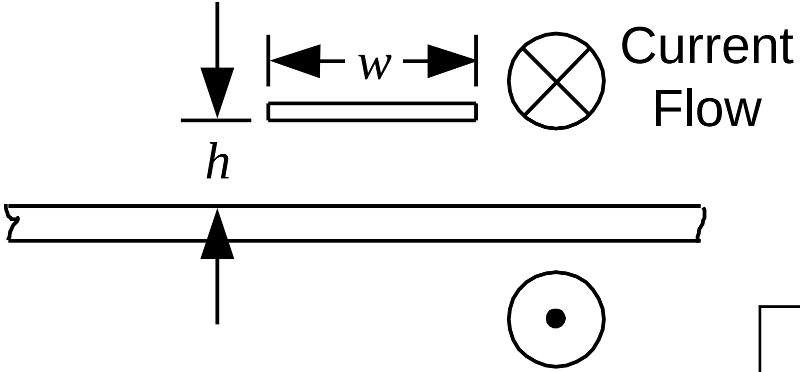


C = 0.01 pF
for FIR 0.25 mm

ε_r = *relative* dielectric constant of the PCB material
d = PCB thickness in millimeters
A = area of parallel plates in square millimeters

PWB Traces Over Ground Planes

Inductance inversely proportional to width

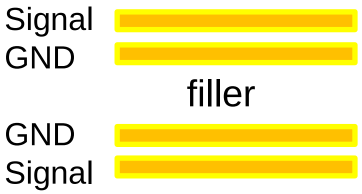


$$L = \frac{2 \cdot \ell \cdot h}{w} \text{ nH/cm}$$

h (cm)	w (cm)	Inductance (nH/cm)
0.25	2.5	0.2
1.5	2.5	1.2

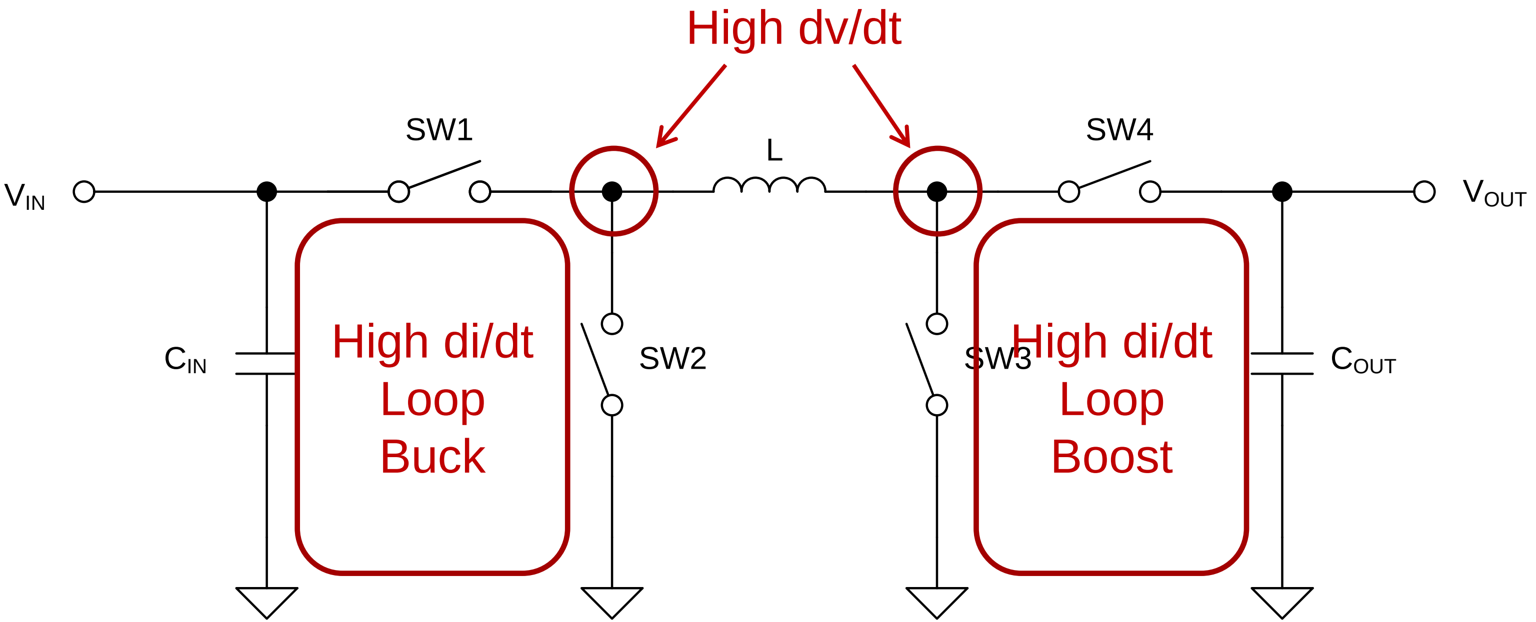
PCB Stack-up

- PCB Stack-up is essential for low EMI board designs
- Place GND layer next to power layer for noise suppression
- Use at least 4 layers and keep the outer layers together for maximum flux cancellation

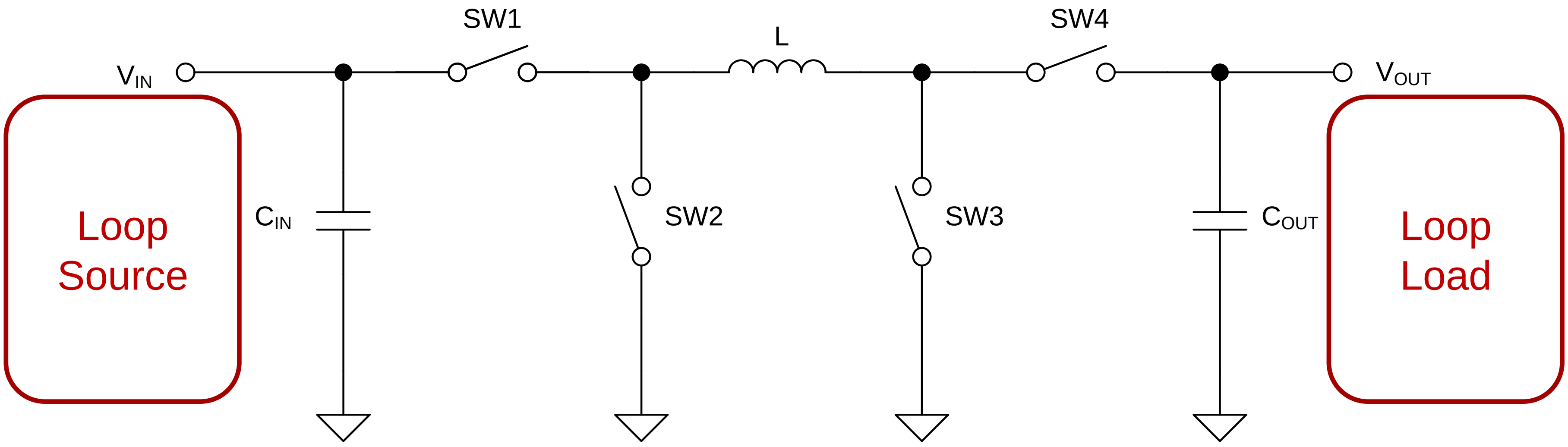


- Make sure there is no cut in the GND layer below the high di/dt paths

4-Switch Buck-boost Converter



4-Switch Buck-boost Converter

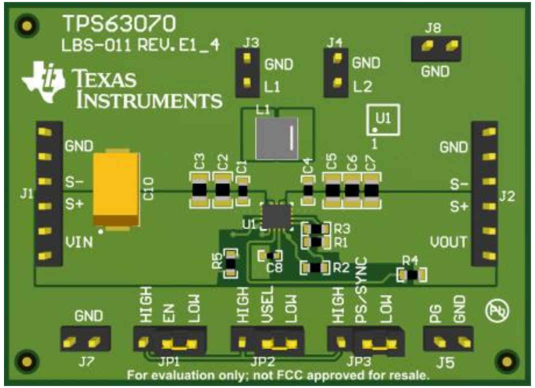


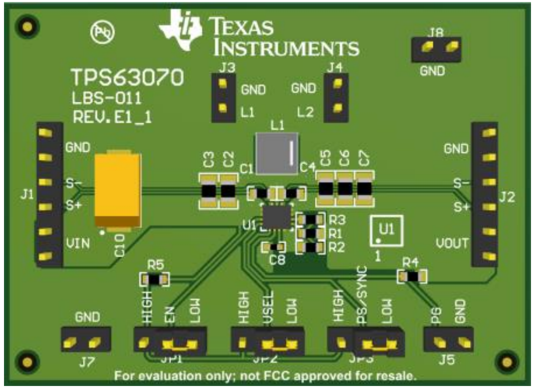
Layout for low EMI

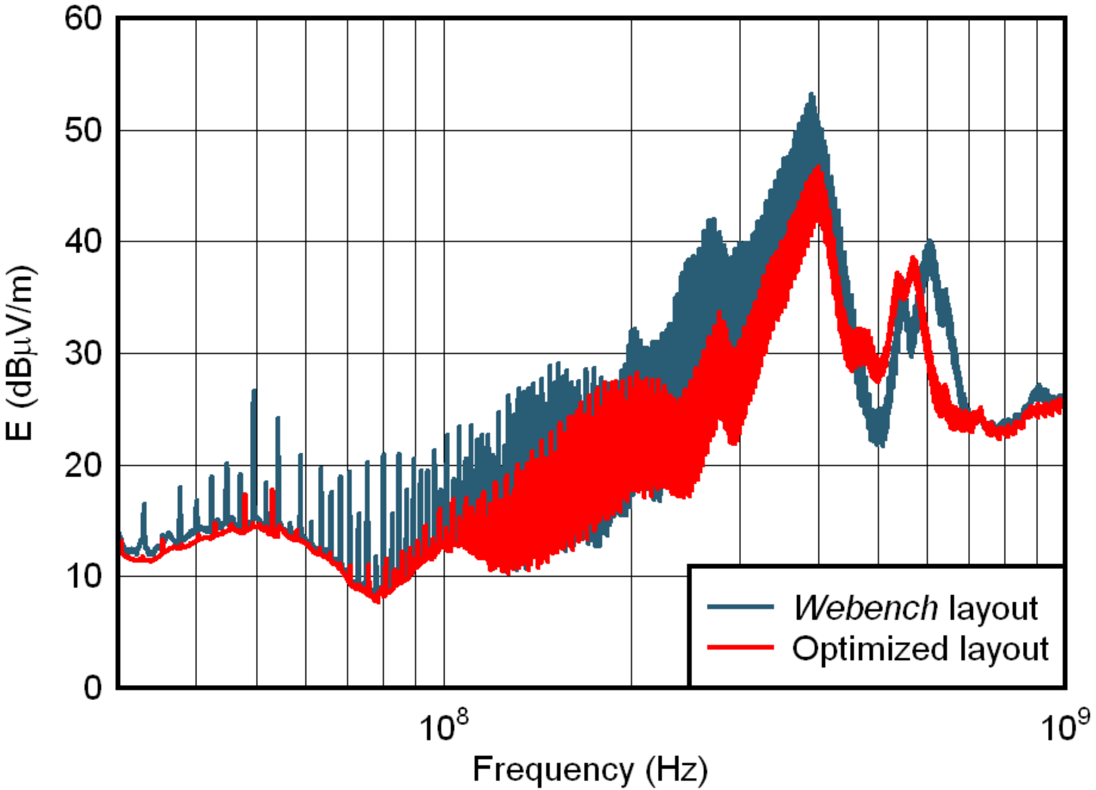
- Start with hot loops
- Use shielding effects
- Use 4 layer board with specific layer stackup
  - Thick center core material
  - Outer layers shield hot loops/important nodes
- Placing small high-frequency caps close to input and output pins might be helpful

REAL WORLD EXAMPLE WITH TPS63070

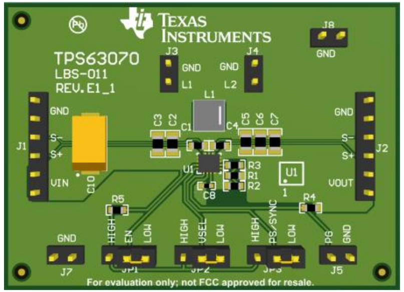
Fast Created Layout compared to Good Layout

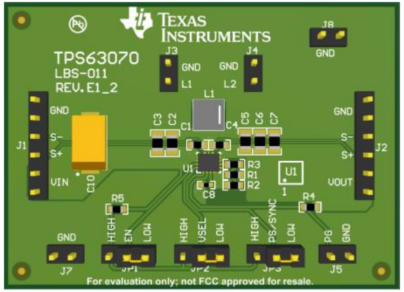


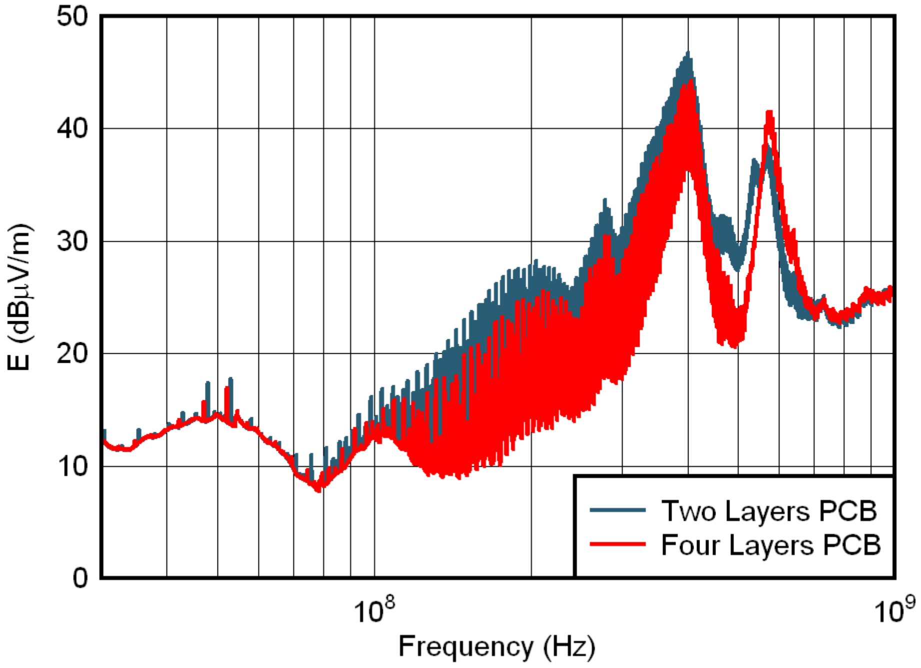


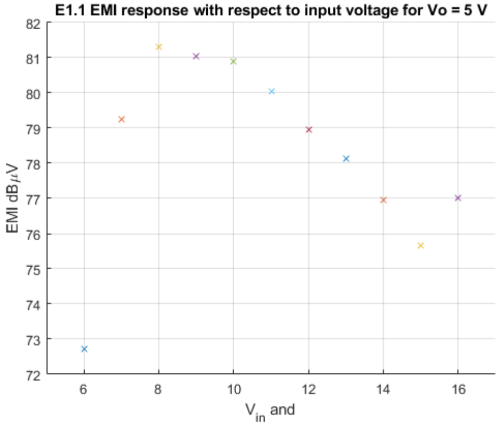


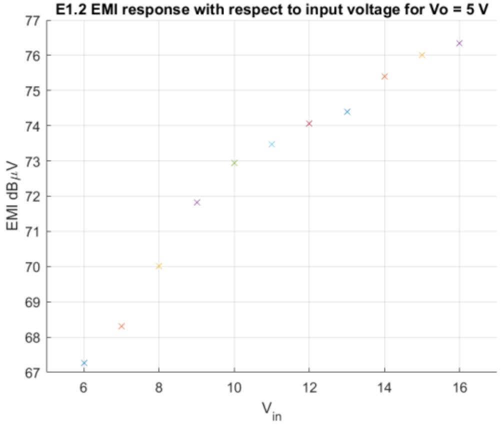
Good layout 2 Layer vs. 4 Layer



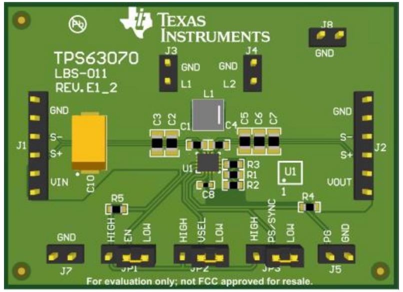


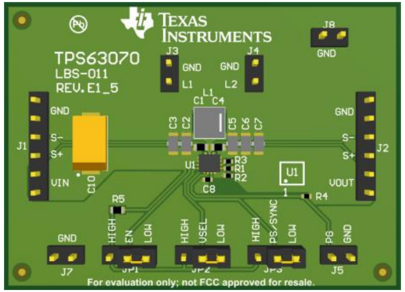


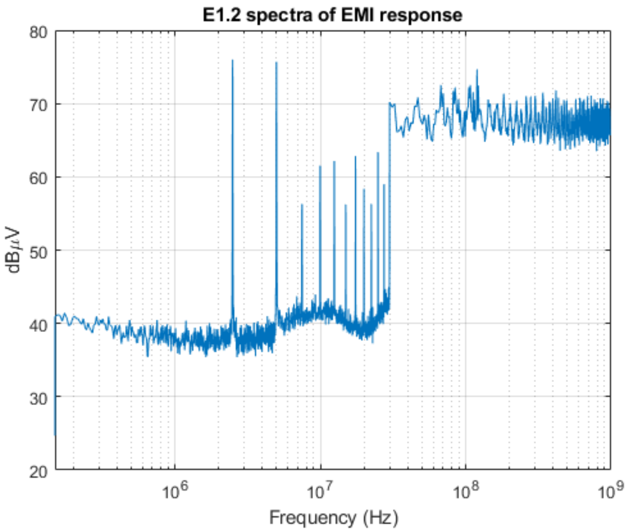


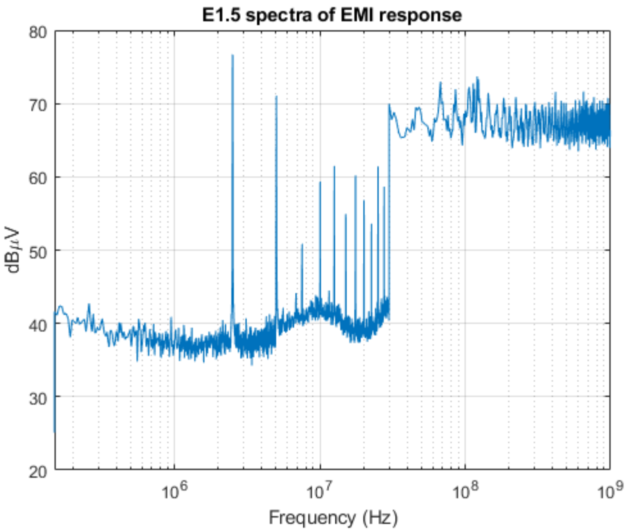


Good Layout compared to Minimum Size

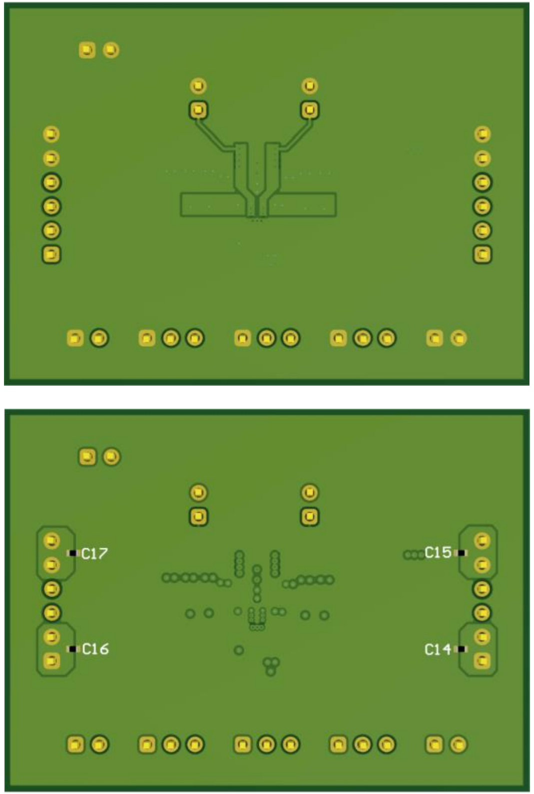


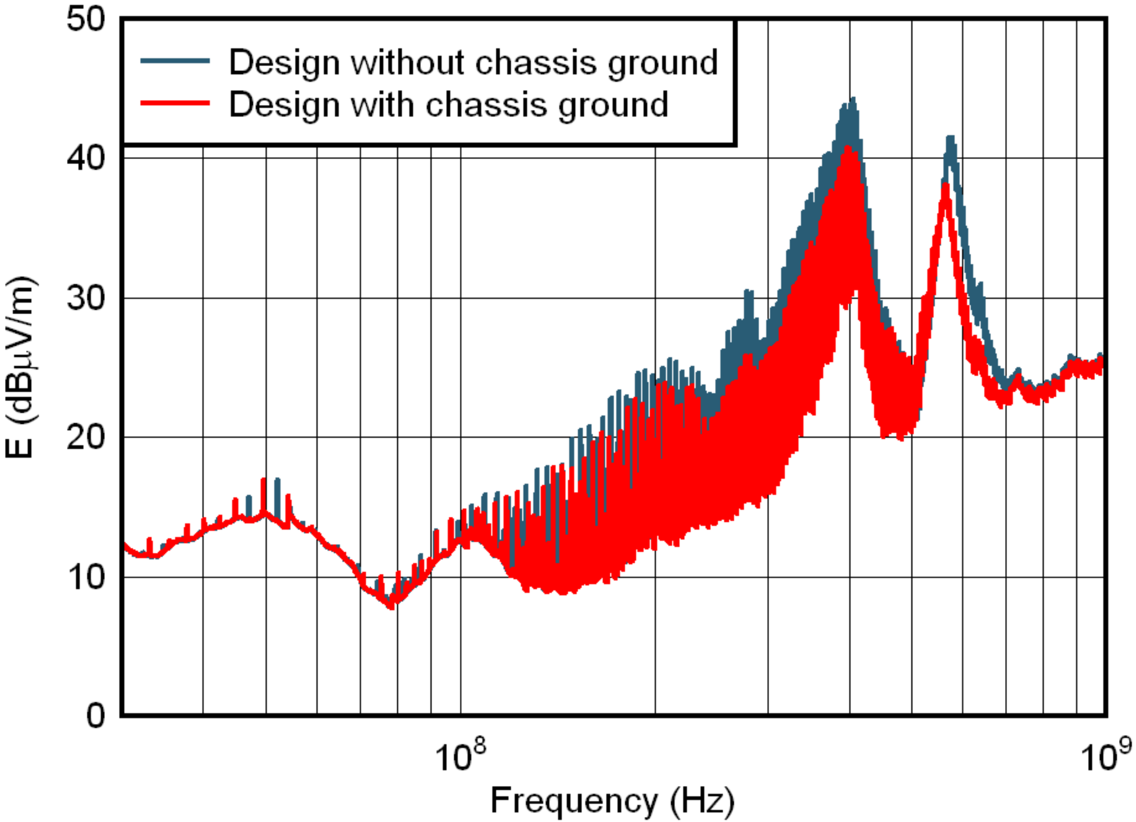






Good layout without and with Chassis GND





Buck-Boost Tools and Links

- EMI
  - Layer Design for Reducing Radiated EMI of DC to DC Buck-Boost Converters
  - Layout Tips for EMI Reduction in DC/ DC Converters
- Buck-boost Converter Technical Content Summary
  - A Topical Index of TI Low-Power Buck-Boost Converter Application Notes
- Hardware Development Kit
  - TPS63802HDKEVM

- Standard operation
- Backup power supply
- High-side LED driver
- High-side LED driver with dimming option
- Input current limit
- Extended soft start or limit inrush current limitation
- Digital voltage scaling
- Output voltage tracking
- Bypass mode
- Precise enable and start-up delay

TEXAS INSTRUMENTS