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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Data Transmission
- Amplifiers

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI's product-specific websites listed at the end of each article.

A methodology of interfacing serial A-to-D converters to DSPs

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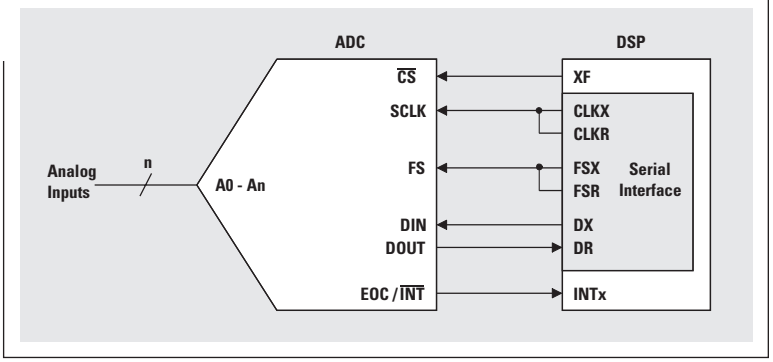
Application Manager

Introduction

Designers of DSP systems often have to rewrite their interface software when a desired increase in system performance requires the replacement of the current A-to-D converter with a device of higher speed or resolution. This article describes a method for interfacing various types of serial ADCs to the standard serial port of a DSP (TMS320C50) while keeping the software modifications at a minimum. It concludes with the introduction of "C-callable assembler routines" provided by TI's application staff that relieve the experienced C-programmer from performing tedious assembler studies.

Figure 1. Typical serial interface between an ADC and a DSP



Serial analog-to-digital converters

Table 1 lists a range of serial ADCs that interface directly to DSPs without additional control logic. All these devices have the following in common:

- the conversion is performed by successive approximation based on charge redistribution,
- a conversion is initiated by an external trigger signal, and
- the data format for the transfer between DSP and ADC is 16 bits.

For purposes of describing interface timing the devices in Table 1 are grouped in two categories:

- on-the-fly converters that perform a conversion while exchanging data with the host, and
- sequential converters that execute a conversion following a data transfer.

Figure 1 shows a typical interface between a DSP and a serial ADC. The DSP general-purpose I/O XF signal activates the ADC. The control and data signals of the DSP serial port manage the transfer of data. The additional EOC/INT output, only available on sequentially converting ADCs, signals the end of a conversion to the DSP, indicating that a new transfer can begin.

Before the timing sequence of a data transfer is discussed, the reader should understand the internal operation of the standard serial interface.

Standard serial interface

TI provides a variety of DSPs with different types of serial interfaces including:

- buffered serial port (BSP) with auto-buffering unit module (AMU),
- buffered serial interfaces with internal FIFO, and
- time-division-multiplex (TDM) serial interfaces, particularly useful for telecom applications.

The standard serial interface is the focus of this discussion because it is used far more often than the BSP or the TDM serial port. The serial port interfaces to data converters via the following six control lines:

CLKX *Transmit clock input or output.* This signal clocks data from the transmit shift register (XSR) to the DX pin. The serial port can be configured for internal clock generation or to accept an external clock. If the port is configured to generate the

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Table 1. Family of serial A-to-D converters

DEVICE	CONVERSION	SUPPLY (V)	RESOLUTION (bits)	INPUT CHANNEL	CONVERSION RATE (MSPS)	POWER DOWN	SWEEP MODE	FIFO
TLV1570	On-the-fly	2.7 – 5.5	10	1	1.25	Auto	–	–
TLV1572	On-the-fly	2.7 – 5.5	10	8	1.25	Auto	✔	–
TLV1544	Sequential	2.7 – 5.5	10	4	0.1	Prog.	✔	–
TLV1548	Sequential	2.7 – 5.5	10	8	0.1	Prog.	✔	–
TLV2544	Sequential	2.7 – 5.5	12	4	0.2	Prog.	✔	✔
TLV2548	Sequential	2.7 – 5.5	12	8	0.2	Prog.	✔	✔
TLC2554	Sequential	5.0	12	4	0.4	Prog.	✔	✔
TLC2558	Sequential	5.0	12	8	0.4	Prog.	✔	✔

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data clock on-chip, CLKX becomes an output, providing the data clock for the serial interface. If the port is configured to accept an external clock, CLKX changes to an input, receiving the external clock signal.

FSX *Transmit frame synchronization input or output.* FSX indicates the start of a transmission. The serial port can be configured for internal frame-sync generation or to accept an external frame-sync signal. If the port is configured to generate the frame sync pulse on-chip, FSX becomes an output. If the port is configured to accept an external frame sync pulse, this pin becomes an input.

DX *Serial data transmit.* DX transmits the actual data from the transmit shift register (XSR).

CLKR *Receive clock input.* CLKR always receives an external clock for clocking the data from the DR pin into the receive shift register (RSR).

FSR *Receive frame synchronization input.* FSR always receives an external frame sync pulse to initiate the reception of data at the beginning of a frame.

DR *Serial data receive.* DR receives the actual data which are clocked into the receive shift register (RSR).

Figure 2 shows the block diagram of the standard serial interface. The operation of the serial port is supported by the following five 16-bit registers:

DXR *Data transmit register.* Transmit data are written by the CPU into this register and then copied into the XSR. The DXR provides double buffering function by allowing the CPU to update its content via a new write-cycle, while the previous data transmit out of XSR is still ongoing.

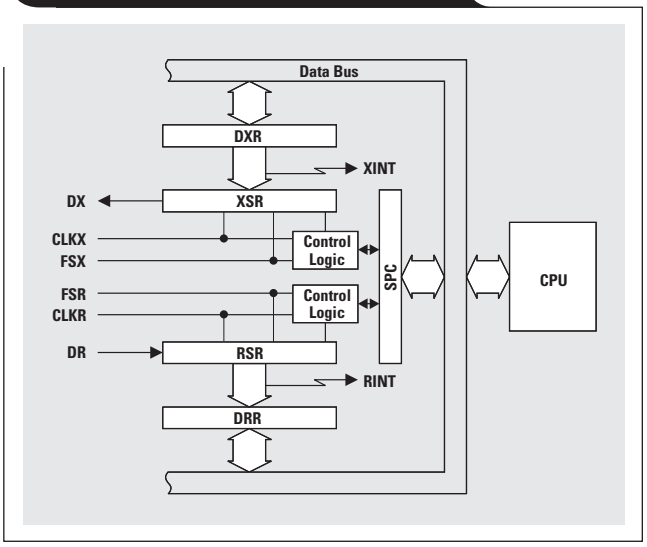
XSR *Transmit shift register.* Transmit data are copied from the DXR into the XSR and sent to the data converter.

RSR *Receive shift register.* Receive data from the data converter are clocked into this register and then copied to the DRR.

DRR *Data receive register.* Receive data, copied from the RSR, are read by the CPU from this register. The DRR provides double buffering function by allowing the CPU to read its content, while the next data reception into RSR has already started.

SPC *Serial port control register.* The SPC contains control bits, which are set by the CPU to configure the operation of the serial port.

Figure 2. Standard serial interface block diagram



Serial port general operation

In the transmit direction the CPU initiates a data transfer by writing transmit data to the DXR. Then the data are copied from the DXR into the XSR and clocked out to the DX output. Upon the completion of a DXR-to-XSR copy, a transmit interrupt, XINT, is generated. This interrupt signals the CPU that new data can be written into the DXR.

In the receive direction the incoming data are clocked into RSR and then copied into DRR. Upon the completion of the data copy, a receive interrupt, RINT, is generated. This interrupt signals the CPU that new data are available in DRR. The CPU needs to read these data, while the next receive frame is clocked into the RSR.

Serial port configuration

Before a data transfer can be executed, the serial port needs to be configured via the serial port control register, SPC. Figure 3 shows the 16-bit memory-mapped SPC of the TMS320C50DSP (R = read-only bits, R/W = read/write bits).

Out of the 16 bits of the SPC, only six R/W bits (shaded bits in Figure 3) are used to configure the serial port. The remaining non-shaded R/W bits, such as the emulation bits FREE and SOFT, and the digital loop back bit, DLB, are set to zero (FREE = SOFT = DLB = 0).

Figure 3. Serial port control register

FREE	SOFT	RSRFULL	/XSREMPTY	XRDY	RRDY	IN1	IN0	RRST	XRST	TXM	MCM	FSM	FO	DLB	RES
R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Table 2 explains the functions of the six bits that configure the serial port.

The following example shows a typical serial port configuration when interfacing to a serial A-to-D converter from Texas Instruments.

- For standard serial port operation, all non-shaded R/W bits are set to zero *(Free = Soft = DLB = 0)*.
- During the SPC configuration the serial port transmitter and receiver need to be disabled by setting the respective reset bits to zero *(/XRST = /RRST = 0)*.
- Assuming that no external clock and frame sync generator are used, both signals need to be generated on-chip, thus requiring that TXM and MCM be set to one *(TXM = MCM = 1)*.
- To comply with the 16-bit data format of the A-to-D converter, FO is set to zero *(FO = 0)*.
- As mentioned previously, all serial ADCs require a trigger signal for each data transfer plus subsequent conversion. As will be shown in the following section, this trigger signal is already available through the FS-pulse of the serial port. For this purpose the serial port needs to be configured for burst mode operation by setting FSM to one *(FSM = 1)*.

Table 2. Important SPC bits for an ADC/DSP interface

NAME	FUNCTION
/XRST/RRST	The Transmit and Receive reset signals activate and deactivate the transmitter and receiver of the serial port. /XRST, / RRST = 1, transmitter and receiver are active /XRST, / RRST = 0, activity halts
TXM	The Transmit Mode bit specifies the source for FSX-pulse generation. TXM = 1, FSX is generated on-chip and synchronized to CLKX TXM = 0, FSX needs to be applied from external source
MCM	The Clock Mode bit specifies the clock source for CLKX. MCM = 1, on-chip clock source is used MCM = 0, external clock source is chosen
FSM	The Frame Synch Mode bit specifies when a frame sync pulse is needed. FSM = 1, Burst Mode is selected (an FS-pulse is used for each word) FSM = 0, Continuous Mode is selected (only one start pulse is required)
FO	The Format bit specifies the word length of the transmitter and receiver. FO = 0, word length is 16-bit FO = 1, word length is 8-bit

Figure 4 shows the resulting binary pattern with the corresponding hex code that is loaded into the SPC.

The assembler instruction << *SPLK #0038h , SPC* >> commands the CPU to write the content 38h into the serial control register, SPC. The CPU then activates the serial port via a second instruction << *SPLK #00F8h , SPC* >> by setting the /XRST and /RRST bit to one.

Transmit and receive operations in burst mode

The serial port can be programmed for continuous mode or burst mode operation. Both modes indicate the beginning of a data frame via a frame-sync pulse at FS. In continuous mode, only one FS-pulse is needed to indicate the beginning of a number of consecutive data frames. In burst mode, an FS-pulse indicates the start of one data frame (16 SCLK cycles) only, thereby providing the required trigger signal for an A-to-D conversion. Therefore, the serial port needs to operate in burst mode. Figure 5 shows the interface timing of the serial port in burst mode operation.

The data clock has the two designators CLKX and CLKR because the clock signal of the serial port transmitter is identical to the one of the serial port receiver. Figure 1 shows that when the serial port is configured for on-chip clock generation (MCM = 1), CLKX is not only connected to the clock input of the ADC but also fed back into the data clock input of the serial port receiver. The same is valid for the frame-sync signals, FSX and FSR.

A data transfer is initiated by the CPU writing transmit data (i.e., ADC configuration data) into the data transmit register, DXR. With the second rising edge of CLKX, the content of DXR is copied into the transmit shift register, XSR. At this time, a frame-sync pulse and a transmit interrupt, XINT, are generated. With the first rising edge of CLKX after FSX has gone low, transmit data are shifted out to the DX-pin while receive data are clocked into the receive shift register, RSR, via the DR-pin. Both data streams, in transmit and receive, start with the most significant bit, MSB. While data change with the rising edge of CLKX, the falling edge of CLKX latches the transmit data into the ADC and the receive data into RSR. With the 16th falling edge of CLKX (after FSX has gone low), the receive shift register, RSR, is full. The content of RSR is copied into the data receive register, DRR, and a receive interrupt, RINT, is generated. The falling edge of the 16th CLKX cycle completes an entire data transfer, both in receive and transmit. Any further data transfer needs to be initiated with a CPU reload of DXR.

The serial port interrupts, XINT and RINT (shaded gray in Figures 5 and 6), represent internal signals, which are available to the CPU only. If either one of these interrupts

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Figure 4. Serial port configuration code

FREE	SOFT	RSRFULL	/XSREMPTY	XRDY	RRDY	IN1	IN0	RRST	XRST	TXM	MCM	FSM	FO	DLB	RES	
0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	Bin
0				0				3				8				Hex

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Figure 5. Transmit and receive operation in burst mode

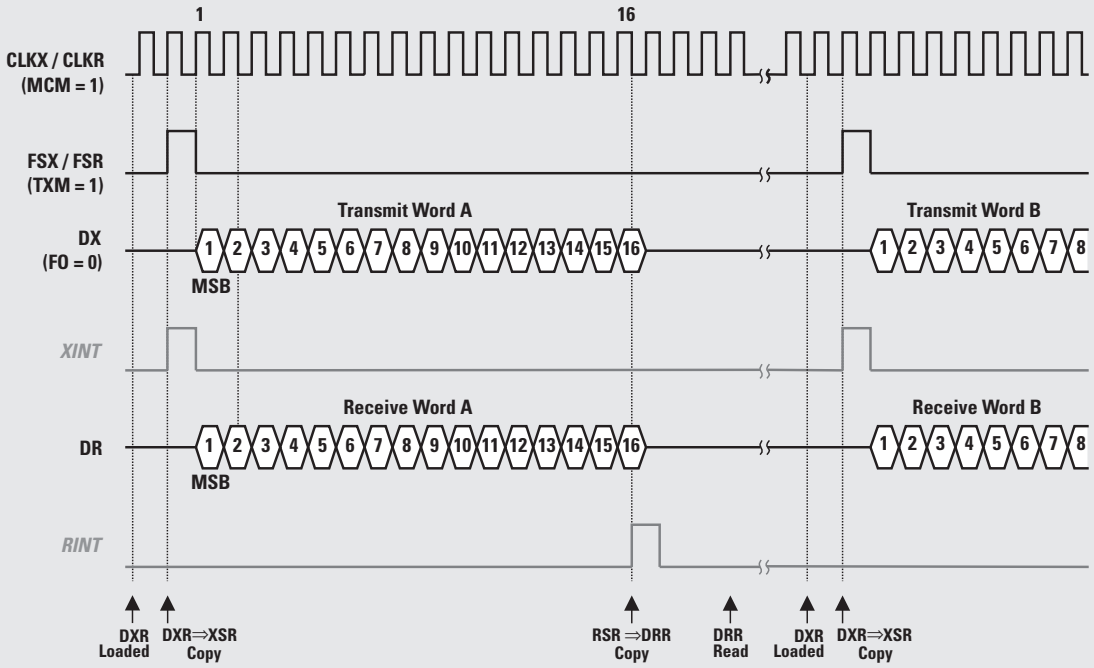
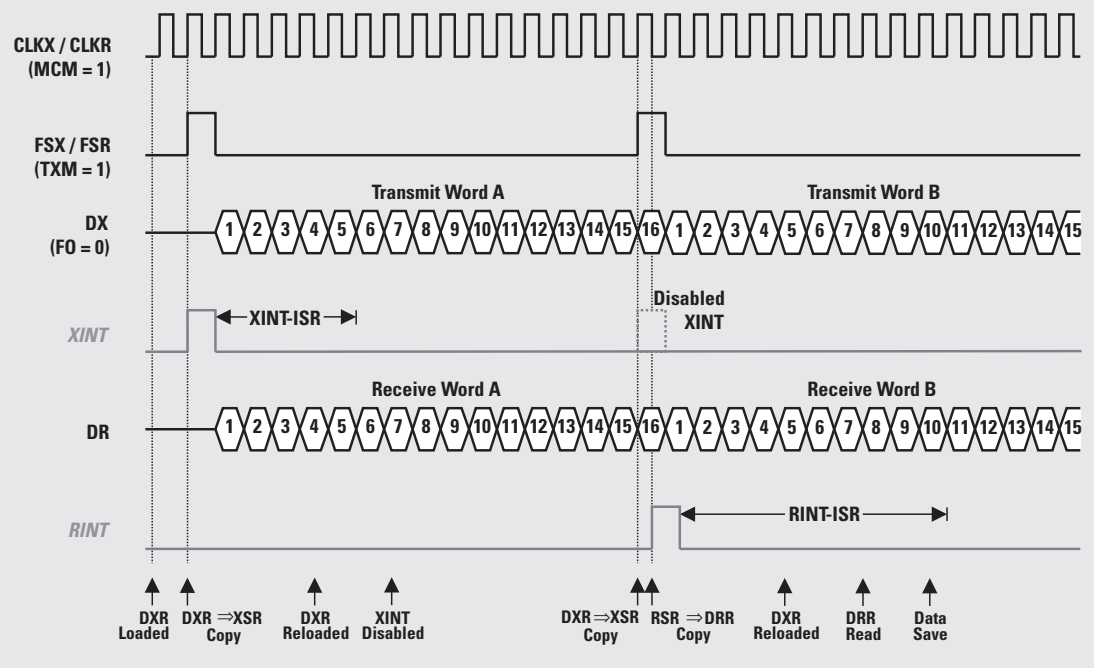


Figure 6. Burst mode operation at maximum packet frequency



occurs, the program execution is directed to a transmit interrupt service routine, XINT-ISR, or a receive interrupt service routine, RINT-ISR. Within those ISRs, the CPU can execute serial port supporting tasks while a data transfer over the serial interface is still in progress.

For example, an XINT-ISR is often used to reload DXR after the old DXR content is copied into XSR. This ensures that the next DXR-to-XSR copy happens as soon as XSR is empty and a second data transmit can follow immediately. However, as will be shown in the next secton, when interfacing to sequentially operating ADCs, XINT needs to be disabled. A RINT-ISR is used to read the data receive register, DRR, and to save the content into data memory. When interfacing to on-the-fly converters, the RINT-ISR can also include the initiation of the next data transfer to maximize the data throughput.

A specific case of the burst mode is the operation at maximum packet frequency, shown in Figure 6.

At maximum packet frequency, the data bits in consecutive packets are transmitted contiguously with no inactivity between bits. This is achieved by reloading DXR during the first XINT-ISR. A second instruction disables XINT for all further data frames. A XINT-ISR executing these two instructions takes approximately five CLKX cycles to complete. With the rising edge of the 16th CLKX cycle, the last transmit bit is shifted out of XSR, and the latest DXR content is copied into XSR. At this time a new frame sync pulse, which overlaps the last transmit bit of the previous frame, is generated to start a new data transfer.

With the 16th falling edge of CLKX, half a clock cycle later, the last receive bit is clocked into the RSR. The subsequent RSR-to-DRR copy generates a receive interrupt. During the following RINT-ISR, the CPU reloads the transmit data register, DXR. It then reads the receive data register, DRR, and saves its content into data memory. While the CPU is executing the RINT-ISR, the serial port continues to transfer data. From now on, only one interrupt service routine, the RINT-ISR, is used to save the receive data into memory, as well as to initiate all further data transfers. Care must be taken when adding further instructions to the RINT-ISR. Since the data stream needs to be contiguous, the length of the ISR must not exceed 15 CLKX cycles.

Interfacing to sequential ADCs

The sequential A-to-D converters in Table 1 operate in two phases. In phase 1, the ADC simultaneously receives configuration data from the DSP and transmits conversion results to the DSP. During this data transfer, the ADC is configured for the desired operation mode and starts sampling the analog input channel. Phase 2 represents the actual analog-to-digital conversion, followed by an interrupt signal once a conversion is complete. The advantage of the sequential operation is that the sampling period can be extended by a factor of 2 without affecting the conversion time. This is particularly useful for sampling high-impedance input sources. A long sampling time allows the ADC internal switched capacitors to be charged longer, thus helping the analog input signal sampled to settle within a 0.5-LSB accuracy.

Figure 7 shows the timing diagram of the TLV2544 ADC in single-shot mode. Because a conversion needs to be completed before another one can be started, a contiguous flow of data bits is not possible, which is true for all sequentially operating ADCs.

Note that most ADCs provide a programmable EOC/INT pin to signal the end of a conversion. The following discussion assumes that the EOC/INT pin is programmed to use the /INT pulse to indicate the end of a conversion. The two gray-shaded signals, EOC and RINT, serve demonstration purposes only.

EOC presents the internal conversion time of the A-to-D converter, while RINT demonstrates the occurrence of the DSP internal receive interrupt.

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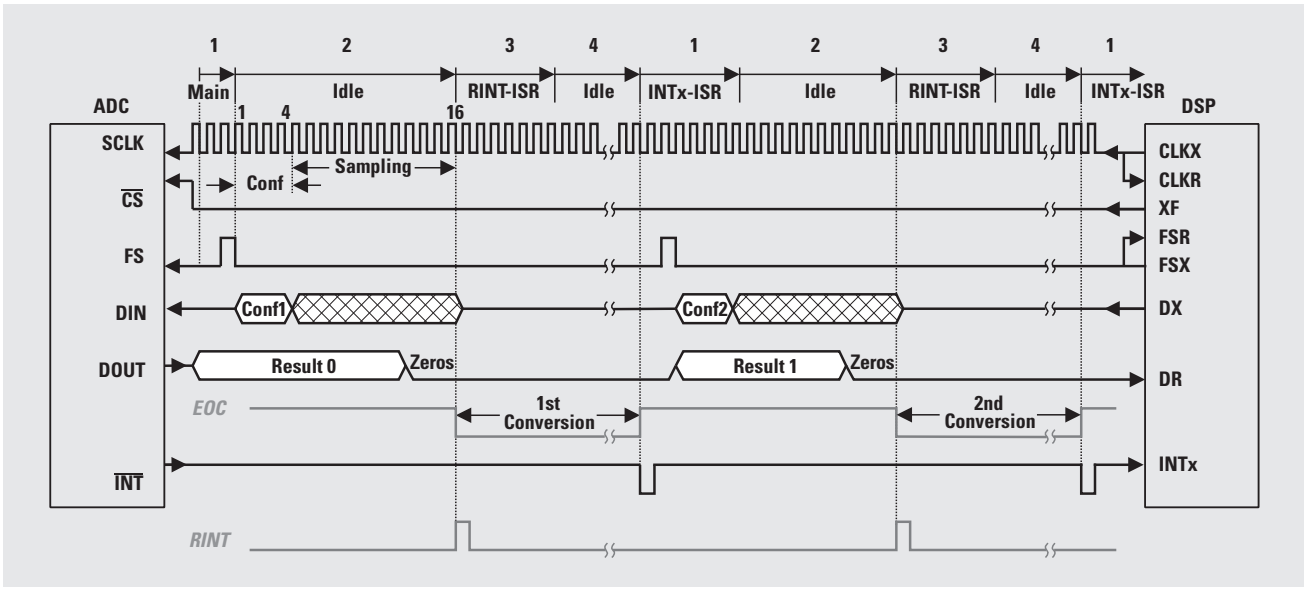
Figure 7. ADC/DSP interface timing for a sequential ADC



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The data acquisition process starts with the DSP providing the data clock, SCLK, for the serial interface. The DSP then activates the ADC by applying a logic low via the external flag output, XF, to the /CS input of the A-to-D converter. With the falling edge of /CS, the data output of the ADC leaves the high-impedance state and provides a random logic value at DOUT.

After the ADC is enabled, each data transfer is executed by the following five steps:

1. In the main routine, the DSP initiates a data transfer by writing ADC configuration data into the DXR of the serial port. On the second rising edge of SCLK following the DXR-write, a frame sync pulse, FS, is generated.
2. With the falling edge of FS, the serial port transmits configuration data to the ADC via DIN. The first four bits represent the actual configuration data, while the remaining 12 bits are ignored by the ADC. Simultaneously the ADC transmits the conversion results via DOUT to the DSP. To comply to the 16-bit frame format, the results of a 10-bit converter is followed by six zero bits. A 12-bit conversion result requires only four trailing zeros.
3. With the 16th falling edge of SCLK, the DX output, and with it DIN, goes into high-impedance, while DOUT stays low till the next data transfer. The A-to-D converter starts the conversion process and the generated receive interrupt of the serial port leads the CPU to enter the RINT-ISR. During this interrupt routine, the CPU reads the receive data from the serial port and saves it into data memory.
4. Upon the completion of the RINT-ISR the CPU idles until an unmasked interrupt occurs. The ADC completes the conversion and provides an interrupt pulse via its /INT output to one of the DSP external interrupt inputs, /INT1 – /INT3.
5. The CPU now enters the INTx-ISR, reloading the DXR with ADC configuration data (i.e., the channel number). The new DXR-write initiates the next data transfer sequence, and Steps 1–4 are repeated until all samples have been acquired.

Figure 8 shows the basic program flow that supports the above interface timing.

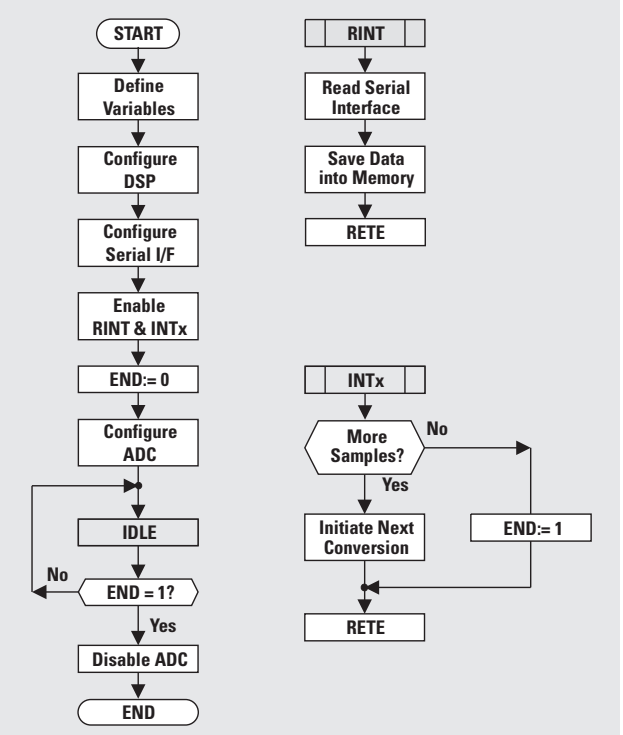
Interfacing to "on-the-fly" ADCs

These converters perform the analog-to-digital conversion at the same time they transfer data to the DSP. A data acquisition, including device configuration and data conversion, is completed within the 16 data clock cycles, thus allowing the stream of data bits to be contiguous. On-the-fly converters usually provide a sample rate of 1–4 MSPS. Figure 9 shows the timing diagram of the multi-channel, on-the-fly A-to-D converter, TLV1570.

After the DSP has activated the ADC by taking /CS low, the data transfer is executed by the following three steps:

1. In the main routine, the DSP writes ADC configuration data into the DXR of the serial port and generates an FS-pulse as well as a transmit interrupt, XINT. The serial port executes the first transfer of data by sending a

Figure 8. Interface program for sequential ADCs



Main routine

The main routine starts with defining the following variables:

- the number of samples to be acquired,
- the memory start address for the acquired data, and
- the ADC configuration words such as the conversion mode, the sampling mode, and the channel numbers.

The DSP configuration disables all interrupts, specifies the wait-states to zero, and defines the program memory range for the data acquisition program. Then the serial port is configured for burst mode operation and on-chip data clock and frame-sync generation.

The two interrupts, RINT and INTx, are enabled, and the END-flag, which determines the end of the data acquisition program, is set to zero.

To configure the A-to-D converter, the DSP takes the XF-output low and enables the ADC via the /CS- input. The CPU loads the DXR with ADC configuration data, causing the first data transfer to start. Then the CPU is set into idle mode, waiting for interrupts to occur.

Once an ISR has been completed, the CPU checks for program completion. As long as the END-flag is zero, the CPU returns to idle mode. If the END-flag is one, the DSP disables the ADC by taking XF high, thus completing the main routine.

RINT-ISR

During the RINT-ISR the CPU reads the receive data in the serial port, saves the data into memory, and returns to the main routine.

INTx-ISR

The INT-ISR initiates all further data transfers. As long as more samples are to be acquired, the CPU continuously reloads the DXR to start a new conversion.

Once all samples have been acquired, the END-flag is set to one and program control returns to the main routine.

16-bit configuration word to the ADC. In receive, the ADC provides 16-bit output data, consisting of four preceding zeros and a 12-bit conversion result. Meanwhile the XINT-ISR reloads DXR and disables XINT for all further data frames.

2. While the data transfer continues, the CPU idles, waiting for a receive interrupt to occur.
3. With the rising edge of the 16th SCLK cycle, a new FS-pulse starts the next data frame. Upon the falling edge of the 16th SCLK cycle, a RINT is generated that forces the CPU to leave the idle mode and enter the receive interrupt service routine. Within the RINT-ISR, the CPU reads the DRR and saves the received data into memory. It then writes a new configuration word into DXR to prepare for the next data frame. After completing the RINT-ISR, the CPU returns to idle mode. Then Steps 2 and 3 are repeated until all samples have been acquired.

Figure 10 shows the timing diagram of the 12-bit, single-channel ADC, TLV1572. The interface timing is similar to that of the TLV1570, except that the output data of the

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Figure 9. ADC/DSP interface timing for a multi-channel on-the-fly ADC

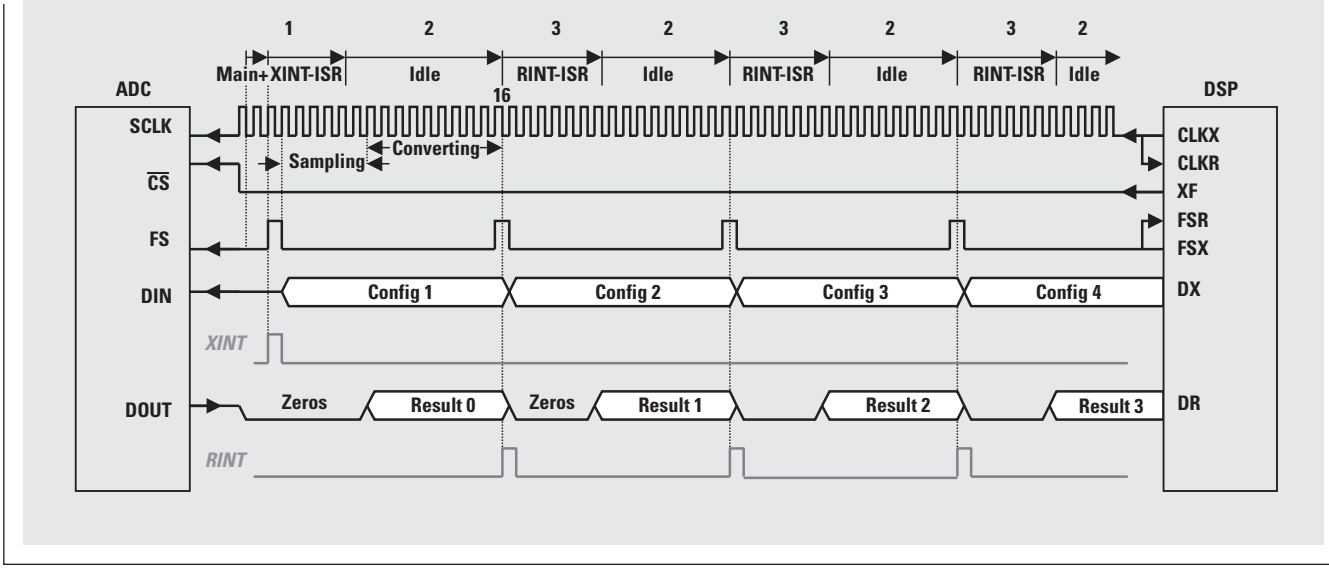
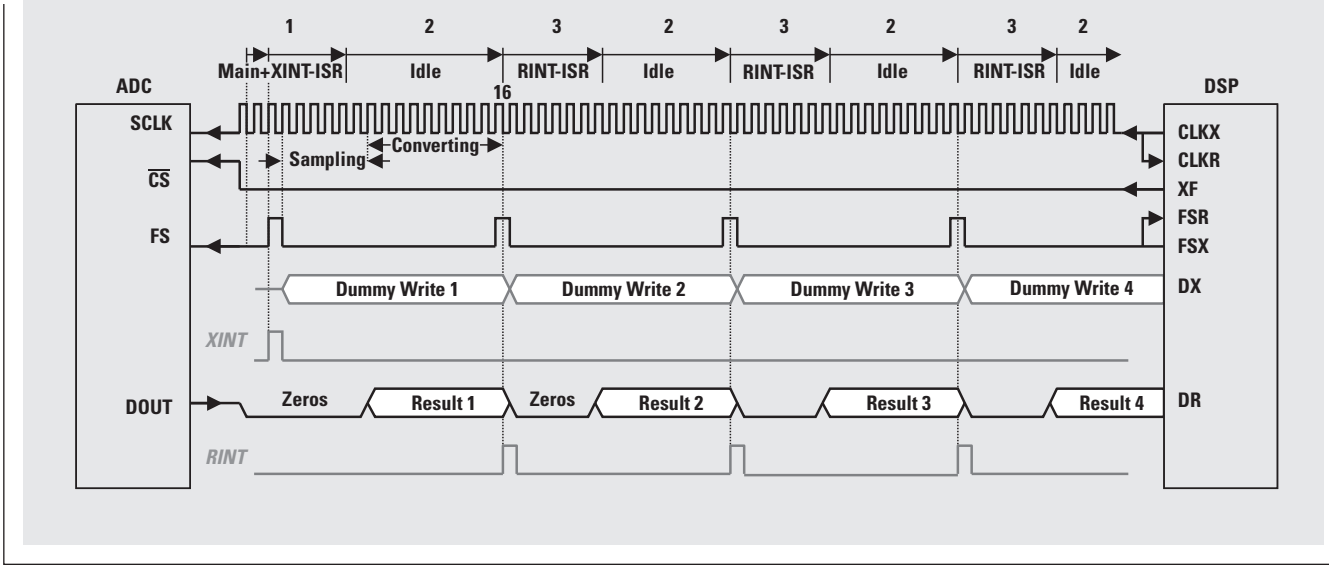


Figure 10. ADC/DSP interface timing for a single-channel, on-the-fly ADC



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TLV1572 represent the results of the current conversion, while the output data of the TLV1570 are the results of the conversion executed in the previous data frame.

The TLV1572 is not configurable and therefore provides no DIN terminal. The DSP still needs to perform a dummy write of the DXR (i.e., with random data) to generate the required FS-pulse, which indicates the start of a data frame and triggers the A-to-D conversion.

Figure 11 shows the basic program flow that supports the above interface timing.

C-callable interface routines

The previous flowcharts describe the structure of the interface routines written in assembler. These assembler routines are used to investigate and to optimize the interface timing between newly released data converters and DSPs. However, with the majority of DSP programmers using C rather than assembler, TI's application team for analog products has made its assembler routines C-callable.

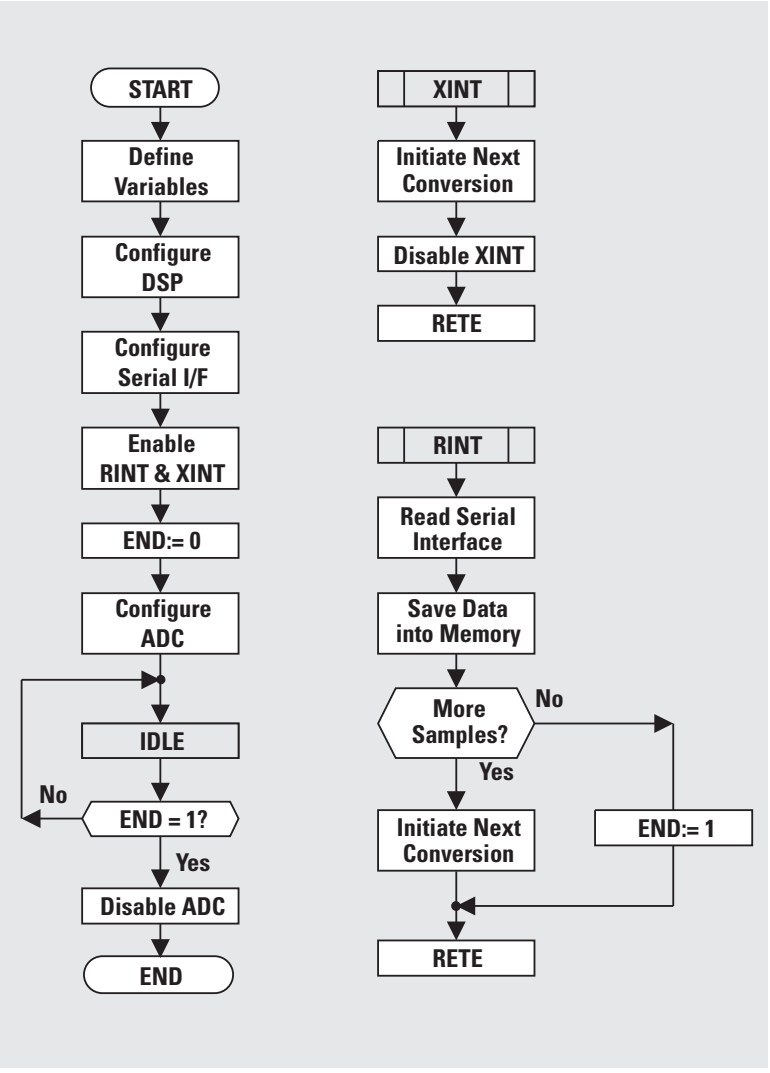
Figure 12 gives an example of a C-callable assembler routine for the 8-channel, 12-bit ADC, TLV2548.

In addition, the assembler routine received a save-context and a restore-context task.

- Save-context saves all pointers and registers, such as frame-pointer, stack-pointer, status and auxiliary registers, which have been used previously in the C-program.
- Restore-context restores the original content of these registers before returning to the C-program.

After the variable definition in C, a call instruction starts the assembler routine. All previously used registers are saved, and the actual data acquisition begins. Once the user-defined number of samples has been received, all pointers and registers are restored. The CPU exits the assembler routine and returns to the C-program. Using C-callable interface relieves the programmer from the tedious task of studying device-specific assembler code.

Figure 11. Interface program for on-the-fly ADCs



Main routine

The main routine is almost the same as the one in Figure 8, except that the internal transmit interrupt, XINT, is used instead of the external interrupt, INTx.

The main routine starts with defining the number of samples to be acquired, the memory start address for the acquired data, and the ADC configuration words. In the case of a non-configurable device, there are no configuration words. Instead, any random code can be written to DXR to start a data transfer.

The main routine continues with configuring the DSP and the serial port.

Then the two serial port interrupts, RINT and XINT, are enabled, and the END-flag is set to zero.

To configure the ADC, the DSP takes the XF-output low and enables the device via the /CS- input. The CPU writes configuration data to DXR. The following data transfer configures the ADC, while the CPU goes into idle mode, waiting for interrupts to occur.

Once an ISR has been completed, the CPU checks for program completion. Depending on the status of END, the CPU either returns to idle mode or disables the ADC and completes the main routine.

XINT-ISR

With the start of the first data frame, a XINT is generated. The CPU enters the XINT-ISR and reloads DXR to ensure an immediate start of the second frame, once the first transfer is completed and XSR is empty.

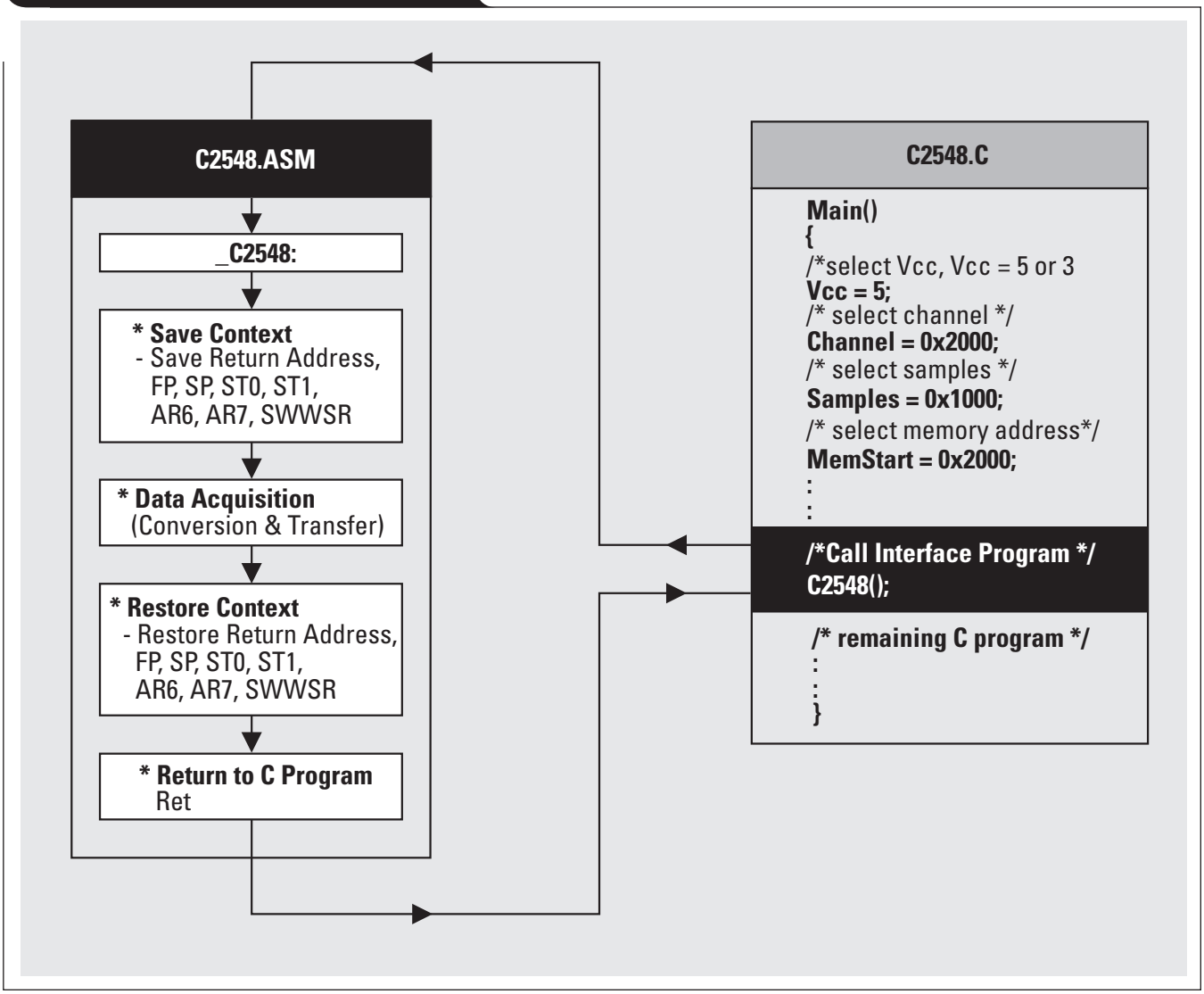
Then the CPU disables XINT for all further transfers.

RINT-ISR

This RINT-ISR is the sum of the previous RINT- and INTx-ISRs for sequential converters. The CPU reads the receive data and saves it into memory.

As long as more samples are to be acquired, the CPU continuously reloads the DXR to start a new conversion. Once all samples have been acquired, the END-flag is set to one and program control returns to the main routine.

Figure 12. C-callable interface program



References

For more information related to this article, visit the TI Web site at www.ti.com/ and look for the following materials by entering the TI literature number into the quick-search box.

Document Title	TI Lit. #
1. Analog Applications (August 1999)	SLYT005
2. Characteristics, Operation, and Use of the TLV157XEVM	SLAU025
3. Interfacing the TLV1572 ADC to the TMS320C203 DSP	SLAA026B
4. TLV1570 EVM User's Guide	SLAU024
5. TLV1572 EVM User's Guide	SLAU018
6. Choosing an ADC and Op Amp for Minimum Offset	SLAA064
7. Interfacing the TLV1544 ADC to the TMS320C203 DSP	SLAA028A
8. Interfacing the TLV1544 ADC to the TMS320C50 DSP	SLAA025A
9. Switched-capacitor ADC Analog Input Calculations	SLAA036

Related Web sites

Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device*.html

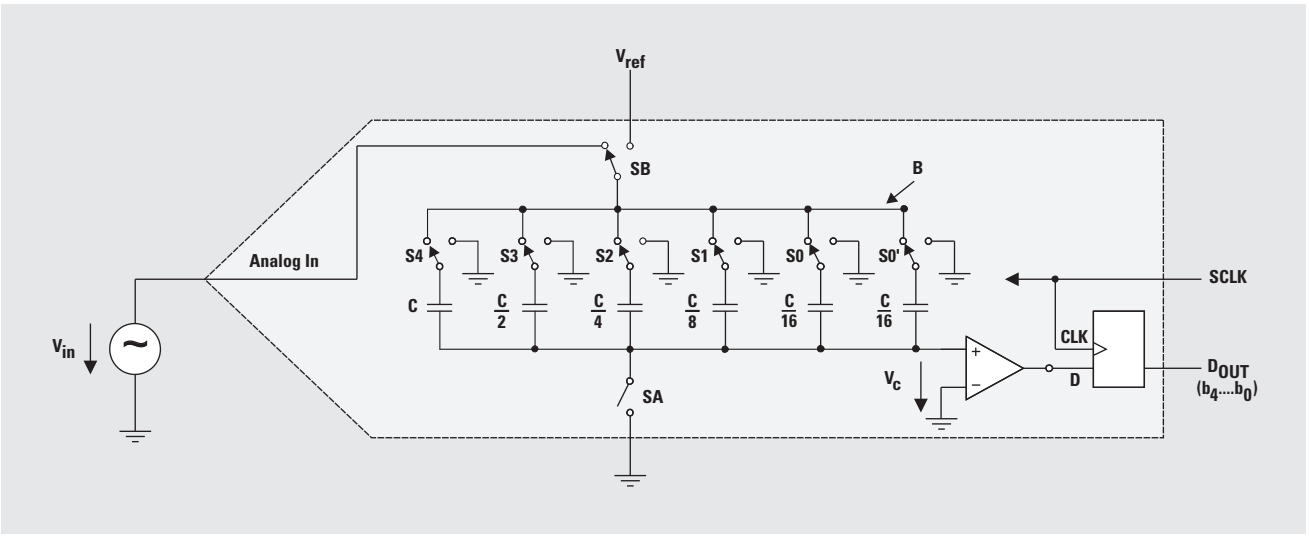
Replace *device* with tlc2554, tlc2558, tlv1544, tlv1548, tlv1570, tlv1572, tlv2544, or tlv2548

www.ti.com/sc/docs/products/dsp/tms320c50.html

The operation of the SAR-ADC based on charge redistribution

By Thomas Kugelstadt
Application Manager

Figure 1. Five-bit SAR-ADC based on charge redistribution



All Texas Instruments TLV- and TLC-series sequential serial analog-to-digital converters perform successive approximation based on charge redistribution. This article explains the operation of the SAR (successive approximation register)-ADC (analog-to-digital converter). It provides a concise description of a model SAR-ADC based on charge redistribution. Figure 1 shows the simplified circuit of a 5-bit charge redistribution converter using switched capacitor architecture.

All capacitors have binary weighted values, i.e., C, C/2, C/4,….C/2^{n-1}. The last two capacitors having the value C/2^{n-1} are connected so that the total capacitance of the n+1 capacitors is 2C. MOS-transistors are used to implement the required n+3 switches, and the voltage comparator provides the appropriate steering of the switches via auxiliary logic circuitry. The conversion process is performed in three steps: the sample mode, the hold mode, and the redistribution mode (in which the actual conversion is performed).

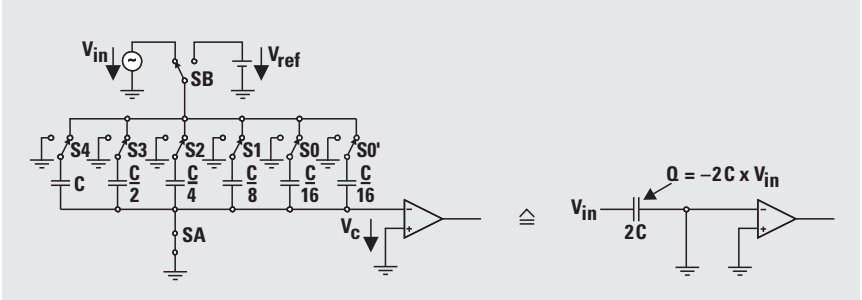
Sample mode

In the sampling mode (Figure 2), switch SA is closed and SB is switched to the input voltage V_{in}. The remaining switches are turned to the common bus B. Due to charging, a total charge of $Q_{in} = -2C \times V_{in}$ is stored on the lower plates of the capacitors.

Hold mode

During the hold mode (Figure 3), switch SA is opened while the switches S4….S0′ are connected to ground,

Figure 2. Sample mode



thereby applying a voltage of $V_c = -V_{in}$ to the comparator input. This means that the circuit already has a built-in sample-and-hold element.

Redistribution mode

The actual conversion is performed by the redistribution mode. The first conversion step, shown in Figure 4, connects C (the largest capacitor) via switch S4 to the reference voltage V_{ref}, which corresponds to the full-scale range (FSR) of the ADC.

Capacitor C forms a 1:1 capacitance divider with the remaining capacitors connected to ground. The comparator input voltage becomes $V_c = -V_{in} + V_{ref}/2$. If $V_{in} > V_{ref}/2$, then $V_c < 0$, and the comparator output goes high, providing the most significant bit MSB (bit 4) = 1. On the other hand, if $V_{in} < V_{ref}/2$, then $V_c > 0$, and bit 4 = 0.

The second conversion step connects C/2 to V_{ref}. If the first conversion step resulted in bit 4 = 1, switch S4 is turned to ground again to discharge C as shown in Figure 5; otherwise it remains connected to V_{ref} if bit 4 = 0 (Figure 6), resulting in a comparator input voltage $V_c = V_{in}$ + bit 4 – $V_{ref}/2$ + $V_{ref}/4$.

According to this voltage, the next most significant bit (bit 3) is obtained by comparing V_{in} to 1/4 V_{ref} or 3/4 V_{ref} through the different voltage dividers. Switch S3 is then either turned to ground if bit 3 = 1, thereby discharging C/2, or S3 remains connected to V_{ref} if bit 3 = 0.

This process continues until all bits are generated, with the final conversion step being performed at a comparator input voltage of $V_c = -V_{in}$ + bit 4 x $V_{ref}/2$ + bit 3 x $V_{ref}/4$ + bit 2 x $V_{ref}/8$ + bit 1 x $V_{ref}/16$ + bit 0 x $V_{ref}/32$.

Related Web site

www.ti.com/sc/docs/products/msp/dataconv/index.htm

Figure 3. Hold mode

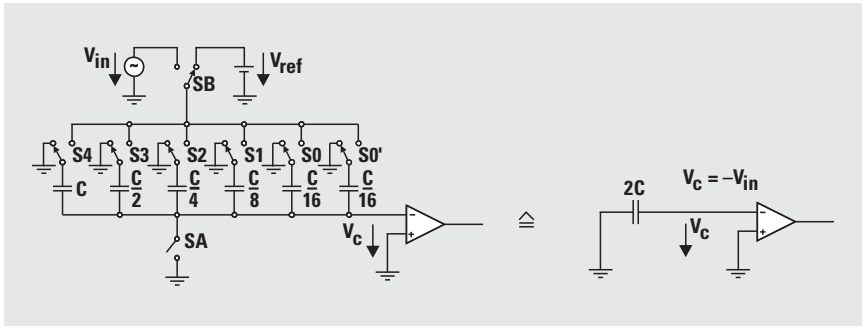


Figure 4. Conversion Step 1 determines the MSB (bit 4)

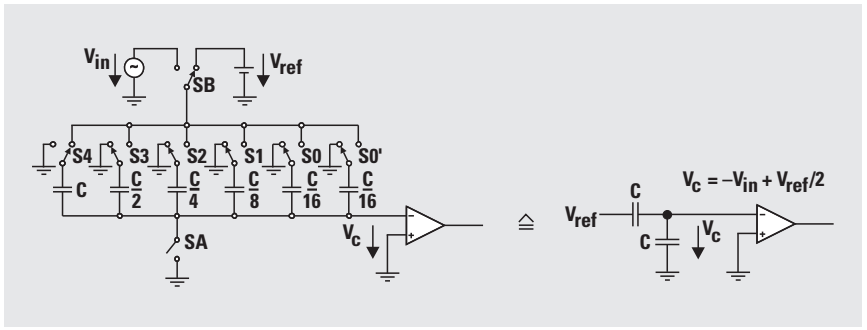


Figure 5. If bit 4 = 1, V_{in} is compared with 3/4 V_{ref}

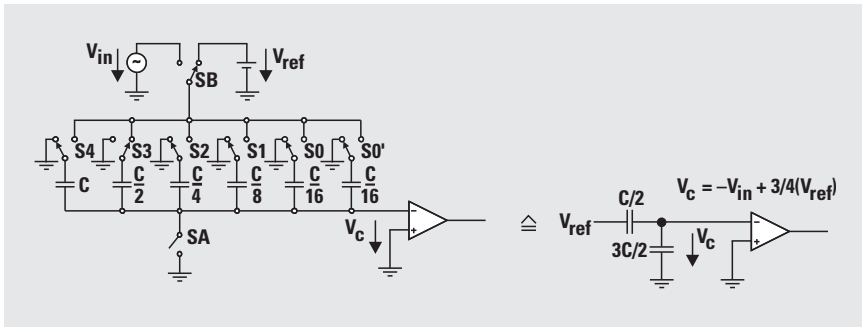
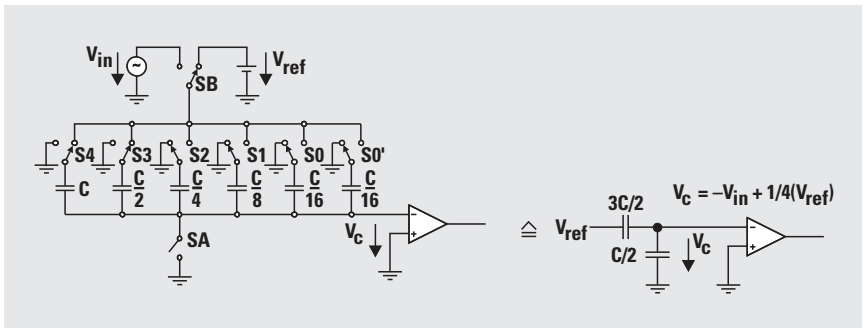


Figure 6. If bit 4 = 0, V_{in} is compared with 1/4 V_{ref}



Power supply solutions for TI DSPs using synchronous buck converters

By Bang S. Lee
Application Specialist, Power Management

Introduction

This article describes simple power solutions for TI's TMS320C6000 and TMS320VC54xx DSP applications using synchronous buck converter controllers such as the TPS56100, TPS5210, TPS56xx, and TPS5602. DSP power solutions from a single-input-only system (5-V or 12-V), a dual-input system (5-V and 12-V), and a wide-input voltage system (4.5-V ~ 25-V) are presented.

Review of DSP power requirements and synchronous buck converter controllers

The TI DSP families ('C6000 and 'C54xx) require separate core and I/O power. Table 1 summarizes the voltage supply for the current 'C6000 and 'C54xx families.

TI DSPs do not require specific power sequencing between the core supply and the I/O supply; however, systems should be designed to insure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long-term reliability of the device. System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers.

TI's synchronous buck converter controllers (TPS56100, TPS5210, TPS56xx, and TPS5602) are specifically designed to provide excellent transient response and high efficiency for the microprocessor power applications such as the 'C6000 and 'C54xx families from TI, as well as similar digital loads. In addition, the hysteresis control method is used so that power-supply designers do not have to worry about the stability and compensation issues. Table 2 summarizes the controller characteristics.

Table 1. Summary of DSP 'C6000 and 'VC54xx power requirements

TI DSP	CORE VOLTAGE (V)	I/O VOLTAGE (V)
TMS320C6201/'C6202/'C6211	1.8	3.3
TMS320C6202B/'C6203/'C6204/'C6205	1.5	3.3
TMS320C6701/'C6711	1.8	3.3
TMS320VC5402/'VC5409/'VC5420/'VC5421	1.8	3.3
TMS320VC549/'VC5410	2.5	3.3
TMS320VC5416/'VC5441	1.5	3.3

Solution 1—single-input voltage application (V_{in} = 5 V)

The TPS56100, a synchronous buck switch-mode power-supply controller, provides an accurate programmable supply voltage suitable for 5-V input-only microprocessor power applications. The reference voltage, ranging from 1.3 V to 2.6 V, is determined by the voltage programming (VP) pins. The output voltage can be set equal to the reference voltage using VP, or it can be extended to some multiple of the reference voltage using the sampling resistors (R2, R3) (see Figure 1). The TPS56100 also includes an inhibit input to control power sequencing and undervoltage lockout, thereby insuring the 5-V supply is within limits before the controller starts.

Table 2. Summary of the TI synchronous buck converter controller characteristics

	V_{in} RANGE (POWER STAGE) (V)	V_{CC} RANGE (CONTROLLER) (V)	V_{out} RANGE (POWER STAGE) (V)	I_{out}* (POWER STAGE) (A)	DRIVER CURRENT (CONTROLLER) (A)	OTHERS
TPS56100	5	5	1.3 to 2.6	7	2	1 channel
TPS5210	4.5 ~ 12	12	1.3 to 3.5	8	2	1 channel
TPS56xx	5	12	1.5, 1.8, 2.5, or 3.3	8	2	1 channel
TPS5602	4.5 ~ 25	4.5 ~ 25	Adjustable	4/channel	1.2 at V_o = 3 V	2 channels

*The current capability can be extended in multi-phase configuration or if the switching devices are added in parallel; see Table 2 in TI TPS56100/5210 datasheets.

Figure 1 shows the typical application circuit using the TPS56100, which features an accurate programmable step-down DC-DC converter. The VP pins and the two external resistors (R2, R3) determine a programmable output voltage from 1.3 V to approximately 5 V. The output voltage, V_O, is set with the following equation:

$$V_o = \left(1 + \frac{R2}{R3}\right) V_{ref} \qquad (1)$$

Figures 2 and 3 show power solutions using the TPS56100, suitable for 5-V-only systems. The application circuit for 1.5-V core and 3.3-V I/O supply voltage is identical with the figures except for the core voltage supply (1.5 V) and SVS. To avoid bus contention issues within a DSP system, the recommended start-up sequencing is met by using PWRGD (power good signal) pins as shown in the figures. The PWRGD connected to the Enable pin of the other power supply provides the start-up sequencing (core voltage first, then peripheral voltage). After approximately 10 ms —set by C5, R4, and R5 (see Figure 1)— the voltage on the PWRGD pin goes high, and the other TPS56100 is brought up.

The Schottky diode D1 provides a measure of protection during the power-down sequence and during other periods when the DV_{DD} supply is below the CV_{DD} supply by limiting the CV_{DD} - DV_{DD} voltage to the forward drop of D1. If CV_{DD} fails, the PWRGD pin of the power supply shuts down the other supply.

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Figure 1. A 5-V input-only application circuit using the TPS56100 (7-A output)

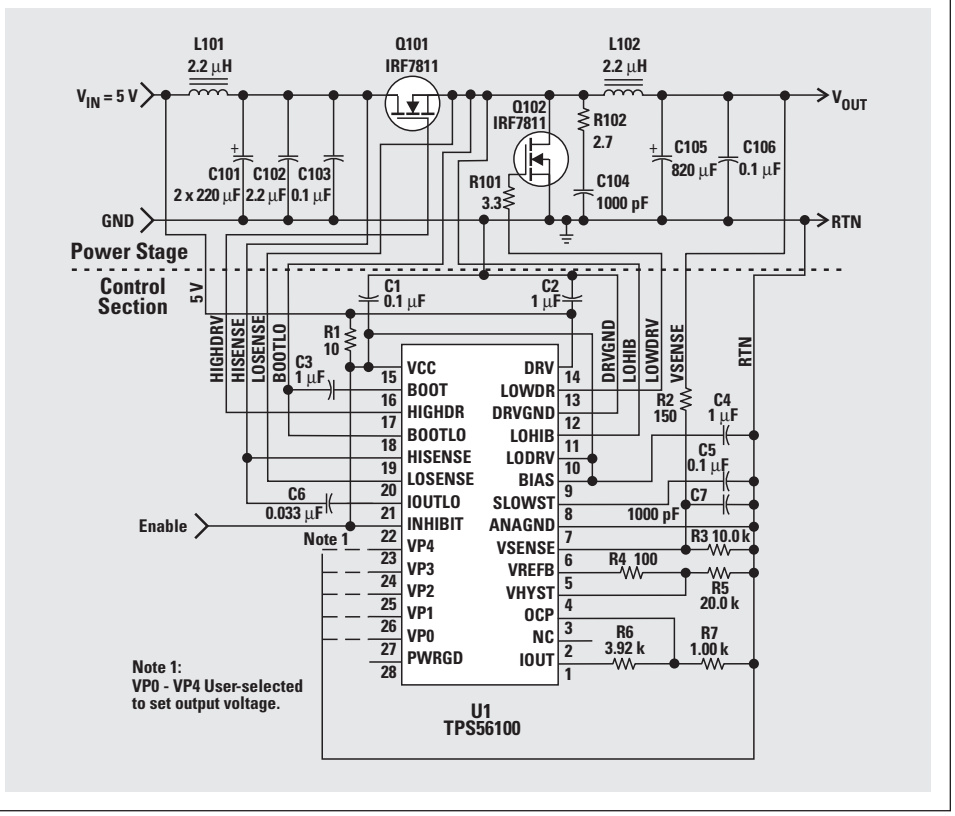

Figure 2. TMS320C6000/'VC5420/'VC5409/ 'VC5402 power-supply solution using TPS56100 for a 5-V input-only system

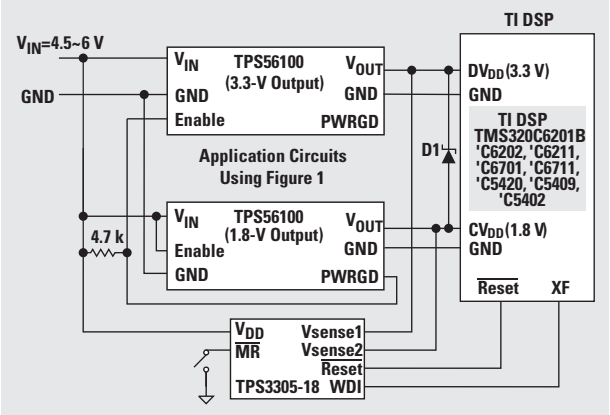

Figure 3. TMS320VC549/'VC5410 power-supply solution using TPS56100 for a 5-V input-only system

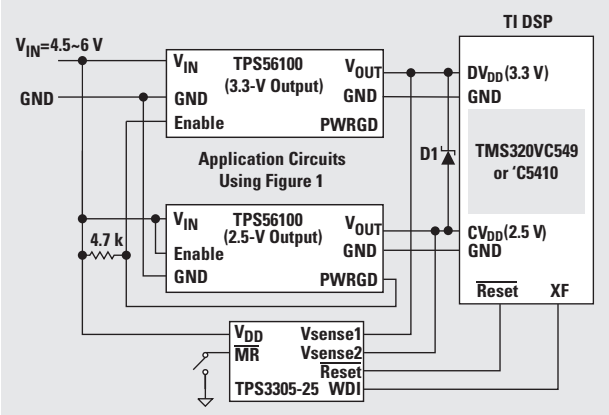

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Table 3. Summary of setting values for TPS56100 1.5-/1.8-/2.5-/3.3-V outputs

OUTPUT VOLTAGE (V)	R2 (Ω)	R3 (Ω)	C7 (pF)	VP TERMINALS (0 = GND, 1 = FLOATING OR PULL-UP TO 5 V)					V_{ref}
				VP4	VP3	VP2	VP1	VP0	(V_{dc})
3.3	1K	1K	100	0	1	0	0	0	1.65
2.5	100	20K	1000	1	1	0	1	0	2.50
1.8	100	20K	1000	0	0	1	0	1	1.80
1.5	100	20K	1000	0	1	0	1	1	1.50

Table 3 shows the setting values of TPS56100 to generate the output voltages 1.5 V, 1.8 V, 2.5 V, or 3.3 V. To obtain the 3.3-V output, set the reference voltage to 1.65 V and replace R2 and R3 with 1-kΩ resistors. For the 1.5-V, 1.8-V, and 2.5-V output voltages, the reference voltage represents the output voltage.

Two EVMs (evaluation modules)—SLVP128 (7-A output) and SLVP133 (3-A output)—are available to provide a convenient method for evaluating the performance of the TPS56100. A completed and tested power supply is included in each EVM.

Solution 2—single-input voltage application (V_{in} = 12 V)

The TPS5210 is suitable for single 12-V input-only system applications. The reference voltage, ranging from 1.3 V to 3.5 V, is determined by the voltage identification code (VID) pins. The output voltage can be set equal to the reference voltage using VID or can be extended to some multiple of the reference voltage using the external sampling resistors (R2, R3). The TPS5210 also includes an inhibit input to control power sequencing.

Figure 4 shows the typical application schematic using the TPS5210, which features a fast step-down DC-DC converter.

The VID pins and the two external resistors (R2, R3) determine a programmable output voltage from 1.3 V to approximately input supply voltage. The output voltage between 1.3 V and 3.5 V can be easily set by shorting the correct VID inputs to ground. Values above the maximum reference voltage (3.5 V) can be achieved by setting the reference voltage to any convenient voltage within its range and selecting values for R2 and R3 to give the correct output.

Figure 4. A 12-V input-only application circuit using the TPS5210 (8-A output)

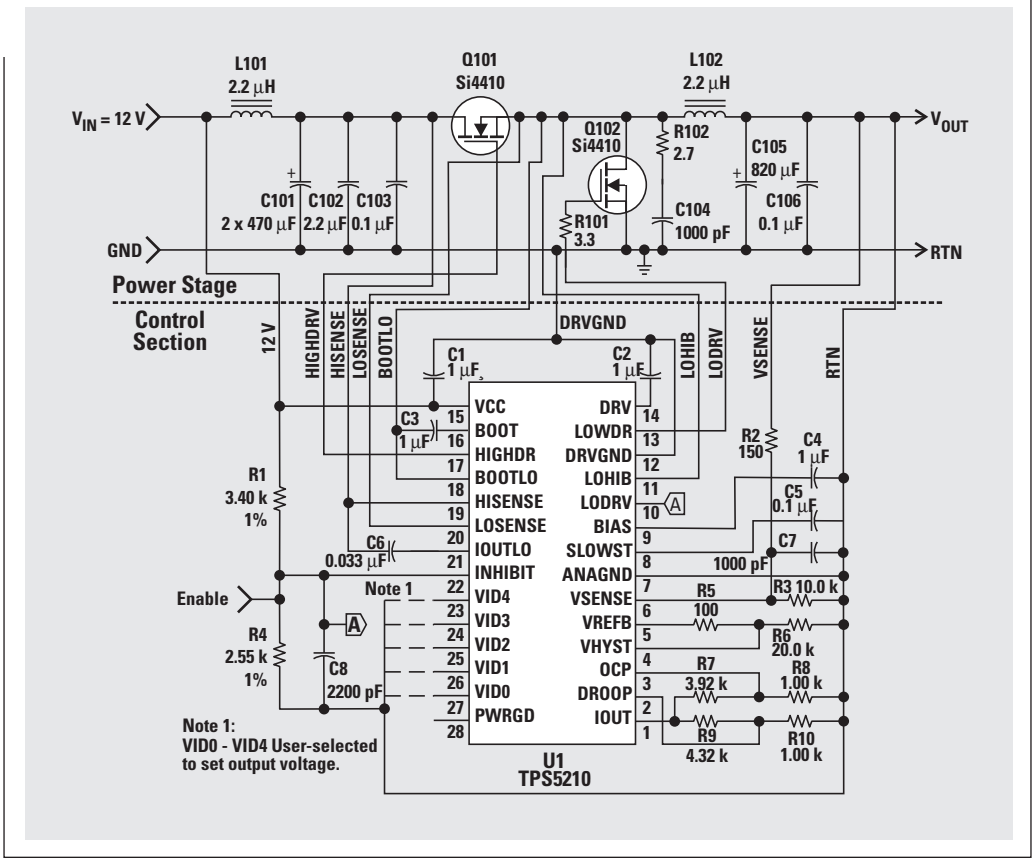

Table 4. Summary of setting values for TPS5210 1.5-/1.8-/2.5-/3.3-V outputs

OUTPUT VOLTAGE (V)	VID TERMINALS (0 = GND, 1 = FLOATING OR PULL-UP TO 5 V)					V_{ref}
	VID4	VID3	VID2	VID1	VID0	(V_{dc})
3.3	1	0	0	1	0	3.30
2.5	1	1	0	1	0	2.50
1.8	0	0	1	0	1	1.80
1.5	0	1	0	1	1	1.50

The output voltage is obtained with the following equation:

$$V_o = \left(1 + \frac{R2}{R3}\right) V_{ref} \quad (2)$$

R2 and R3 can also be used to make small adjustments to the output voltage within the reference voltage range and/or to adjust for load-current active droop compensation. If there is no need to adjust the output voltage, R3 can be eliminated.

Table 4 shows the setting values of TPS5210 to generate the output voltages 1.5 V, 1.8 V, 2.5 V, or 3.3 V. The reference voltage represents the output voltage.

The power solutions for TMS320C6000 and TMS320VC54xx using TPS5210 are shown in Figures 5 and 6. As described in the previous section, the cross-connection between PWRGD (power good signal) and Enable provides the start-up sequencing. The application circuit for 1.5-V core and 3.3-V I/O supply voltage is identical with Figures 5 and 6 except for the core voltage supply (1.5 V) and SVS.

The two power supplies should be placed close to the DSP to minimize the trace resistance and inductance and to minimize the ground loop current between the two output grounds. This ground loop current can generate radiated EMI noise that can adversely affect any circuitry within the loop. The ground connection must be made directly on the DSP to help minimize the problem.

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Figure 5. TMS320C6000/'VC5420/'VC5409/'VC5402 power-supply solution using TPS5210 for a 12-V input-only system

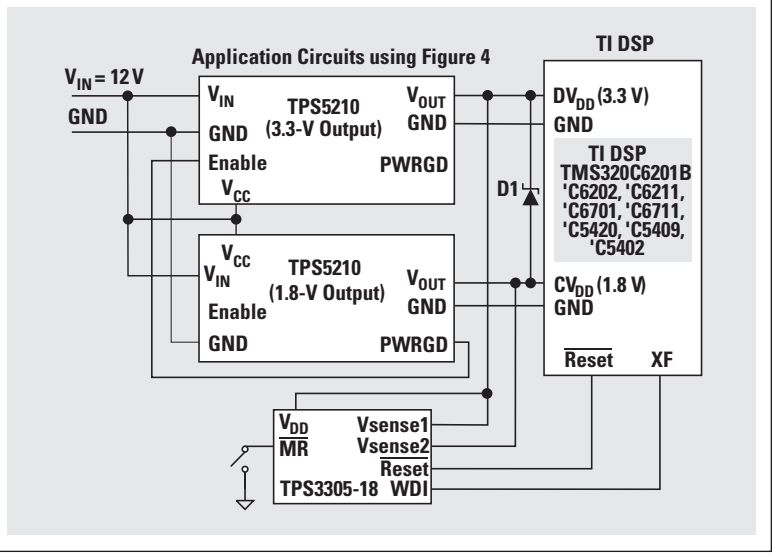

Figure 6. TMS320VC549/'VC5410 power-supply solution using TPS5210 for a 12-V input-only system

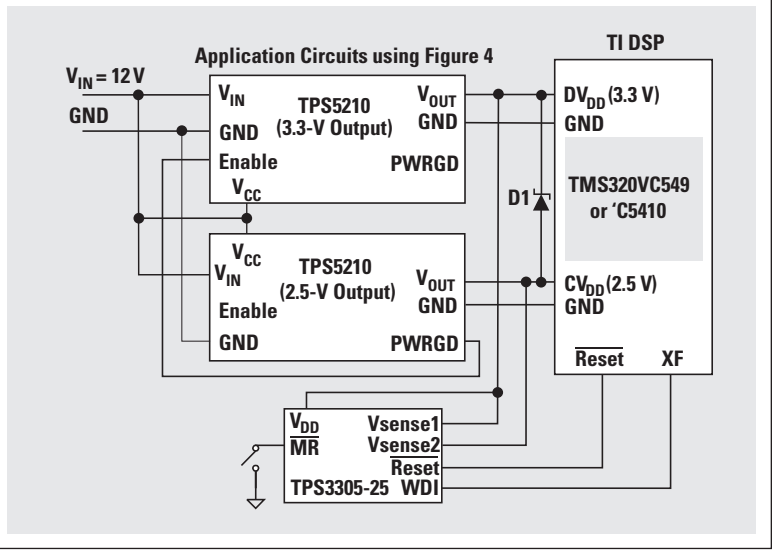

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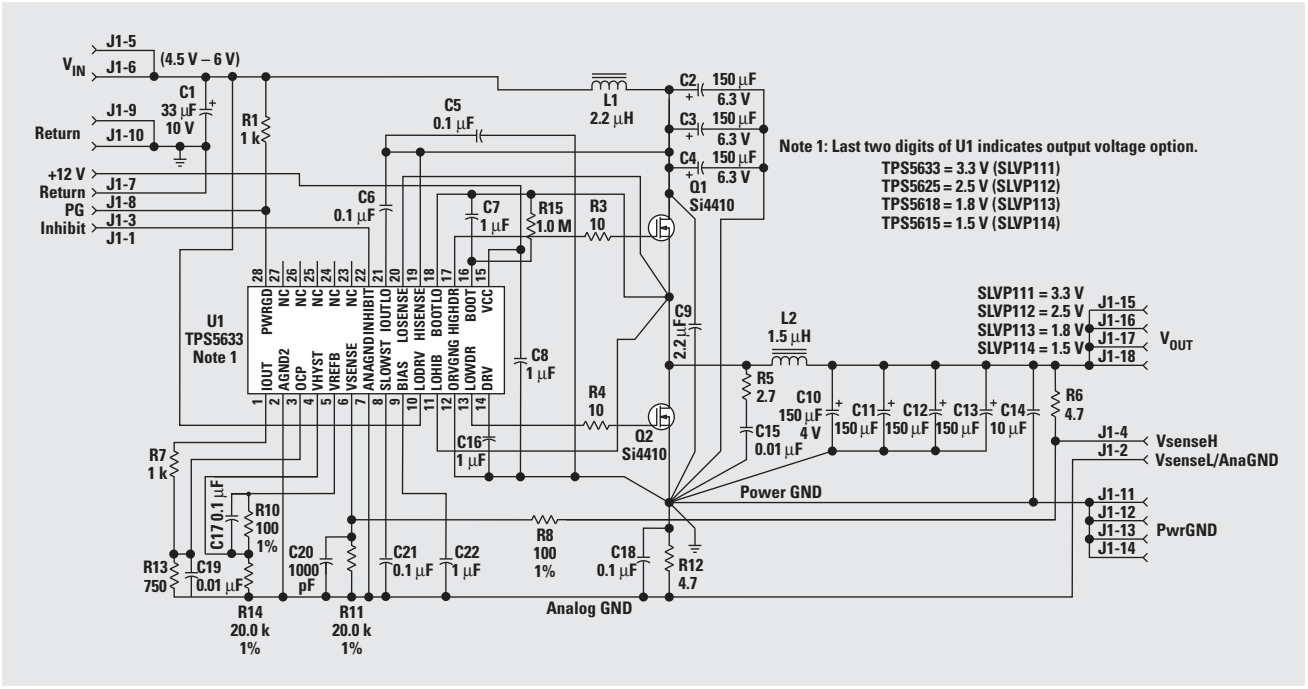
Figure 7. A dual-input application circuit using the TPS56xx (8-A output)



Solution 3—dual-input voltage application (V_{in} = 5 V and 12 V)

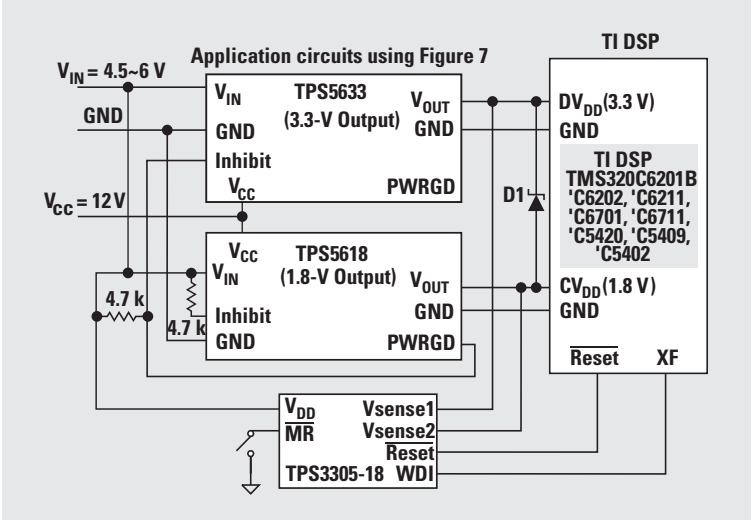
The TPS56xx, a synchronous buck switch-mode power-supply controller, is useful in applications with dual-input voltages and wide DC load ranges, such as multiple-DSP applications. Synchronous buck converters using the TPS56xx feature fixed output voltages of 3.3 V, 2.5 V, 1.8 V, or 1.5 V, providing an elegant power-supply solution for rapidly transitioning DSP loads, fast memory, and similar processors.

A hysteretic controller with user-selectable hysteresis is used to dramatically reduce overshoot and undershoot caused by load transients. The inhibit pin can be used to control power sequencing. Inhibit and undervoltage lockout assures that the 12-V supply voltage and system supply voltage (5 V) are within proper operating limits before the controller starts.

Figure 7 shows the typical application circuit using the TPS5633, which features an accurate 3.3-V output. The optional output voltages (1.5 V, 1.8 V, or 2.5 V) are obtained by replacing controller U_1 with TPS5615, TPS5618, or TPS5625 devices, since the power stage circuitry is identical.

Power solutions using the TPS56xx for TI's DSP are shown in Figures 8 and 9. The application circuit for 1.5-V core and 3.3-V I/O supply voltage can be implemented as described in previous sections.

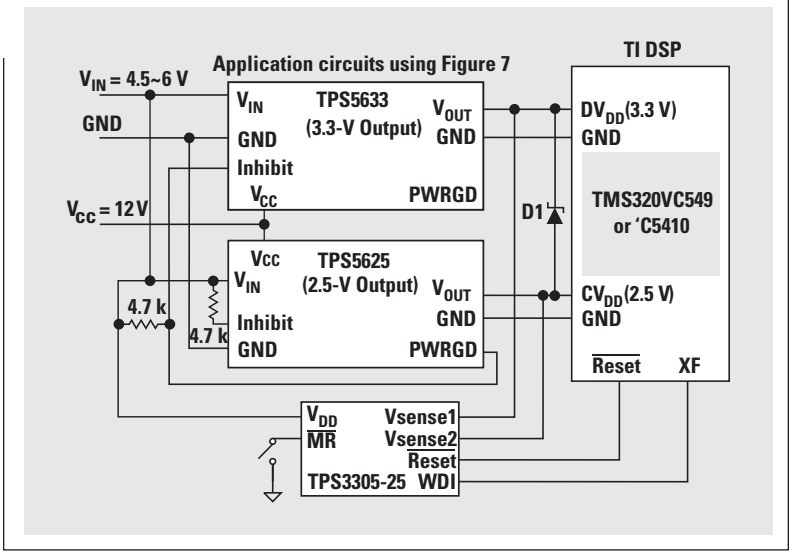
Figure 8. TMS320C6000/'VC5420/'VC5409/'VC5402 power-supply solution using the TPS5618 and TPS5633 for a dual-input system



The PWRGD connected to the inhibit pin of the other power supply provides the start-up sequencing (core voltage first, then peripheral voltage). After approximately 10 ms—set by C21, R10, and R14 (Figure 7)—the voltage on the PWRGD pin goes high, and the other TPS56xx is brought up.

Four EVMs—the SLVP111 (3.3 V), SLVP112 (2.5 V), SLVP113 (1.8 V), and SLVP114 (1.5 V)—are available to provide a convenient method for evaluating the performance of the TPS56xx. A completed and tested power supply is included in the EVM.

Figure 9. TMS320VC549/'VC5410 power-supply solution using the TPS5625 and TPS5633 for a dual-input system (5 V and 12 V)



Solution 4—single wide-input voltage application (V_{in} = 4.5 ~ 25 V)

TI TPS5602, a dual-channel synchronous buck switch-mode power-supply controller, features very fast feedback control and dual channels and is designed specifically for DSP applications that require single wide-input applications. The up and down power sequencing can be easily achieved by setting the standby pins, since both channels are independent. The wide-input voltage and adjustable output voltage make the TPS5602 suitable for many applications.

Figure 10 shows a typical circuit design using the TPS5602 that features a dual-channel synchronous buck converter (1.8-V and 3.3-V outputs). The two output voltages are independent and can be adjustable (1.2-V to approximately input voltage) by using the sampling resistors such as R1,

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Figure 10. A single wide-input application circuit using the TPS5602 (8-A output)

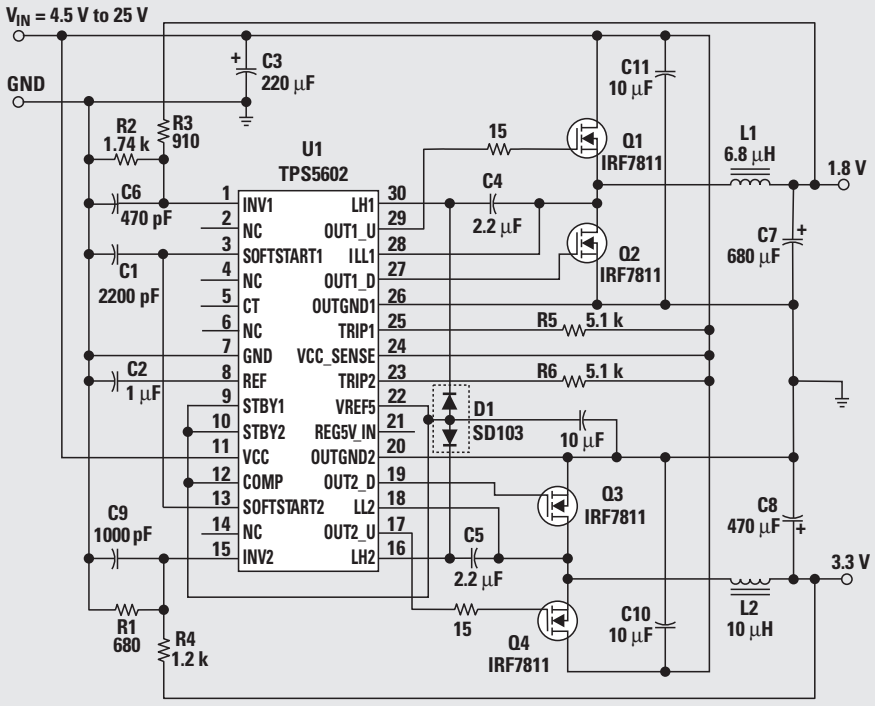

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Figure 11. Fast load transient response

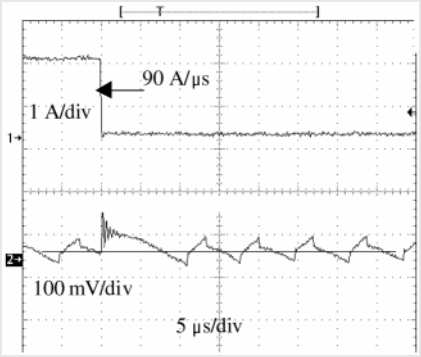


Figure 12. Efficiency of 3.3-V output

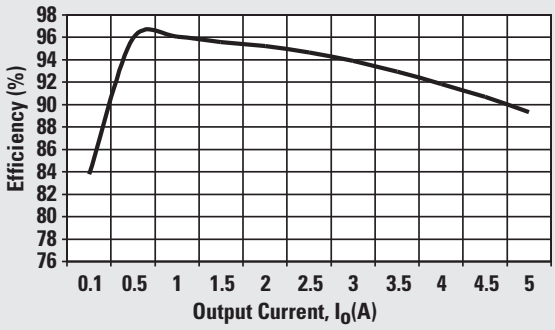
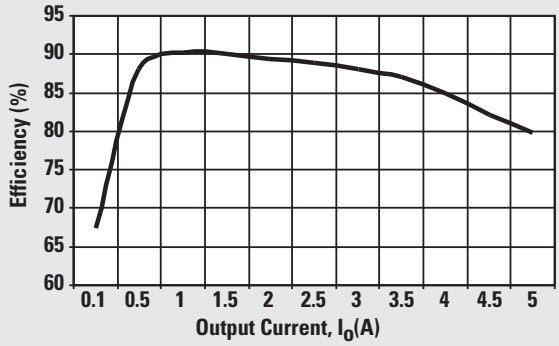


Table 5. Summary of setting values for TPS5602 1.5-/1.8-/2.5-/3.3-V outputs

OUTPUT VOLTAGE (V)	R2 (or R1) (Ω)	R3 (or R4) (Ω)
3.3	680	1.2K
2.5	1K	1.1K
1.8	1.74K	910
1.5	10K	2.67K

Figure 13. Efficiency of 1.8-V output



R2, R3, and R4. The output voltages, OUT1 and OUT2, are set with the following equations, where the reference voltage is 1.185 volts:

$$V_{OUT1} = \left(1 + \frac{R3}{R2}\right) V_{ref} \qquad (3)$$

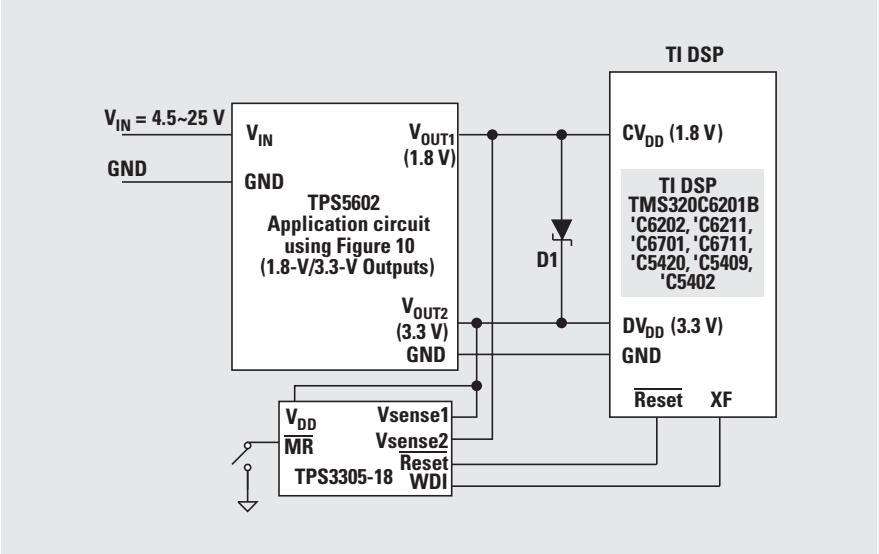
$$V_{OUT2} = \left(1 + \frac{R4}{R1}\right) V_{ref} \qquad (4)$$

Figure 11 shows the TPS5602's transient response. The response is less than 2 microseconds after a load is applied. Conventional PWM buck converters exhibit approximately 100 microseconds of response. Figures 12 and 13 show the efficiency of the two controllers over load up to 5 A. Efficiency can be improved by choosing lower on-resistance MOSFET.

Table 5 shows the setting values of TPS5602 to generate the output voltages 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

The power solutions for TMS320C6000 and TMS320VC54xx using TPS5602 are shown in Figures 14 and 15. The application circuit for 1.5-V core and 3.3-V I/O supply voltage can be implemented as described in previous sections.

Figure 14. TMS320C6000/'VC5420/'VC5409/'VC5402 power-supply solution using TPS5602 for a single wide-input system (4.5 V ~ 25 V)



By using the SOFTSTART1 and SOFTSTART2 pins in Figure 10, the start-up sequencing (core voltage first, then peripheral voltage) can be easily achieved. The SOFTSTART timing can be adjusted by selecting the SOFTSTART capacitor value such as C1 and C12 shown in Figure 10. The equation is

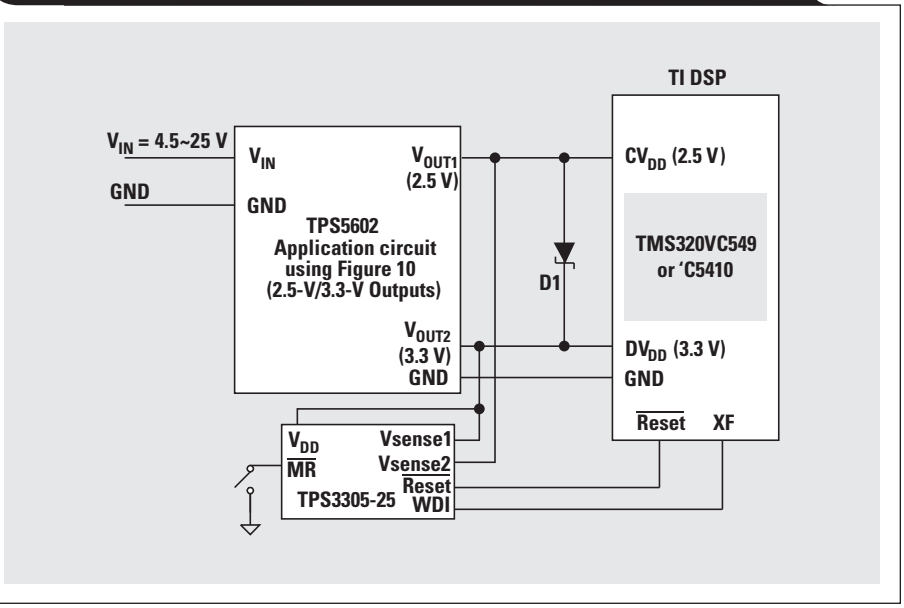
$$C_{soft}(\mu F) = 2 \times T_{soft}(ms), \quad \textbf{(5)}$$

where C_{soft} is the SOFTSTART capacitance and T_{soft} is the start-up time.

For example, to set the start-up time T_{soft} = 5 ms, the capacitance value of C_{soft} = 0.01 µF is needed.

In addition, the TPS5602 has two external pins (STBY1, STBY2) that can be used alternatively for power-up sequencing.

Figure 15. TMS320VC549/'VC5410 power-supply solution using the TPS5602 for a single wide-input system (4.5 V ~ 25 V)



References

For more information related to this article, visit the TI Web site at www.ti.com/ and look for the following materials by entering the TI literature number into the quick-search box.

Document Title	TI Lit. #
1. TPS3305 Application Report	SLVA056
2. TPS5210 Data Sheet	SLVS243
3. TPS5210 User's Guide	SLVU010, SLVU011
4. TPS56xx Data Sheet	SLVS177a
5. TPS56xx User's Guide	SLVU007, SLVU013
6. TPS5602 Data Sheet	SLVS217
7. TPS56100 Data Sheet	SLVS201a
8. TPS56100 User's Guide	SLVU018

Related Web sites

Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device***.html**
Replace *device* with tps3305-18, tps3305-25, tps5210, tps5211, tps5602, tps5615, tps5618, tps5625, tps5633, or tps56100

www.ti.com/sc/docs/products/dsp/c5000/index.htm

www.ti.com/sc/docs/products/dsp/c6000/index.htm

www.ti.com/sc/docs/products/dsp/tms320*device***.html**
Replace *device* with c6201, c6202, c6211, c6701, c6711, vc549, vc5402, vc5409, vc5410, or vc5420

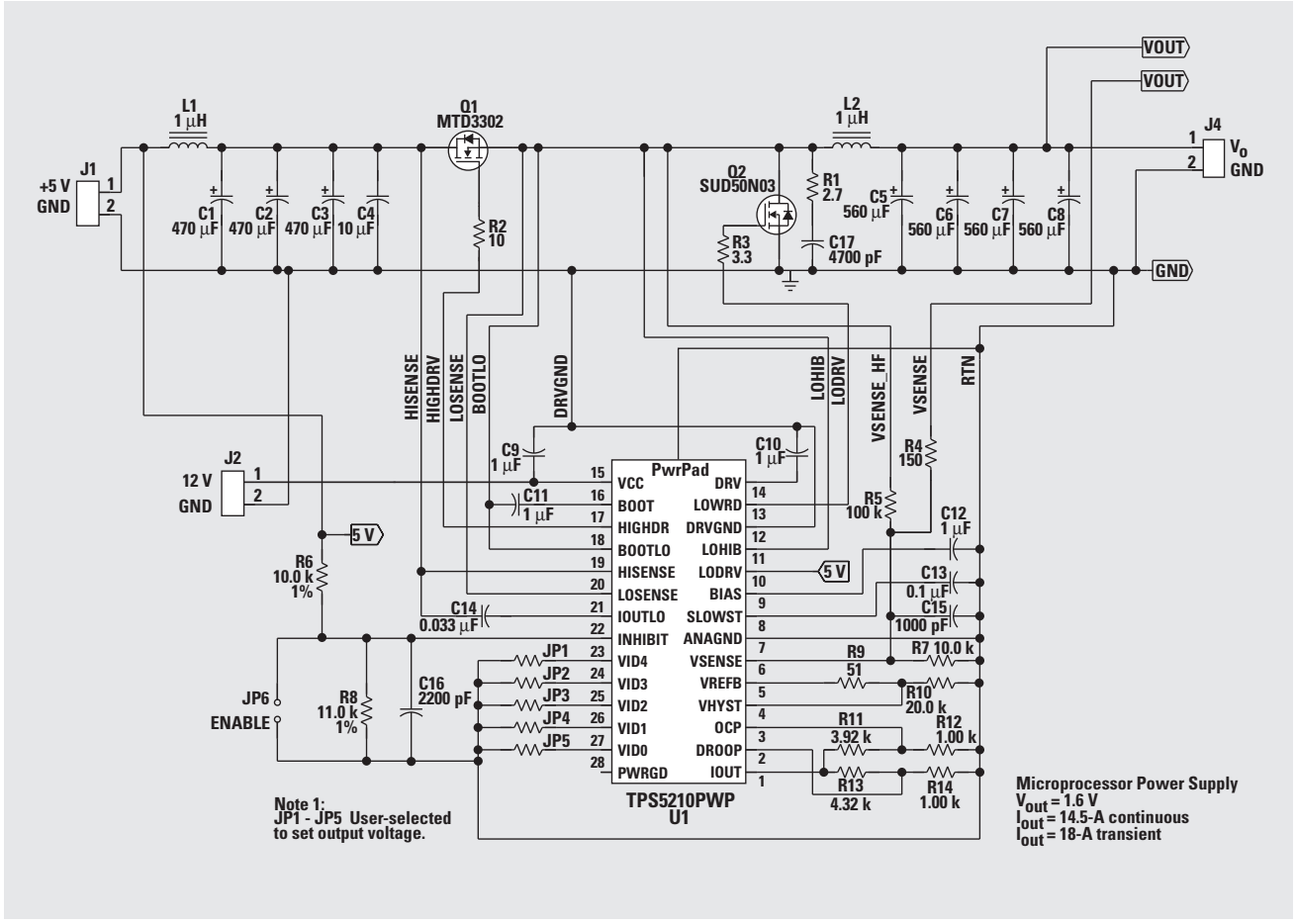
Powering Celeron-type microprocessors using TI's TPS5210 and TPS5211 controllers

By Rais Miftakhutdinov, *System Engineering, Power Management Products,*
and Philip Rogers, *System Engineering, Power Management Products*

Introduction

Performance of desktop application microprocessors is improving rapidly, approaching the requirements that were typical for servers and workstations just a few years ago. In this high-performance PC, the voltage regulator has to supply the high current consumed by the microprocessor core to keep the core voltage within tight static and dynamic tolerances for minimum cost. The TPS5210EVM-147 (SLVP147) evaluation module has been designed and tested to confirm TI's TPS5210 and TPS5211 hysteretic controller performance to supply future Celeron™ microprocessors. The SLVP147 includes a synchronous DC-DC buck converter, high-frequency decoupling capacitors for PGA-370 microprocessor packages, and a load-current transient tester. The DC-DC converter has 5-V input and 1.6-V output voltage and requires 12 V, 30 mA for the controller itself. It was designed as a low-cost solution in motherboard applications where small size is very important. The temperature of the components does not exceed 72°C at room ambient temperature with a load current of 14.5 A. The module has excellent transient characteristics at a peak load current of up to 18.4 A. A four-layer PCB had been used in the module to get electrical and temperature conditions close to actual conditions. The module meets electrical specifications of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines" for >733-MHz clock and 133-MHz bus-frequency Celeron processors.

Figure 1. DC-DC synchronous buck converter schematic



For this application R5 is open.

Brief description of the SLVP147 evaluation module

Several evaluation modules for different desktop motherboard applications have been designed. The description and characteristics of one of them is presented in this report.

The SLVP147 evaluation module (4" x 3.25" x 0.8") includes three main parts:

- 1.6-V power supply (2" x 1.5" x 0.8"),
- Processor bypass capacitors, and
- Transient load.

The four-layer, 1-oz. FR-4 PCB board, which is typical for motherboards, had been used in the module to simulate actual application conditions for an embedded point-of-load power supply.

1.6-V power supply

The 1.6-V power supply is a DC-DC synchronous buck converter (see the schematic in Figure 1 and lower right corner of the evaluation module in Figure 2) that includes input and output filters, power stage, and control section.

The input voltage for the power section is 5 V ± 0.5 V, and the control section requires 12 V ± 0.6 V. All power-supply components are placed in the corner of the board to model the worst-case cooling conditions. Because of

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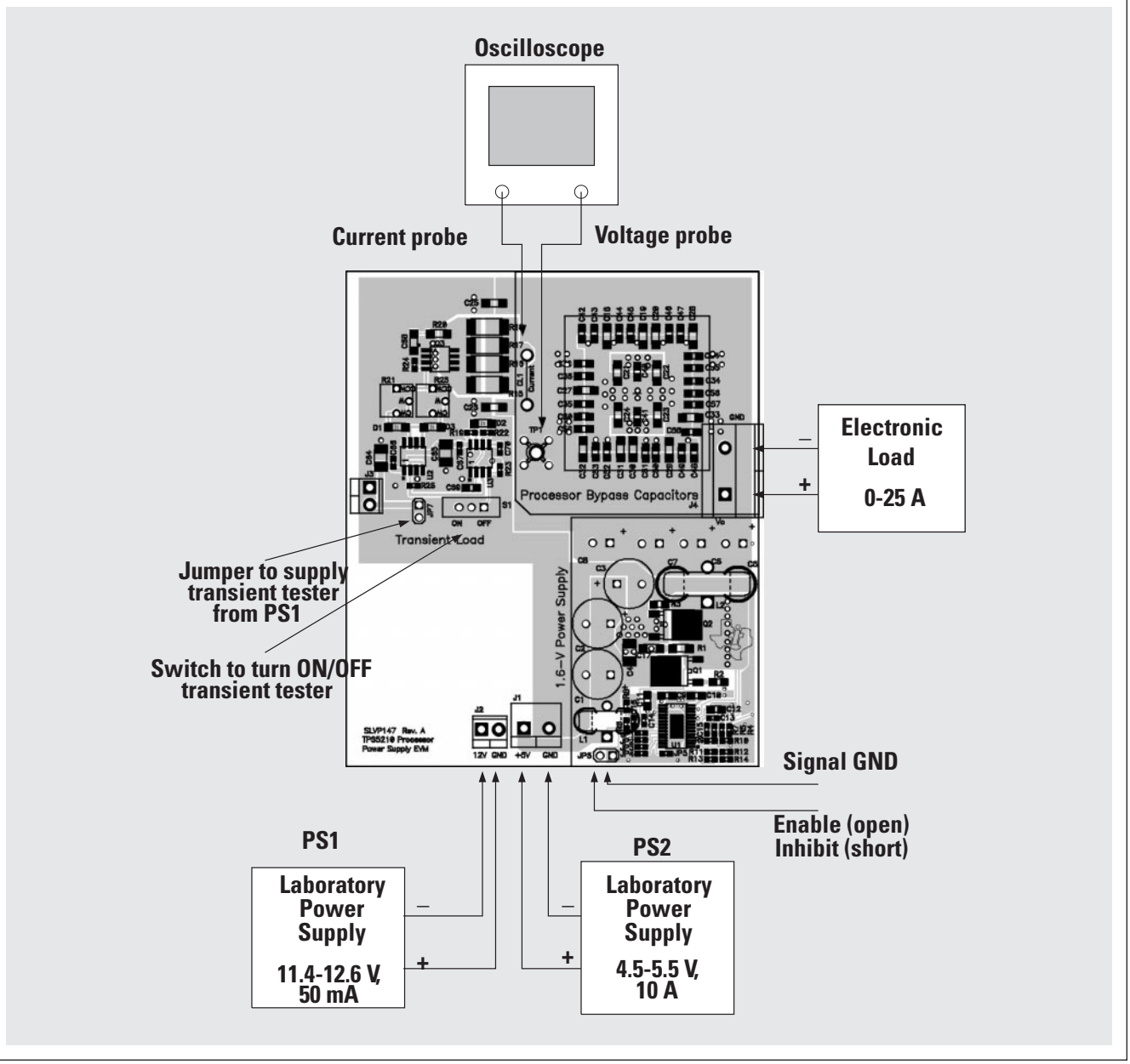
Figure 2. Test setup for SLVP147 EVM



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minimum size requirements, high-performance OS-CON-type capacitors have been selected for the input and output filters. The input filter includes three 10SP470M capacitors C1–C3, 10-µF ceramic capacitor C4, and 1-µH inductor L1. The input capacitors can handle a total maximum RMS current as high as 13.5 A. The output filter has four OS-CON-type capacitors (4SP560M) and a 1-µH inductor, L2. The fast hysteretic controller and active droop reduce the number of capacitors while having a reliable margin for dynamic tolerance. The power stage includes power FETs in DPAK packages Q1, Q2, gate resistors R2 and R3, and snubber circuitry including resistor R1 and capacitor C17. The selection of a 10-MΩ MTD3302 high-side FET and a 7-MΩ SUD50N03-07 low-side FET is a compromise between cost and efficiency.

The controller section is based on the high-performance TPS5210 hysteretic controller and provides the following main functions:

- Adaptive dead-time-control high- and low-side drivers with an 8-V drive regulator and internal bootstrap diode to switch power FETs with minimum control and switching losses
- A sample-hold circuit to sense the V_{ds} of the high-side FET for shutdown overcurrent protection and active droop compensation without expensive external current sensors
- A fast hysteresis comparator, which does not need feedback loop compensation circuitry that reacts to transients in 400–500 ns without restrictions on duty cycle (the hysteresis window is set by an external resistor as a percentage of the reference voltage)
- A 5-bit VID code, enable/inhibit signal input, power good signal, undervoltage lockout for both 12-V and 5-V inputs, and overvoltage shutdown

Processor bypass capacitors

The high-frequency decoupling capacitors (see the upper right corner of the evaluation module in Figure 2) occupy the same area as the cavity of the PG-370 package to model real-load current transient conditions. The decoupling circuitry includes 27 ceramic 0805 1-µF capacitors and 16 ceramic 4.7-µF capacitors in 1206 packages. Test point

Table 1. VRM 8.4 requirements and test data

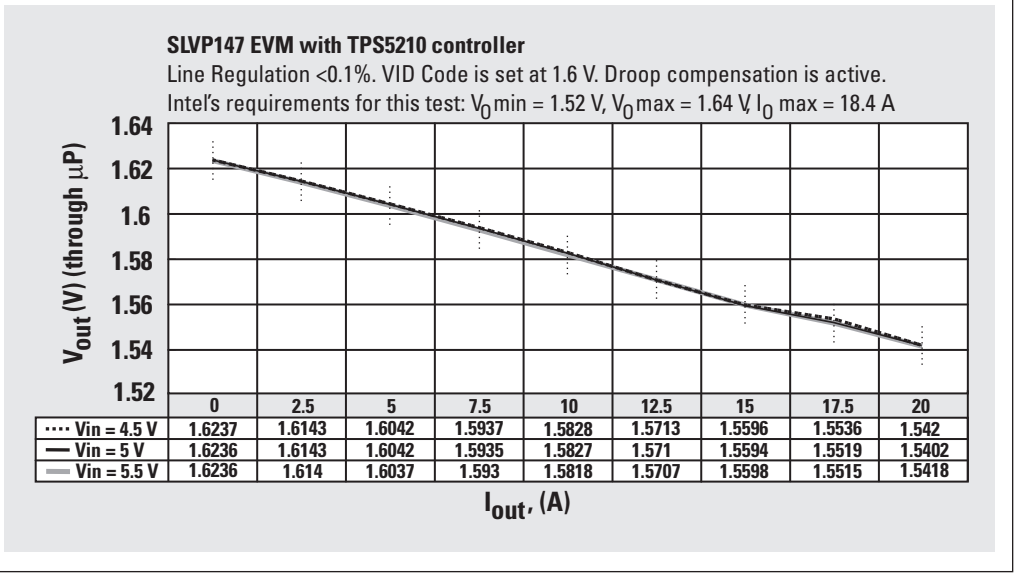
TEST	DESCRIPTION	SPECIFICATION	DATA
1	Operating voltage and load current (VRM 8.4. sections 1.1 and 1.2)	Input voltages 4.75 to 5.25 VDC and 11.40 to 12.6 VDC. Load current 0 to 18.4 A	Unit operates over the full input-voltage and load-current range at switching frequency 135 to 175 kHz (Figure 7)
2	Steady-state output voltage (VRM 8.4. section 1.1)	Output voltage within 1.52 to 1.64 VDC	Output voltage over the full input-voltage and load-current range within 1.551 to 1.624 V including droop compensation. Temperature regulation and set point < 1% (Figure 3).
3	Transient output voltage (VRM 8.4. section 1.1)	Output voltage within 1.52 to 1.65 VDC at load-current steps in 0.8- to 18.4-A range with 20-A/µs slew rate	Output voltage within 1.552 to 1.644 V, response time < 500 ns, recovery time < 7 µs for step-up and < 34 µs for step-down (Figures 4 and 5)
4	Output ripple and noise (VRM 8.4. section 1.1)	Included in steady-state output-voltage requirements. Measured with 20-MHz frequency band.	20-mV peak-to-peak maximum (Figure 6)
5	Turn on overshoot (VRM 8.4. section 1.1)	< 10%, no load and full load	< 1.3% at all load conditions (Figure 11)
6	Turn on response time (VRM 8.4. section 1.1)	< 10 ms	< 9 ms (Figure 11)
7	Power good signal (VRM 8.4. section 1.1)	High if the output voltage exceeds ±12% from nominal; otherwise low, transition to high within 20 ms	±12% from nominal, guaranteed by controller design
8	Output enable (VRM 8.4. section 1.3)	Open-collector input signal	Guaranteed by controller design (Figure 11)
9	5-bit VID (VRM 8.4. section 1.3)	Input open-collector TTL signals	Guaranteed by controller design, internal pull-up resistors
10	Efficiency (VRM 8.4. section 1.4)	> 80% at 14.5-A output current. > 40% at 0.5-A output current.	83.5% at 15 A after 12 hours of operation (Figure 8)
11	Overcurrent protection, output short circuit current (VRM 8.4. section 1.5)	Withstands a continuous short circuit of the output	Converter shuts down if the load current exceeds 22 A or shorts. Restarts by cycling V_{CC} voltage.
12	Overvoltage protection (VRM 8.4. section 1.5)	Latches output off if V_{out} = 110 to 125% of nominal	Internal overvoltage protection if V_{out} = 112 to 120% of nominal
13	Maximum component temperature	FETs < 90°C at room temperature with natural cooling	FETs = 72°C, capacitors = 52°C, PCB = 47°C at room temperature of 22°C
14	Dimensions	2.5" x 1.5" x 0.8" (target for embedded regulator, not for VRM 8.4)	2.0" x 1.5" x 0.8"

TP1 (for DC and transient measurements) is placed in the area occupied by the processor to model the worst-case conditions.

Transient load

The transient load tester (see the upper left corner of the evaluation module in Figure 2) provides the high slew-rate load-current pulses. It includes an oscillator based on the TLC555D timer, a TPS2812D driver, and a FET switch connected in series with paralleled resistors to produce the required load-current transient amplitude. The slew-rate levels during rise and fall times can be adjusted separately by variable resistors. The wire loop in series with the load resistors for inserting a current probe provides accurate load-current measurements during transients.

Figure 3. Steady-state output voltage with active droop compensation for improved transient response

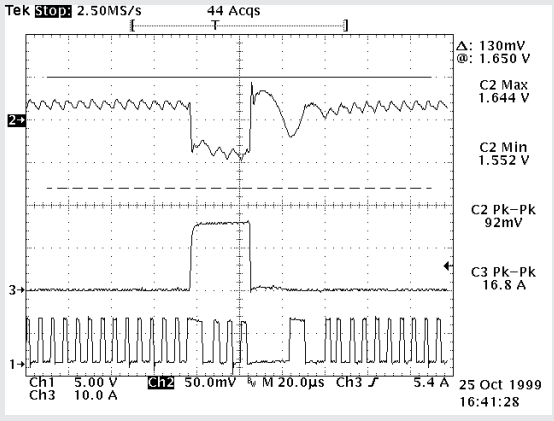


	0	2.5	5	7.5	10	12.5	15	17.5	20
Vin = 4.5 V	1.6237	1.6143	1.6042	1.5937	1.5828	1.5713	1.5596	1.5536	1.542
Vin = 5 V	1.6236	1.6143	1.6042	1.5935	1.5827	1.571	1.5594	1.5519	1.5402
Vin = 5.5 V	1.6236	1.614	1.6037	1.593	1.5818	1.5707	1.5598	1.5515	1.5418

Test results comparison with Intel requirements for VRM 8.4

The design of the SLVP147 EVM is based on the electrical specifications of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines" for >733-MHz clock and 133-MHz bus-frequency Celeron processors. The simplified block diagram of the test setup and the EVM itself are shown in Figure 2.

Figure 4. The output-voltage transient response waveforms measured at test point TP1



The cursors show the limits for this test: 1.52 V minimum and 1.65 V maximum. Ch2 shows output voltage (50 mV/div.), Ch3 shows load current (10 A/div.), and Ch1 shows drain-source voltage (5 V/div.).

All measurements were made at room temperature. During transient tests with 16.8-A load-current steps, the electronic load has been set at 0.8 A to preload the power supply in accordance with VRM 8.4 specification. The VRM 8.4 requirements and test data are shown in Table 1.

Detailed test results and main waveforms

Steady-state output voltage

The steady-state output voltage, measured at test point TP1 at 0- to 20-A load current and 4.5- to 5.5-V input-voltage range, is shown in Figure 3. (The peak load current for this application is 18.4 A.) The line regulation is less than 0.1% (1.6-mV tolerance over the entire input-voltage range). The output voltage depends on the load current because active droop compensation has been used to improve the output-voltage transient tolerance and reduce the number of bulk capacitors. The total voltage droop is 83.5 mV for a current range from 0 to 20 A. Resistor divider R13, R14 sets the 75-mV active droop at a load current of 20 A. The remaining portion of droop (83.5 – 75 = 8.5 mV) relates to the load regulation and droop through supply trace resistance. To compensate the droop, the output voltage had been increased 24 mV above the nominal 1.6 V. It is obvious from Figure 3 that the output voltage is well inside the VRM8.4 specification for a static condition, which is 1.52 V minimum and 1.64 V maximum measured through the microprocessor pins.

Load-current transient response

The output-voltage waveform during the load-current step-up and step-down 16.8-A transition is shown in Figure 4. In accordance with VRM8.4 requirements, the power supply is preloaded by a 0.8-A DC current, which is not included in the load-current transient waveform. The

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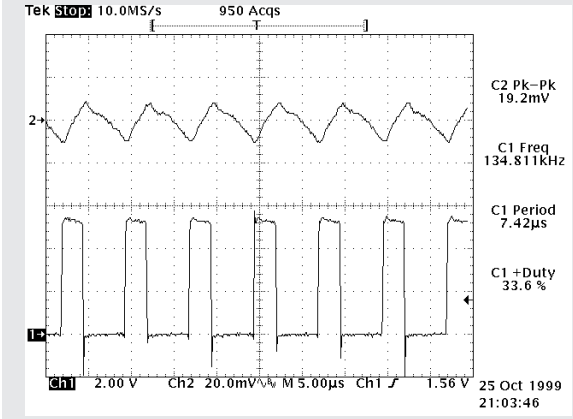
load-current slew rate is 40 A/µs during step-down and 20 A/µs during step-up. The maximum slew rate during load-current step-up is restricted by the stray inductance of the transient tester paths. The peak-to-peak output-voltage amplitude is 92 mV using four 4SP560M OS-CON capacitors. The output-voltage transient lasts only 7 µs for step-up and 34 µs for step-down, which is much less than the 100-µs recovery time from VRM 8.4 requirements.

Special attention has been paid to study the delays between the output-voltage transient and the turn-on of the corresponding FET to see the fast transient response of the hysteretic controller. This delay is 340 ns during the load-current step-down (Figure 5a) and 500 ns during step-up (Figure 5b). Theoretically a voltage mode or current mode controller starts reacting to transients only at the next switching period. To get the same reaction time, these controllers have to run at a switching frequency of over 2 MHz. One can see that the hysteretic controller changes duty cycle in the same switching period when the load-current transient occurs.

Output-voltage ripple and switching frequency range

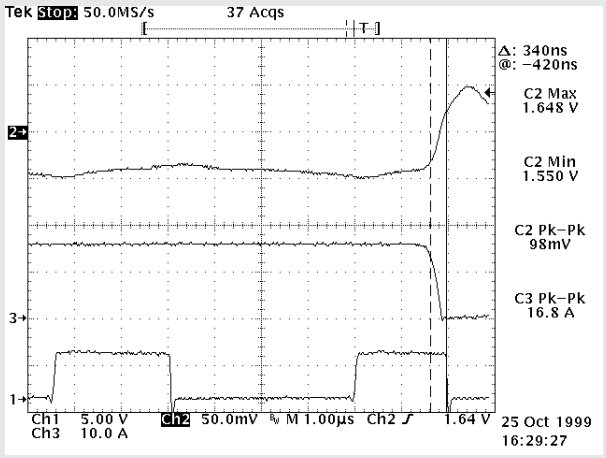
The output-voltage ripple and low-side FET drain-source voltage waveforms are shown in Figure 6. The maximum peak-to-peak ripple does not exceed 20 mV.

Figure 6. Output-voltage ripple and low-side FET drain-source voltage at V_{in} = 5 V, I_{out} = 18 A

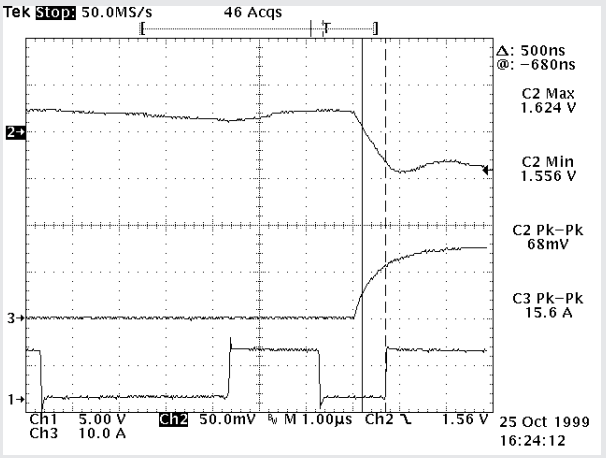


Ch2 shows output-voltage ripple (20 mV/div.), and Ch1 shows drain-source voltage (2 V/div.).

Figure 5. Expanded waveforms during the load-current step-down (a) and step-up (b)



(a)



(b)

The cursors show the 340-ns (a) and 500-ns (b) delays to turn the corresponding FET on after the transient occurs. Ch2 shows output voltage (50 mV/div.), Ch3 shows load current (10 A/div.), and Ch1 shows drain-source voltage (5 V/div.).

The frequency variation is within 135 to 175 kHz over the entire input-voltage and output-current range (see Figure 7). The switching frequency for hysteretic controllers depends on input and output voltage and output filter characteristics. The precise equation for the switching frequency, confirmed by experiments, is represented in TI's application report, "Designing Fast Response Synchronous Buck Converters Using the TPS5210," literature number SLVA044.

Efficiency, power losses, and temperature of components

Efficiency and power losses over the entire input-voltage and output-current range are shown in Figures 8a and 8b. These measurements were made after 12 hours of operation when the temperature of the PCB and components had stabilized. An additional power loss of 0.24 W from the 12-V input is also counted. Efficiency at 15-A load current is 82.8% and, at 0.5 A, is 60.5%. This exceeds specification requirements of 80% and 40%, respectively. The maximum power losses at 15-A load current do not exceed 4.85 W.

The temperature measurements of the main components are shown in Table 2. The measurements were made at a room temperature of 22°C with 5-V input voltage and 14.5-A load current. The cooling conditions were natural without airflow in accordance with the specification. The maximum temperature rise is 50°C on the high-side FET, while the temperature rise of the PCB itself is 25.8°C. These are reasonable values; nevertheless, it is very possible that because the real motherboard has a much larger cooling area, the components will have a lower temperature in the system.

One can see that there is no big difference in temperature of the parallel capacitors, meaning that there is almost equal current sharing between them. The temperature of most components is very close to the PCB temperature.

Continued on next page

Table 2. Temperature measurement results

COMPONENT	PCB	Q1, HIGH-SIDE FET	Q2, LOW-SIDE FET	L1, INPUT IND.	L2, OUTPUT IND.	U1, CONTROLLER	INPUT CAPACITORS			OUTPUT CAPACITORS			
							C1	C2	C3	C5	C6	C7	C8
Temp. (°C)	47.8	72	70	45	50.5	47.5	51.2	48.3	48.3	44.7	45.5	41.3	41
Temp. Rise (°C)	25.8	50	48	23	28.5	25.5	29.2	26.3	26.3	22.7	23.5	19.3	19

Figure 7. Switching frequency variation over the entire input-voltage and output-current range

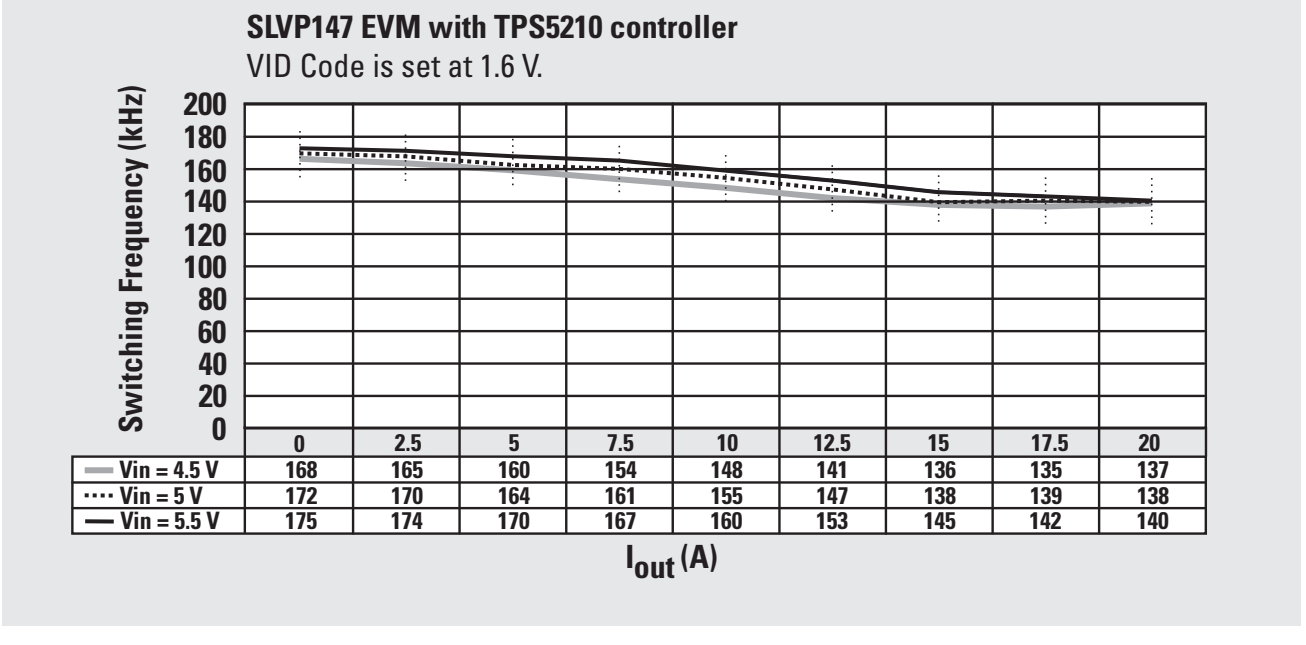


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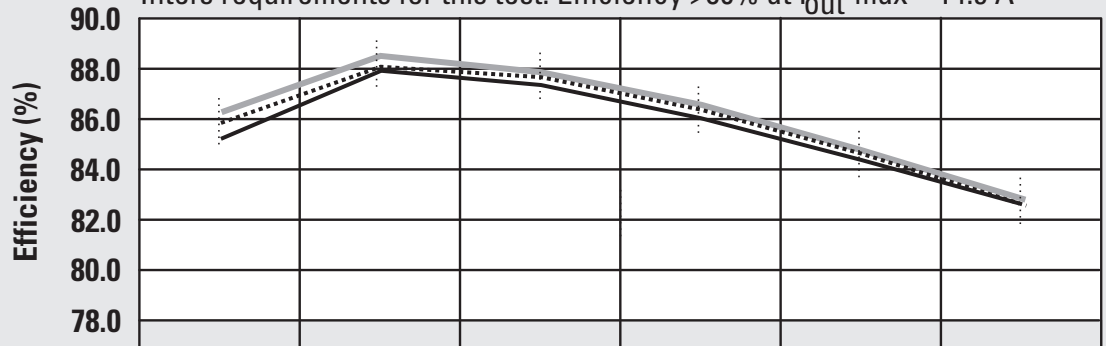
Figure 8. Efficiency (a) and power losses (b) over the entire input-voltage and output-current range after 12 hours of operation

SLVP147 EVM with TPS5210 controller

VID Code is set at 1.6 V Power losses 0.24 W from V_{cc} = 12 V are added.

Intel's requirements for this test: Efficiency >80% at I_{out} max = 14.5 A



	2.5	5	7.5	10	12.5	15
Vin = 4.5 V	86.5	88.8	88.1	86.8	85.0	83.0
Vin = 5 V	86.1	88.3	87.9	86.6	84.8	82.8
Vin = 5.5 V	85.4	88.1	87.6	86.2	84.6	82.8

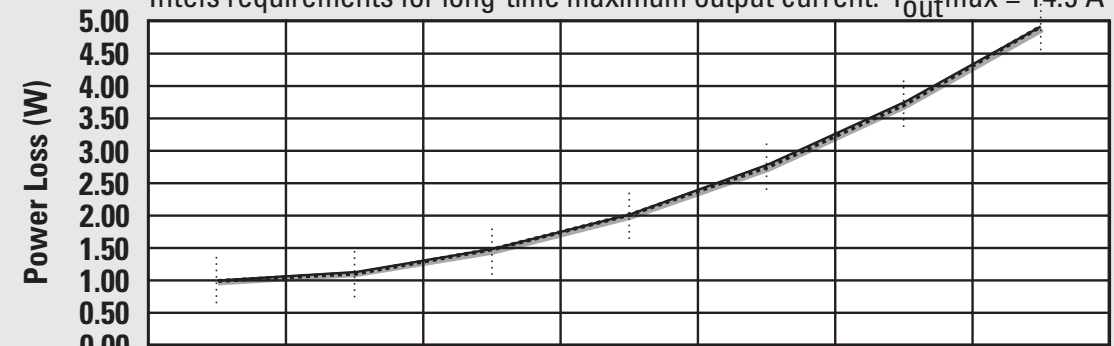
I_{out} (A)

(a)

SLVP147 EVM with TPS5210 controller

VID Code is set at 1.6 V Power losses 0.24 W from V_{cc} = 12 V are added.

Intel's requirements for long-time maximum output current: I_{out} max = 14.5 A



	0	2.5	5	7.5	10	12.5	15
Vin = 4.5 V	0.50	0.63	1.02	1.62	2.41	3.48	4.78
Vin = 5 V	0.53	0.65	1.06	1.65	2.45	3.51	4.85
Vin = 5.5 V	0.55	0.69	1.08	1.70	2.52	3.58	4.85

I_{out} (A)

(b)

The TPS5210 controller has an internal drive-voltage regulator with an 8-V output to decrease power losses in the drive circuitry. These power losses are only 0.24 W in this application. The drain-source voltage of the low-side FET and gate voltages of both FETs are shown in Figure 9.

It is very important to avoid shoot-through current through the power FETs in a synchronous buck converter. The shoot-through current significantly increases power losses and drops reliability. The TPS5210 has active dead-time control to avoid this problem. The waveforms in Figure 10 illustrate that there are optimum delays between turning off the FET and turning on the synchronous FET at all load-current conditions.

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Figure 9. The drain-source voltage of low-side FET and gate voltages of both FETs at V_{in} = 5 V, I_{out} = 18 A

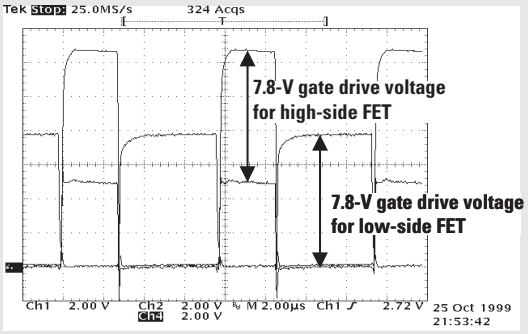
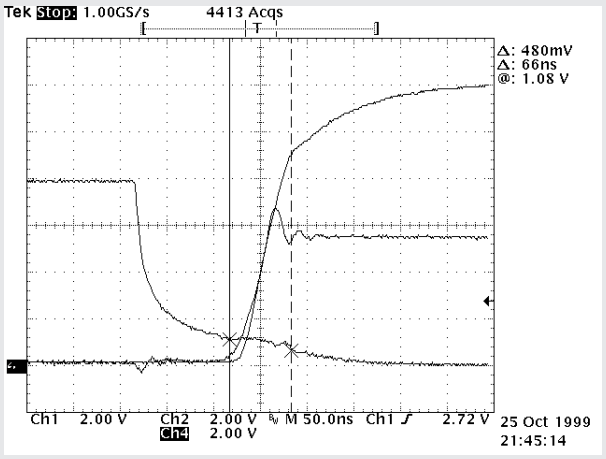
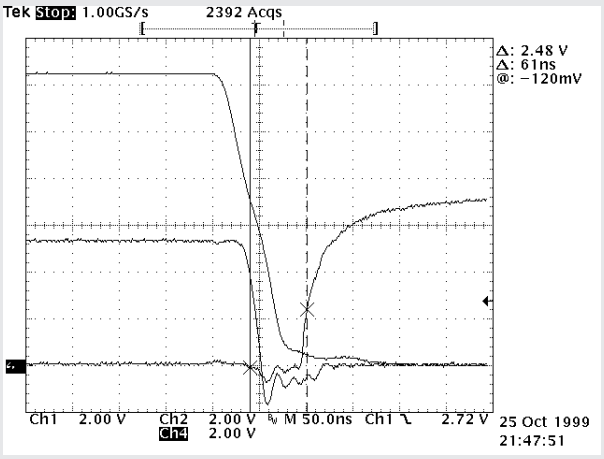


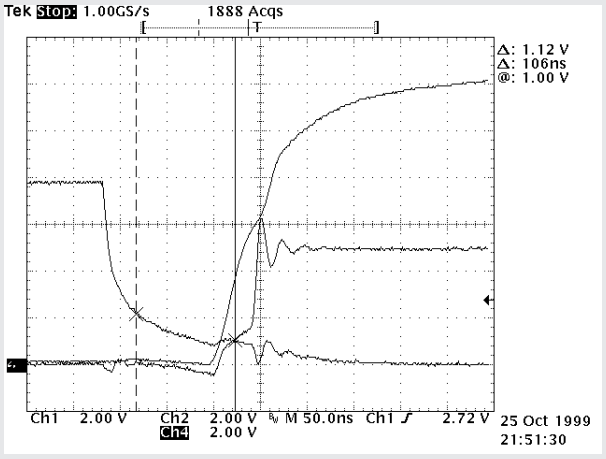
Figure 10. Switching waveforms at I_o = 0 A (a) and (b) and I_o = 18 A (c) and (d)



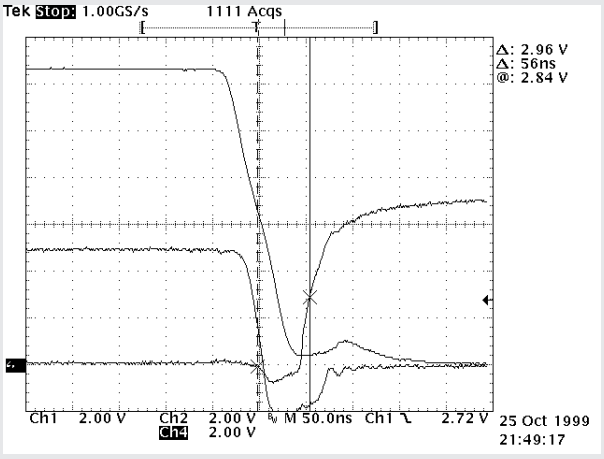
(a)



(b)



(c)



(d)

The cursors show the delay times.
(a) and (c): Low-side FET turns off, high-side FET turns on. (b) and (d): High-side FET turns off, low-side FET turns on.

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Start-up and relative overshoot

Start-up by applying 12-V V_{CC}, while the enable signal and 5-V input voltage are available, is shown in Figure 11a. Start-up by applying the enable signal, while the 5-V input voltage and 12-V V_{CC} are available, is represented in Figure 11b. The overshoot during start-up does not exceed 1.3%, which is well below the required 10%. The output-voltage rise time does not depend on the load current and has a linear ramp form. In this application, rise time was set at about 9 ms by the external capacitor.

Conclusions

- The SLVP147 evaluation module with the TPS5210 hysteretic controller meets the electrical specification of the Intel document "VRM 8.4 DC-DC Converter Design Guidelines."
- The hysteresis window, active droop, and output-voltage set point have been optimized for applications with over 733-MHz clock and 133-MHz bus-frequency Celeron-type processors.
- The load-current transient tests implemented in the EVM transient tester have shown excellent dynamic characteristics of the TPS5210 hysteretic controller for desktop applications using the minimum number of bulk OS-CON capacitors.
- The component temperature measurements in worst-case cooling conditions have given reasonable results.

References

For more information related to this article, visit the TI Web site at www.ti.com/ and look for the following materials by entering the TI literature number into the quick-search box. References without a TI literature number should be available through traditional publishing outlets.

Document Title	TI Lit. #
1. "TPS5210 Programmable Synchronous-Buck Regulator Controller," September 1998 revised May 1999	SLVS171A
2. "TPS5211 High Frequency Programmable Synchronous-Buck Regulator Controller," September 1999	SLVS243
3. "Designing Fast Response Synchronous Buck Regulator Using the TPS5210," Application Report, March 1999	SLVA044
4. "VRM 8.4 DC-DC Converter Design Guidelines," Intel Corporation, November 1999, order number 245335-001.	—
5. R. Miftakhutdinov, "Analysis of Synchronous Buck Converter with Hysteretic Controller at High Slew-Rate Load Current Transients," *Proc. of High Frequency Power Conversion Conference*, 1999, pp. 55-69.	—

Related Web sites

www.ti.com/sc/docs/products/msp/pwrmgmt/index.htm

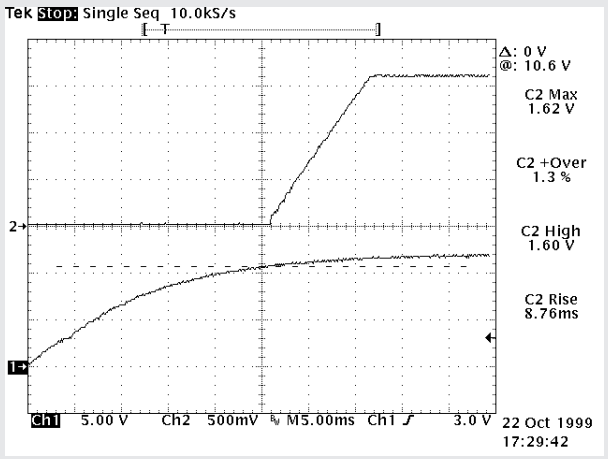
www.ti.com/sc/docs/tools/analog/powermanagementdevelopmentboards.html

Get product data sheets at:

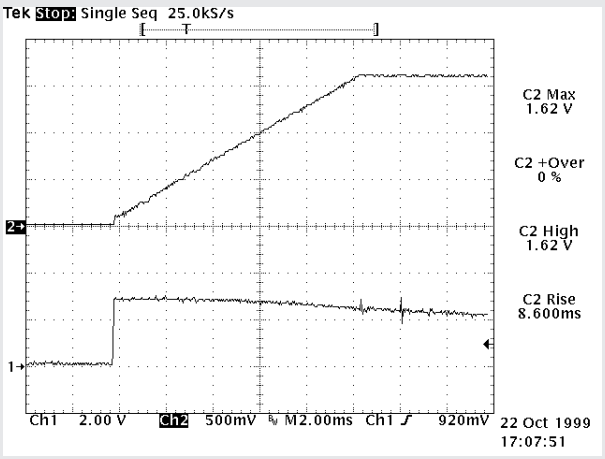
www.ti.com/sc/docs/products/analog/*device*.html
Replace *device* with tlc555, tps2812, tps5210, or tps5211

To order the TPS5210EVM-147 (SLVP147) evaluation module, call TI's toll-free order desk number at 1-800-477-8924, ext. 5800, in North America. To order in other regions, contact the TI Product Information Center for your region (see page 44) or contact your local TI distributor.

Figure 11. Start-up by applying V_{CC} voltage (a) and the enable signal (b)



(a)



(b)

The cursor shows the undervoltage lockout level.
(a): Ch1 shows V_{CC} voltage (5 V/div.), and Ch2 shows output voltage (0.5 V/div.).
(b): Ch1 shows the enable signal (2 V/div.), and Ch2 shows the output voltage (0.5 V/div.).

Skew definition and jitter analysis

By Steve Corrigan
System Specialist, Data Transmission

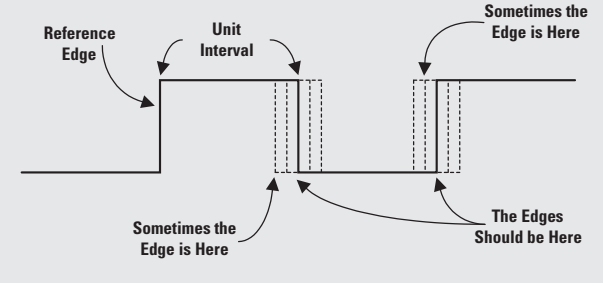
Over the past few years, jitter has become a signal property that many engineers take very seriously. Signal rise times are getting much shorter in high-speed digital systems, and slight variations in the timing of a rising or falling edge are more important with each additional Mbps. The phenomena of signal skew and data jitter in a waveform not only affect data integrity and set-up and hold times but magnify the signaling rate vs. transmission distance tradeoff, ultimately leaving a designer with a degraded system.

Although several standards clearly define various skews and jitters, no one definition can clarify the origins and contents of jitter in a measurement. JEDEC Standard 65 (EIA/JESD65) defines skew as "the magnitude of the time difference between two events that ideally would occur simultaneously" and explains jitter as the time deviation of a controlled edge from its nominal position. IEEE and the International Telecommunications Union (ITU) reinforce this time variation definition with similar discussions (see Figure 1). A more appropriate jitter definition would seem to be one for something called "jitter stew."

Jitter stew

Jitter can best be defined as the sum total of skews, reflections, pattern-dependent interference, propagation delays, and coupled noise that degrade signal quality. Jitter stew basically represents the portion of a unit interval (UI) during which a logic state should be considered indeterminate. The eye pattern is a useful tool for measuring overall signal quality. It includes all of the effects of systemic and random distortion and shows the time during which the signal may be considered valid. A typical eye pattern is illustrated in Figure 2 with the significant attributes identified.

Figure 1. Skewed edges



Several characteristics of the eye pattern indicate the quality of a signal. The height of the eye above or below the receiver threshold voltage level at the sampling instant is the noise margin of the system. Although jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal, jitter present at the receiver threshold voltage level measures the absolute jitter of the signal and is considered by some to be a more effective representation of the jitter applied to the input of a receiver. Jitter is typically given either in time as picoseconds or as a percentage of the UI. The UI or bit-length is the reciprocal value of the signaling rate; therefore, the time a logic state is valid is simply the UI minus the jitter. Percent jitter, which is the jitter time divided by the time of the UI and multiplied by 100, is more commonly used. Note how noise riding the signal levels in Figure 3 not only reduces the noise margin but

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Figure 2. Standard jitter measurement

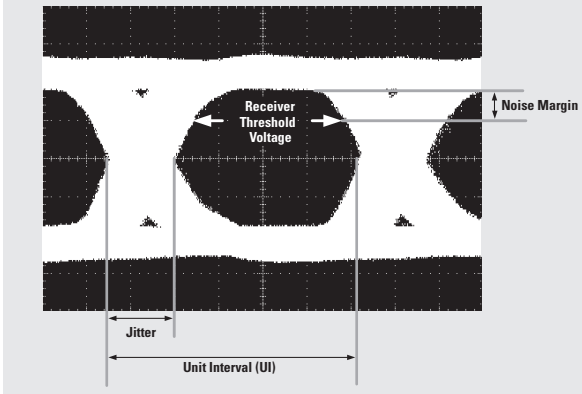
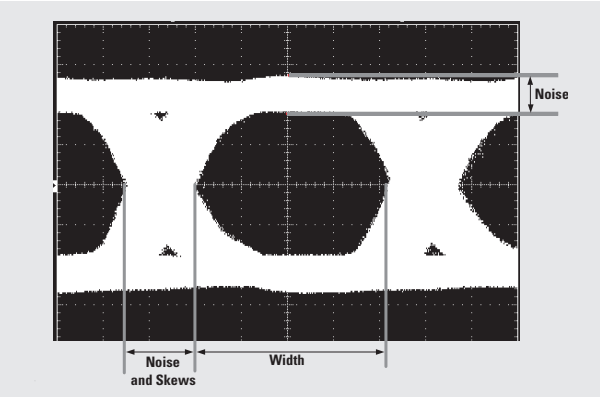


Figure 3. Noise and skews



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also becomes a primary ingredient of the jitter stew present in the eye pattern.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate reception, and lowering the height enters the input voltage threshold of a receiver.

Jitter ingredients

Noise may be coupled onto a signal from several sources and is not uniform at all frequencies. The more obvious noise sources are the components of a transmission circuit that include the signal transmitter, traces, cables, connectors, and receiver. Beyond that, there is a termination dependency, crosstalk, pattern-dependent inter-symbol interference, and V_{CC} and ground bounce.

Inter-symbol interference (ISI)

ISI is a leading cause of signal degradation. Signal attenuation and variations of signal rise and fall times combine to ultimately limit signaling rate and cable length. Figure 4 displays these effects on a signal caused just by the interplay of data patterns, rise times, and circuit impedance.

Typically referred to as pattern-dependent skew, these one-to-zero and zero-to-one voltage attenuation and propagation delays are only a few of the several jitter sources associated with a circuit component's frequency-dependent impedance. Line resistance, capacitance (mutual and ground), conductance, and inductance (series and mutual) interplay with a signal and adjacent signals at different frequencies depending on matters like slew rate, electrical environment, board layout, board composition, and connector and cable quality.

Reflections

Another of the major jitter ingredients results from signal reflections that radiate back and forth on a transmission line due to termination impedance mismatches that also exhibit frequency dependence. Even when a line is properly terminated with a value matching the characteristic impedance of the line, the "real" part of the impedance

Figure 5. Skew from unsymmetrical input-voltage levels

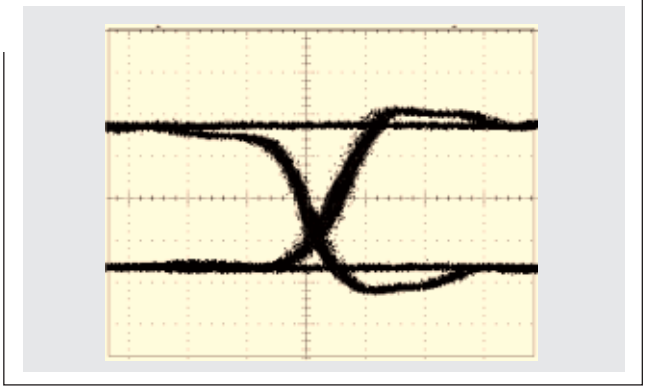
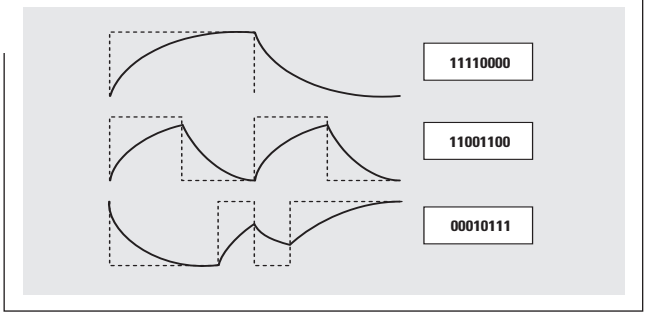


Figure 4. Pattern-dependent skew



actually changes with frequency as frequency-dependent parameters rise and fall in value.

Crosstalk

Crosstalk is jitter induced from the magnetic fields generated by nearby signals. It produces impedance changes in components, connectors, and transmission lines. If an adjacent signal is synchronous and in phase, these frequency-dependent effects may be greatly amplified. Once it is understood that the effective impedance of a circuit changes dramatically with frequency, the causes of jitter and skew are more readily understood. Aside from noise emanating from power supplies and ground, changes in circuit impedance are responsible for most of the jitter in data transmission circuits. The effective impedance of a circuit is a dynamic property not based solely on the physical properties of circuit components. Although skewed signals can result from something as simple as different transmission line lengths, many are the result of circuit component quality. For instance, adjoining signals in a multi-pair cable can arrive at the end of the cable at different times even if the lengths are equal. This time difference is defined as a cable's worst-case delay skew and is used as one of the indicators of cable quality.

Cycle-to-cycle jitter, $t_{jit(cc)}$

An extremely high skew condition occurs in any type of differential connection when the logic levels applied to a differential driver are not symmetrical about the driver's input-voltage trigger threshold—that is, an equal voltage magnitude above and below the trigger voltage. This threshold varies with frequency; therefore, a circuit designed for operation at a particular signaling rate may suffer a severe jitter increase if the signaling rate is changed.

If an input signal is biased equally above and below a driver's triggering threshold, the transition time of the signal to the trigger level is equal; therefore, the differential outputs trigger at the same time with each cycle. However, if the magnitude of the input signal is greater, either above or below the threshold, one cycle triggers earlier than the following cycle ($t_{cycle1} \neq t_{cycle2}$) and appears differentially as displayed in Figure 5. Therefore, $t_{jit(cc)} = | t_{cycle1} - t_{cycle2} |$.

Figure 6. Bank skew

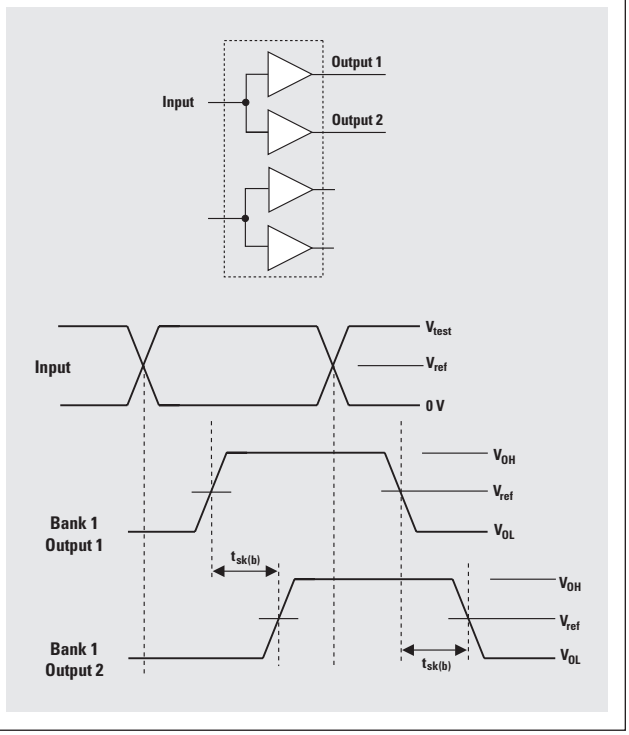
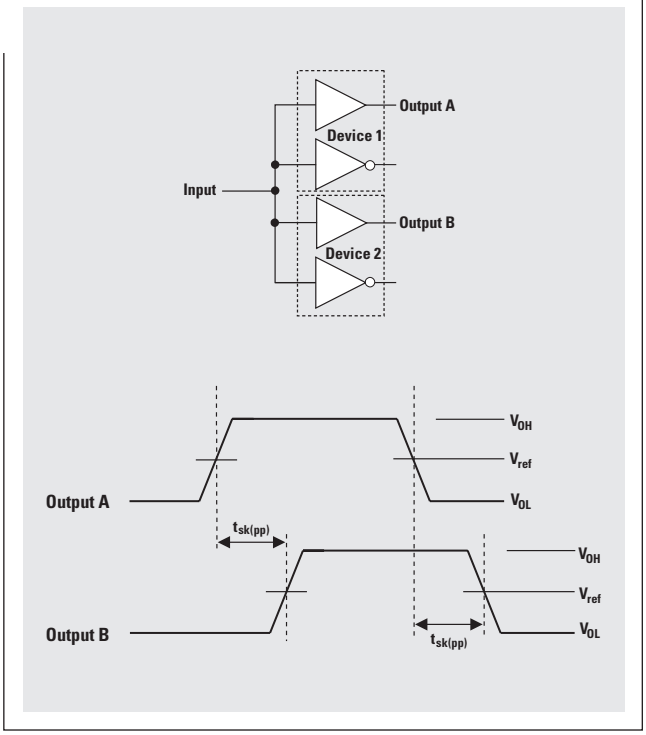


Figure 7. Part-to-part skew



Bank skew, $t_{sk(b)}$

Bank skew is the magnitude of the time difference between the outputs of a single device with a single driving input terminal.

Part-to-part skew, $t_{sk(pp)}$

Part-to-part skew is the magnitude of the difference in propagation delay times between any specified terminals of two separate devices when both devices operate at the same temperature with the same input signals and supply voltages, and have identical packages and test circuits.

Pulse skew, $t_{sk(p)}$

Pulse skew is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

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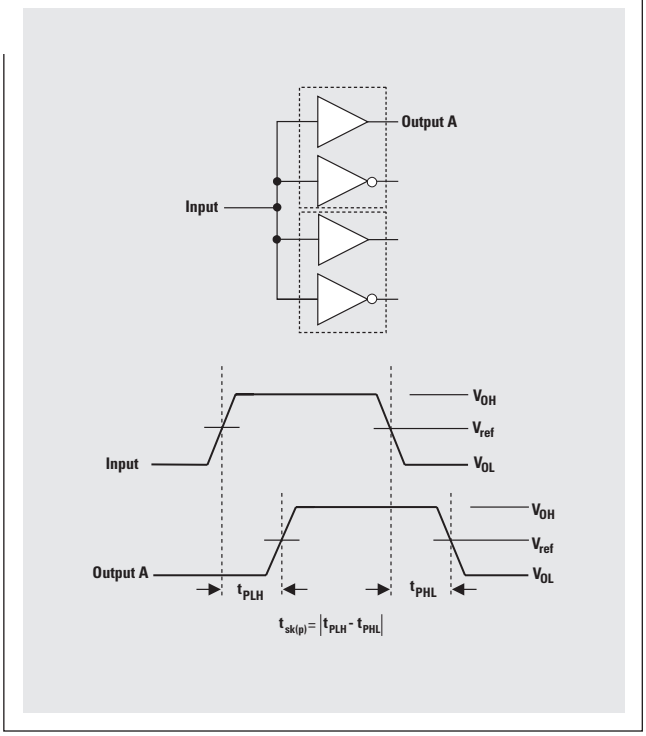
Figure 8. Pulse skew



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Output skew, $t_{sk(o)}$

Output skew is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

Jitter measurement test set-up

Figure 10 shows the circuit under consideration with the transmission line being probed at the output of both driver and receiver. First, the output of the HFS 9003 is applied directly to the input of the oscilloscope, and background noise is measured. This noise measurement, a function of the electrical environment that varies with each application, is subtracted from the overall jitter measurement. The Tektronix 784D is a digital phosphor oscilloscope (DPO), and its "infinite persistence" in DPO mode is employed for jitter measurement. Jitter is then easily measured with the cursors.

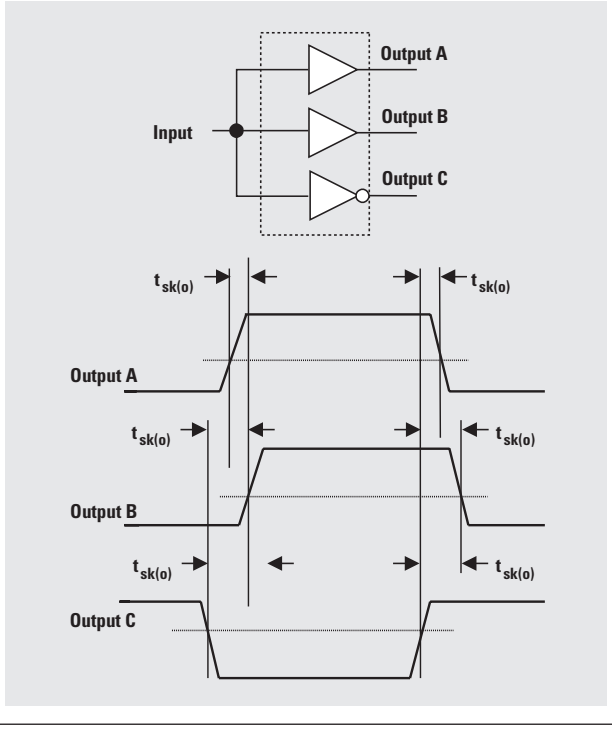
Test equipment

HP E3516A and HP 6236B DC power supplies provide the required supply voltage for the differential driver and receiver in the circuit. For the eye pattern jitter measurements, a Tektronix HFS9003 signal generator is employed as a non-return-to-zero (NRZ), pseudo-random binary sequence (PRBS) signal source for the driver and is adjusted as follows:

- Pattern: NRZ, PRBS
- Transition time: 800 ps
- Input voltage: Balance equally above and below driver threshold

At high signaling rates, the influence of equipment used to measure a signal of concern should be minimized. For differential tests, a Tektronix 784D oscilloscope and Tektronix P6247 differential probes are used. Each has a bandwidth of 1 GHz and a probe capacitance of less than 1 pF.

Figure 9. Output skew



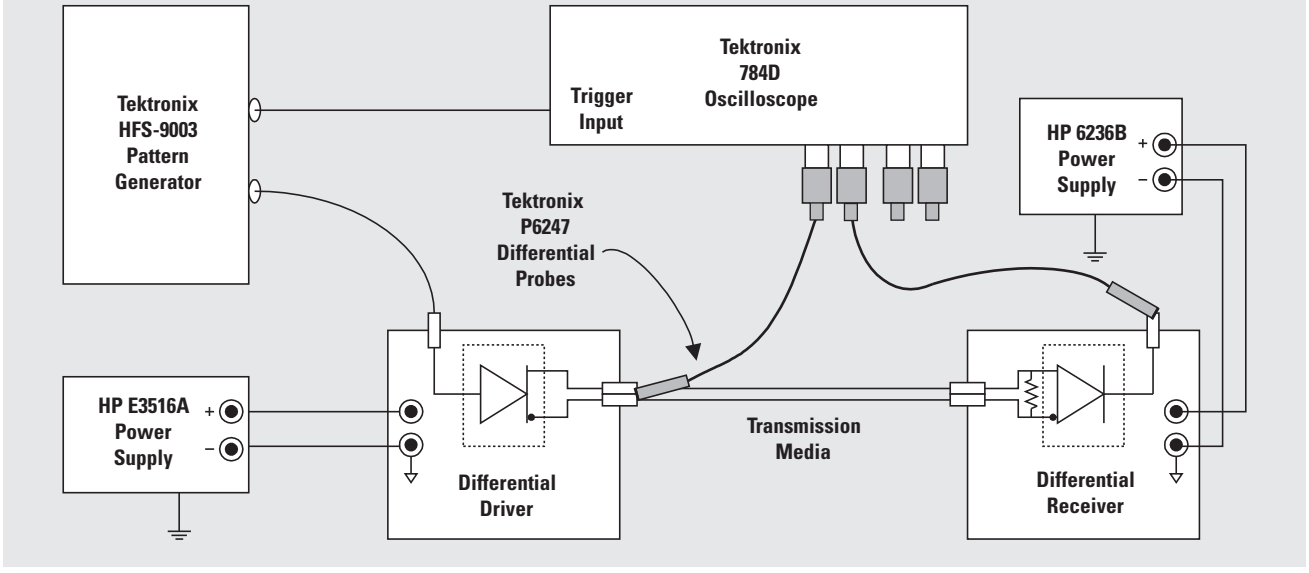
References

1. "EIA/JESD65, JEDEC Standard No. 65"
2. "IEEE Std 1596.3-1996"

Related Web site

www.ti.com/sc/docs/products/msp/intrface/index.htm

Figure 10. Jitter measurement set-up



LVDS receivers solve problems in non-LVDS applications

By E.D. Cole, P.E.
Application Engineer, Data Transmission

Introduction

This article describes how some of TI's customers have solved simple problems using LVDS receivers. They're just not using them with LVDS drivers!

Problem 1: "I don't want to put 5-V PECL in my box."

This customer was designing a small 3.3-VDC battery-powered subsystem. Unfortunately, he had to receive data being sent from a 5-VDC differential PECL driver. He did not want to have 5-VDC in his subsystem and was already looking for ways to reduce the 3.3-V power consumption to extend battery life. The subsystem used a "multi-drop" configuration with 8 loads.

The solution was remarkably simple. He installed 220-ohm series resistors on the differential PECL input lines and terminated the last receiver with 110 ohms. The PECL data was being received at 50 Mbps through 2 meters of CAT5 cable.

LVDS is often thought of as a high-speed device, but this customer knew it also consumed little power. He wasn't going fast, or far, but he needed to get as much done as possible on a single battery charge. He estimates that he doubled the "on" time using LVDS receivers.

Another customer presented a similar application that he had optimized for low power at 100 Mbps. He used the LVDS32A (the operative letter here is "A"), which has an increased input common-mode voltage (V_{ICM}) range. Using this feature allows the transmission line to be terminated "line-to-line" into 100 ohms and not referenced to ground. The '32A handles the 4.4-VDC PECL V_{ICM}, making a resistor divider unnecessary.

TI built up this second circuit in the lab and examined the eye pattern. As shown in Figure 3, the circuit performs extremely well at 100 Mbps. The top trace is the LVDS input to the receiver, and the bottom trace is the receiver output signal.

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Figure 1. 5-V PECL-to-3.3-V LVDS multi-drop data transmission system

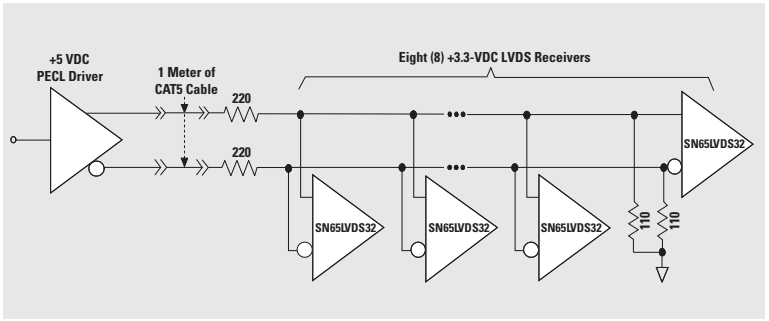


Figure 2. Optimized PECL-to-LVDS using an LVDS32A

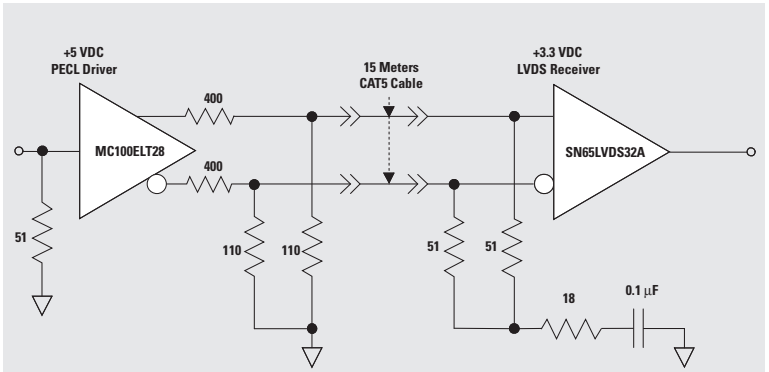
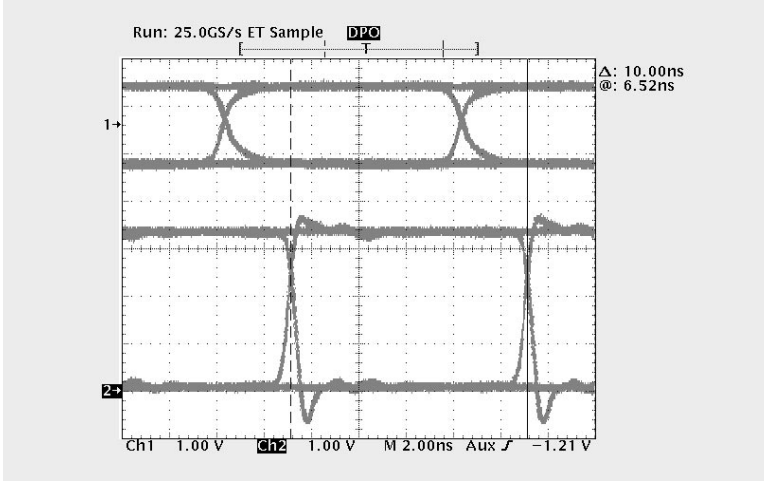


Figure 3. 5-V PECL-to-3.3-V LVDS at 100 Mbps across 15 meters of CAT5 cable



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It was obvious that the signaling rate could be increased, so this was run at 200 Mbps and 300 Mbps. The waveforms at 300 Mbps are presented in Figure 4. The top trace in Figure 4 is the input signal to the LVDS receiver. The bottom trace is the output of the LVDS32A receiver. The cable effects become evident at the higher signaling rates, and the signal degrades rapidly after 330 Mbps.

LVDS is used not only for high-speed but often for low-power applications as well.

Problem 2: "The output from my crystal doesn't look very good!" (or "My processor board seems to work better when the clock has edges.")

Another customer found that the output signal from his crystal oscillator needed to be "cleaned up" and distributed across a processor motherboard. His prior solutions had used a Schmitt trigger. Depending upon which oscillator he used, he sometimes used a transformer before the Schmitt trigger to boost and shift the input level to the Schmitt trigger. He had an unused receiver in a LVDM180 transceiver and now uses it to "clean up his clock," as shown in Figure 5.

This customer has several interesting LVDS applications on his processor board. This one caught the author's eye because it's so simple. The customer realized that an LVDS receiver is a very high-speed comparator, and that's exactly what he wanted. He said that this circuit gives him faster edges, uses less power, reduces his parts count, and is less expensive.

This circuit was tried in the lab with several different crystals (the author even tried it with an LC tank circuit). We found that R2 had to be replaced with a 10-kohm potentiometer because different oscillators had different output waveforms. Adjusting R2 made the duty cycle variable over a very wide range. Results obtained from a 100-MHz crystal are shown in Figure 6. The circuit was constructed with the crystal output connected to the inverting input pin on the LVDM180 (pin 11) instead of to the non-inverting input (pin 12).

If your CLK looks a little like a sine wave, give this a try. The author was impressed.

Problem 3: "Can I use LVDS to receive high-speed 5-V CMOS data?"

A customer asked if he could use LVDS to receive high-speed digital video through 10 meters of CAT5 cable. The driver was a single-ended, high-speed 5-V CMOS driver. He mentioned that the video was streaming at 300 Mbps. He did not know the specific part number of the driver, and he said he "could live with a few errors" since it was video.

One solution was to provide him with the schematic shown in Figure 7. The SN54AHC04 hex inverter was selected as the 5-V CMOS driver along with Belden's Mediatwist™ cable (because that's what was on hand). At 300 Mbps, impedances have to be matched, so the termination scheme was optimized to 100 ohms, and values were selected that would divide the input signal down to the nominal input range (V_{ICM} approximately 1.2 VDC) of the LVDS receiver. Note that this scheme creates the differential input at the receiver by bringing the driver

Figure 4. 5-V PECL-to-3.3-V LVDS32A at 300 Mbps across 15 meters of CAT5 cable

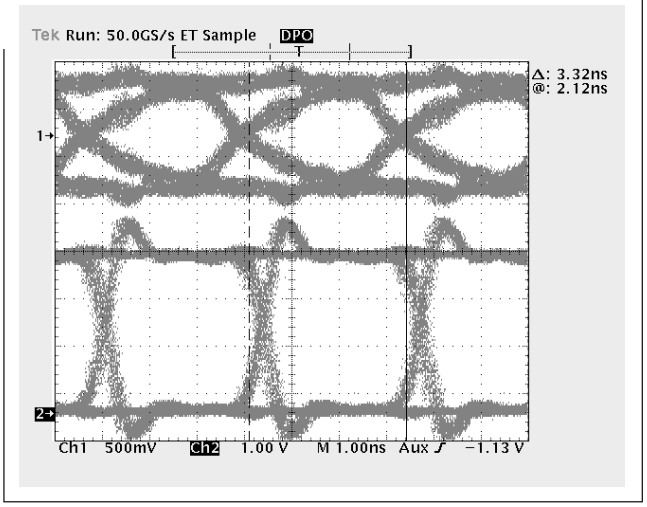


Figure 5. Using an LVDS receiver as a high-speed comparator

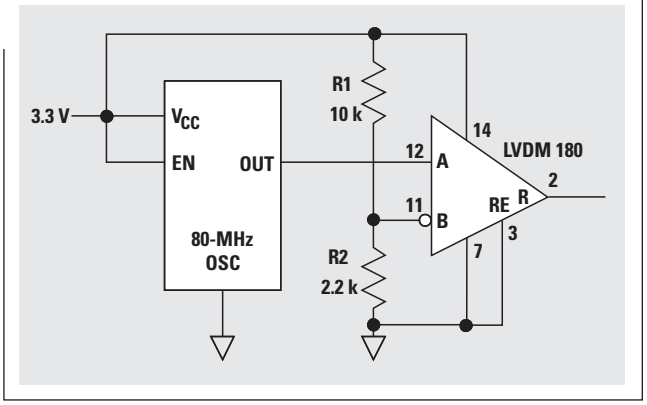
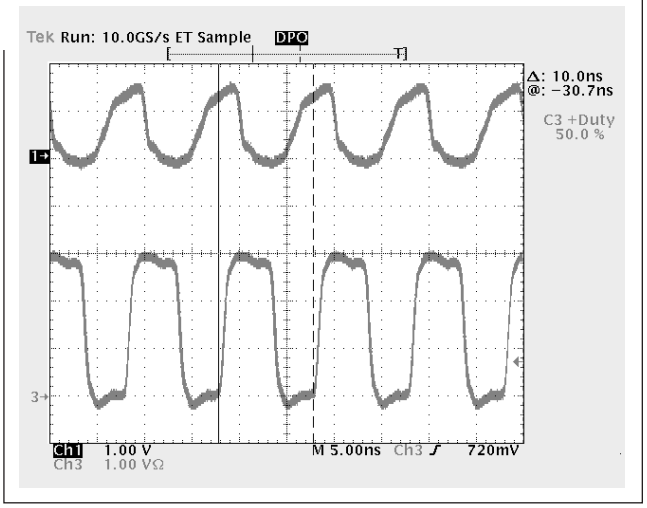


Figure 6. Using an LVDS receiver to improve the edges of an oscillator



ground through the cable. In the actual application, a system ground would be required between the driver supply and receiver supply to minimize any ground potential difference (V_{GPD}) between driver and receiver.

The waveforms shown in Figure 8 verify that the customer could use an LVDS receiver to receive his video data. The top waveform is the digital video signal at the input pin of the LVDS32. The bottom waveform is the output signal from the receiver.

The customer said he "could live with a few errors," so a bit-error-rate (BER) test was performed to see how fast this circuit would go before serious errors occurred. . The test set pattern generator in the BER tester can output only a maximum V_{IH} of 2.0 VDC, which would cause errors if the AHC04 V_{CC} remained at 5.0 V. Fortunately, the AHC04 inverter operates with V_{CC} = 2.5 V to 5 V, so V_{CC} was adjusted to 3.3 VDC, and the BER test was run with V_{IH} = 2.0 VDC and V_{IL} = 1.2 VDC. The test started at 400 Mbps, and the BER was recorded. The signaling rate was decreased in 10-Mbps steps, and the test was repeated. This process was continued until no errors were received at 340 Mbps. The BER results are shown in Figure 9.

The test continued to run, but at 350 Mbps the error rate was 10^{-13}, which equates to 1 bit error in every 10 trillion bits. This would be great since "it's just video." Also, the test time increases as the errors decrease. For example, at 300 Mbps it takes 9.25 hours to transmit 10 trillion (10^{13}) bits, so testing for error rates of 10^{-15} or 10^{-16} takes days to complete. But it's better now than it was—before LVDS, these BER tests were run at 50 Mbps and would take 23 days!

Figure 7. 5-V high-speed CMOS-to-LVDS receiver

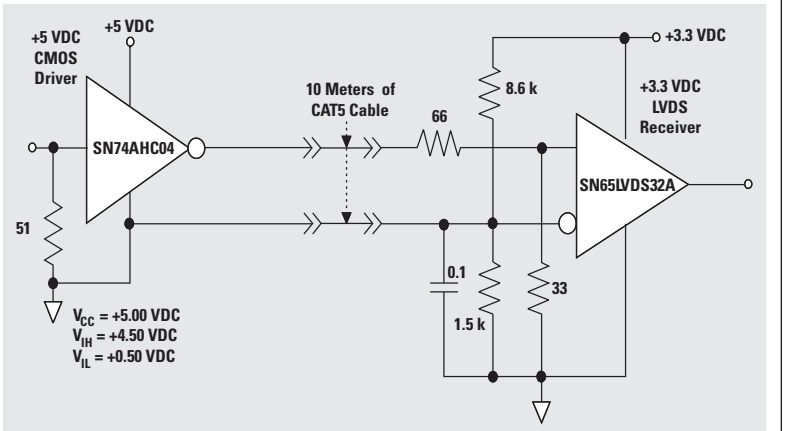
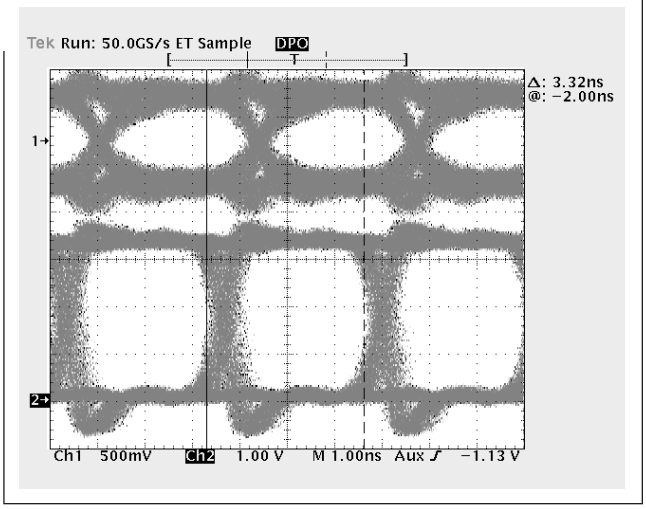


Figure 8. Single-ended 5-V CMOS driver into an LVDS receiver through 10 meters of CAT5 cable at 300 Mbps



Conclusion

This article has demonstrated that an LVDS driver does not always have to be connected to an LVDS receiver. The latter works quite well with other types of drivers, as these customers have demonstrated.

Related Web sites

www.ti.com/sc/docs/apps/analog/lvds_and_lvdm_general_purpose.html

www.ti.com/sc/docs/products/msp/intrface/index.htm

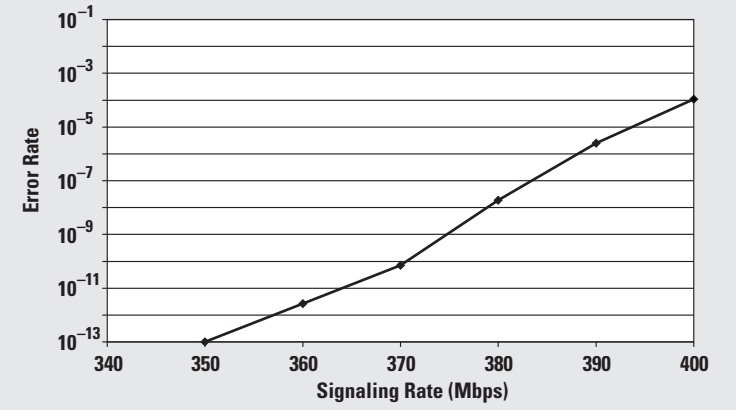
Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device*.html

Replace *device* with sn65lvdm180, sn65lvds31, or sn65lvds32a

www.ti.com/sc/docs/products/logic/sn54ahc04.html

Figure 9. Bit error rate vs. signaling rate



Matching operational amplifier bandwidth with applications

By Ron Mancini
Senior Application Specialist, Operational Amplifiers

Introduction

Selecting the correct op amp for an application requires investigation of many different parameters. Voltage offset, bias currents and similar parameters are easy to evaluate because they are DC parameters that do not vary with frequency. Accuracy, on the other hand, is hard to specify and comply with because it is a function of frequency; hence, accuracy specifications involve the knowledge of frequency-dependent feedback circuits that are bandwidth-dependent.

The bandwidth (BW) problem is complicated by the op amp's feedback because it hides decreasing BW until accuracy problems become apparent. If op amps had a constant open-loop gain, the accuracy of an op amp circuit would remain constant. The open-loop gain of any op amp decreases with increasing frequency. Except for a phenomenon called "peaking," all op amps lose accuracy at high frequencies. The designer's problem is selecting an op amp that has an acceptable accuracy loss at the frequencies of interest. Proper analysis of this problem requires an understanding of feedback, loop gain, and frequency dependence.

Preserving the signal integrity or accuracy during amplification is an essential part of the design, but in order to preserve the signal one must define the signal. Defining the signal sounds like a simple task, but it is complicated and must be performed in several different ways. Various methods used for defining the frequency content of the signal are examined in detail in this article because no single method works for every case.

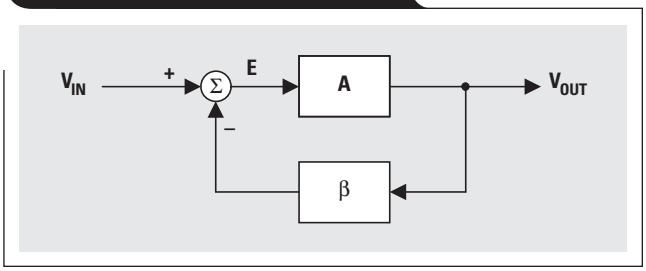
Feedback and accuracy

The basic feedback circuit is shown in Figure 1, where E is the error voltage, β is the feedback factor, and A is the forward gain. Equations 1 and 2 govern the circuit performance.

$$V_{OUT} = EA \quad \textbf{(1)}$$

$$E = V_{IN} - \beta V_{OUT} = V_{IN} - \beta EA \quad \textbf{(2)}$$

Figure 1. Basic feedback loop



The accuracy equation (Equation 3) is obtained by combining Equations 1 and 2.

$$\frac{E}{V_{IN}} = \frac{1}{1 + A\beta} \quad \textbf{(3)}$$

Equation 4, which is the circuit gain, is also obtained from Equations 1 and 2 and is shown for completeness.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad \textbf{(4)}$$

The quantity Aβ appears in both equations and is called loop gain because it has a special significance in feedback circuits. The loop gain determines the stability of a feedback circuit as shown in Equation 4 (instability occurs when $A\beta = -1$), and it determines the accuracy as shown in Equation 3. Accuracy and stability are inversely related—i.e., stability decreases as accuracy increases, and vice versa. The loop gain is calculated with the voltage inputs grounded (current inputs open), so the input signal and position (plus or minus input) have no effect on the loop gain. This means that the loop gain for a noninverting, inverting, or differential op amp is the same. Three op amp circuits are shown in Figure 2, and the loop gain for all circuits is given in Equation 5.

$$A\beta = \frac{aR_G}{R_F + R_G} \quad \textbf{(5)}$$

The parameter "a" is the open-loop gain of the op amp, and it is often confused with the forward gain, "A." The op amp open-loop gain decreases with frequency, hence the error increases with frequency, as Equation 3 illustrates.

A more in-depth analysis of stability and feedback is found in References 1, 2, and 3.

Defining a signal to determine its BW

The simplest case exists when the amplifier circuit specifications are included in the system specifications or given to the amplifier designer. A good amplifier specification shows the low-frequency gain at one frequency and the high-frequency gain at a second frequency. Sometimes the rate of the gain decrease (gain roll-off) is specified in dB/decade.

When a complex signal is applied to the amplifier input, and only a distortion or fidelity specification is given, the systems designer has passed the signal definition problem to the circuit designer. The circuit designer must determine what portion of the signal can be sacrificed because of loop gain reduction ("a" decreases with frequency) while meeting the distortion or fidelity specification. The first step in this procedure is to divide the signal into segments and analyze each segment using a Fourier series. An arbitrary maximum frequency is chosen; frequencies exceeding the maximum frequency are discarded, and the signal is reconstructed from the remnants. If the signal meets the specification,

the maximum frequency equals the BW requirement. If the signal does not meet the specification, a new maximum frequency is chosen and this procedure is repeated until the required distortion or fidelity specification is met.

Computer programs best implement the Fourier series procedure, but the procedure is complicated and laborious, so many engineers take the easy path of looking at test results. It is common for engineers to use the video screen or data error rate to evaluate amplifiers. They will solder the test units into working circuit boards and evaluate the video op amp performance by observing the screen. Likewise, data transmission amplifiers are often evaluated by in-circuit testing. The Fourier procedure must be used in many designs because in-circuit testing does not allow for manufacturing tolerances, it is not as accurate as the Fourier procedure, and it is hard to use where the results are not easily observable.

At this point it may seem that the easiest and safest path is to select an op amp with a BW much larger than required, but that isn't an option in most cases because extra BW is costly and amplifies noise. The extra cost is prohibitive in multiple op amp or high-volume applications; thus, in-circuit testing or Fourier series analysis is used to evaluate the BW requirements of op amps. Extra BW can't multiply the signal, and "Murphy's Law" guarantees that it will multiply noise. When the only op amp that fits the BW requirement has extra BW, the designer should consider putting a passive filter in the signal chain to limit the noise passed by the system.

There is an extra requirement imposed on op amps that are used in active filter circuits. These op amps must have adequate BW to support the signal and to function as an active filter at noise frequencies. Often active filter op amps have their BW set by the noise frequencies rather than by the signal frequencies. Circuit designers must predict the highest noise frequency by calculation, measurement, or experience if they want to design good workable filters.

Voltage feedback op amps

The gain versus frequency plot of a typical voltage feedback amplifier (VFA) is shown in Figure 3. The loop gain-plus-one separates the closed-loop gain and forward gain plots. The closed-loop gain is down 3 dB at the intersection point. The loop gain decreases at –20 dB/decade beginning at low frequencies. The error increases as the frequency increases.

The open-loop gain plot of the TLV2472 is shown in Figure 4. This plot defines the op amp open-loop gain, "a," which is not necessarily the forward gain, "A." The error equation for the op amp circuits shown in Figure 2 is given in Equation 6.

$$\frac{E}{V_{IN}} = \frac{1}{1+A\beta} = \frac{1}{1+\frac{aR_G}{R_F+R_G}} \qquad (6)$$

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Figure 2. Op amp circuits

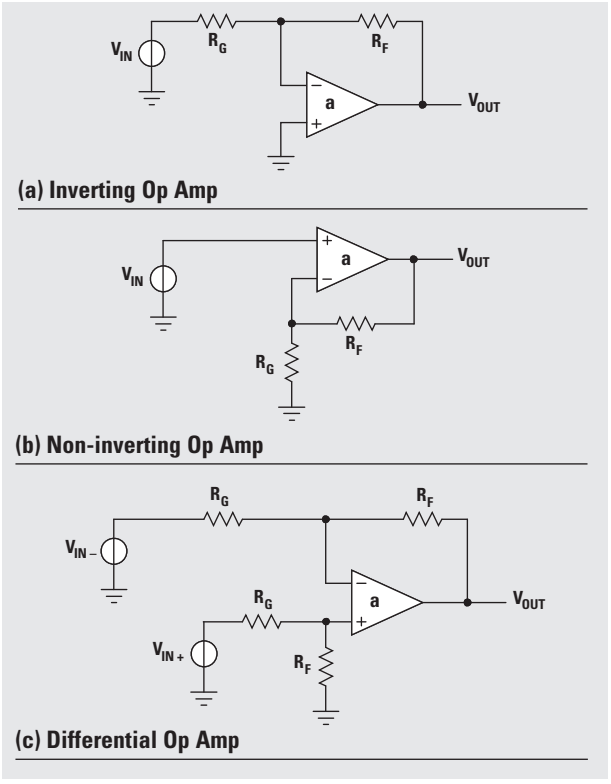


Figure 3. Plot of op amp equation

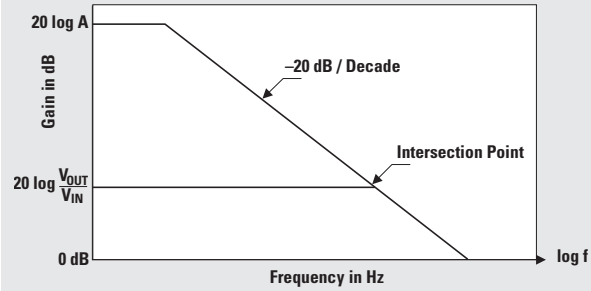
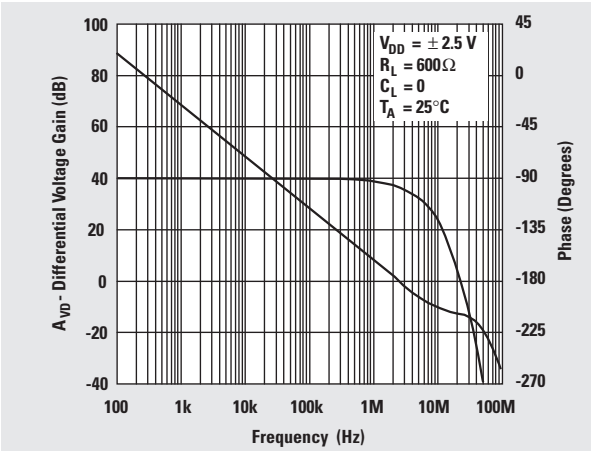


Figure 4. Open-loop gain plot of the TLV247x



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The loop gain equation contains the closed-loop gain equation; thus, the error is dependent on the closed-loop gain and the amplifier frequency response.

For a non-inverting circuit with a closed-loop gain of 2 (6 dB), the open-loop gain is approximately 61 dB at 1 kHz; therefore, the non-inverting circuit built with a TLV2472 op amp has about 0.18% error at 1 kHz. For a non-inverting circuit with a closed-loop gain of 10 (20 dB), the open-loop gain is approximately 43 dB at 1 kHz; therefore, the non-inverting circuit built with a TLV2472 op amp has about 7.9% error at 1 kHz.

For an inverting circuit with a closed-loop gain of 2 (6 dB), the open-loop gain is approximately 61 dB at 1 kHz; therefore, the non-inverting circuit built with a TLV2472 op amp has about 0.26% error at 1 kHz. For a non-inverting circuit with a closed-loop gain of 10 (20 dB), the open-loop gain is approximately 43 dB at 1 kHz; therefore, the non-inverting circuit built with a TLV2472 op amp has about 8.7% error at 1 kHz.

Although the advertised gain-BW product of the TLV2472 is 2.8 MHz, circuits built with this IC can show gain errors at much lower frequencies because the amplifier gain starts falling off at much lower frequencies.

Current feedback op amps

The loop gain for a current feedback amplifier (CFA) is given in Equation 7, where Z is the transimpedance (sometimes called transresistance) and Z_B is the input buffer's output impedance. Z functions in a CFA like the amplifier gain, "a," does in a VFA. Both are very large quantities, so they are very hard to measure. Transimpedance measurements must be made at very high frequencies and in the presence of noise, so many manufacturers do not include transimpedance plots in their data sheets.

$$A\beta = \frac{Z}{R_F\left(1+\frac{Z_B}{R_F+R_G}\right)} \quad \textbf{(7)}$$

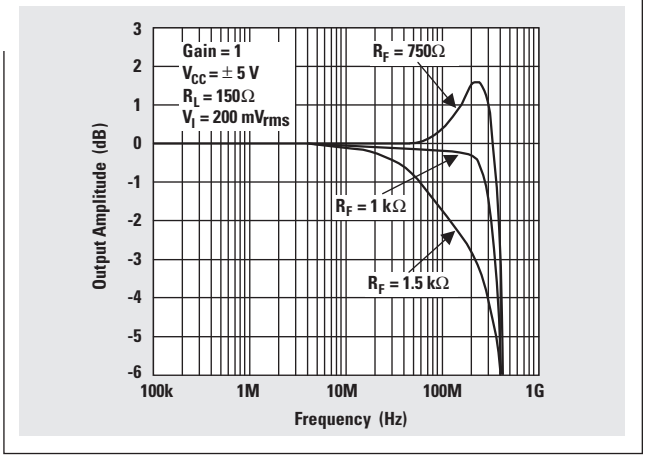
The input buffer's output impedance is made very small by design, and when it is neglected, Equation 8 results.

$$A\beta = \frac{Z}{R_F} \quad \textbf{(8)}$$

The closed-loop gain is not contained in the loop gain; thus, the CFA BW and error are independent of closed-loop gain. The manufacturer seldom plots the transimpedance, hence open-loop gain plots cannot be used to calculate the error. The manufacturers do plot amplitude versus frequency as a function of feedback resistance, supply voltage, and closed-loop gain. These plots are used to determine the accuracy of the circuit.

Figure 5 is the closed-loop response plot of the THS3001; notice that the response can be peaked, flat, or rolled off. The peaked response (R_F = 750 Ω) creates distortion in a perfect signal because it emphasizes the high-frequency components in the signal. Sometimes the peaked response is chosen because it compensates for high-frequency gain lost due to stray capacitances or cables. Some CFAs have external leads that enable peaking control so that the overall response can be made flat.

Figure 5. Closed-loop response plot of the THS3001



The rolled-off response (R_F = 1.5 kΩ) is used only when a less expensive op amp having the correct BW can't be found. When the signal requires a 10-MHz BW, and a lower-cost op amp can't be found, the designer often makes R_F = 1.5 kΩ or slightly more to roll off the gain so that the circuit cannot amplify high-frequency noise. The R_F = 1 kΩ response is usually chosen because it amplifies the signal with the best fidelity.

Conclusions

Determining the amplifier's required BW can be as simple as in-circuit testing or as complicated as using Fourier series analysis. The VFA loop gain contains the closed-loop gain; thus, the error is related to the closed-loop gain and amplifier frequency response. Selecting the proper BW VFA consists of using the op amp open-loop gain plot to calculate the error at the operating frequency. Selecting the proper CFA consists of reviewing the closed-loop gain plots and calculating the error based on these plots. In either case, excess BW is detrimental to good circuit performance because it contributes to instability, increases cost, and amplifies noise.

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For more information related to this article, visit the TI Web site at www.ti.com/ and look for the following materials by entering the TI literature number into the quick-search box.

Document Title	TI Lit. #
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2. "Stability Analysis of Voltage Feedback Op Amps, Including Compensation Techniques"	SLOA020
3. "Current Feedback Amplifier Analysis and Compensation"	SLOA021

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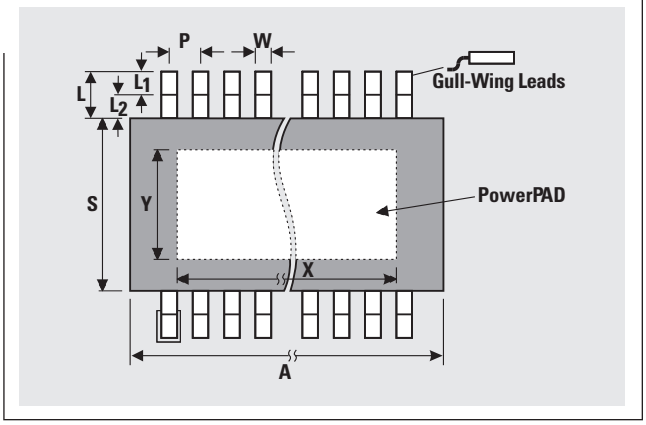
Replace *device* with ths3001 or tlv2472

PCB layout for the TPA005D1x and TPA032D0x Class-D APAs

By Richard Palmer
Application Specialist, Audio Amplifiers

Following good, sensible printed circuit board (PCB) layout practices will ensure peak performance and reliability from Class-D audio power amplifiers. A good thermal and mechanical bond between the device pins and PowerPAD™ and the PCB landings (pads) will provide the necessary electrical and thermal pathways for the amplifier to operate efficiently and dissipate the heat generated during peak operation. This can be achieved with an understanding of the basic manufacturing process and a proper layout of the IC and PowerPAD footprint. Once the device is in place, the power and ground connections must be made. A solid ground plane is recommended when possible as it provides a low-impedance ground return path, connects to the device PowerPAD to serve as a heat sink, and reduces crosstalk between channels. Routing and decoupling of the power traces provides the proper paths for return currents and minimizes the fluctuations of the voltage at the power pins. The routing of the signal path wraps up the device layout, with only a few sensitive nodes in the Class-D and headphone amplifier circuits to consider. Some miscellaneous considerations, when employed, will improve the quality of the end product and facilitate the production of the circuit, improving reliability and providing a much less stressful environment for the engineer and PCB manufacturer.

Figure 1. 48-pin HTSSOP package



PCB footprint for the device

The TI TPA005D1x and TPA032D0x Class-D devices come in the 48-pin HTSSOP (TSSOP with a PowerPAD) package. A small portion of the package is shown in Figure 1, with the maximum and minimum lengths for the dimensions provided in Table 1 in both millimeters (mm) and thousandths of an inch (mils). The PowerPAD is a leadframe die pad located on the bottom of the package that serves as a thermal path between the silicon die of the amplifier and the ground plane of the PCB.[1] It is approximately 5.4 mm (210 mils) long and 2.3 mm (90 mils) wide and is centered on the bottom of the package. The device pins are bent downward in what is called a "gull wing" shape and have a constant pitch of 0.5 mm (19.7 mils).

Continued on next page

Table 1. Dimensions of the device and PCB footprint for the 48-pin HTSSOP package

ITEM	MEASUREMENT	SYMBOL**	DIMENSIONS*			
			MAXIMUM		MINIMUM	
			(mm)	(mils)	(mm)	(mils)
HTSSOP package (Figure 1)	Pitch, IC pins	P	0.5	19.7	0.5	19.7
	Width, IC pins	W	0.27	10.6	0.17	6.7
	Length, IC pin	L	1.05	42	0.95	37.4
	Length, IC pin, package to foot	L_2	0.55	21.7	0.2	7.8
	Length, IC pin, foot	L_1	0.75	29.5	0.5	19.7
	Width, package	S	6.2	244	6.0	23.6
	Length, package	A	12.6	496	12.4	488
	Width, PowerPAD	Y	2.3	90	N/A	N/A
	Length, PowerPAD	X	5.45	215	N/A	N/A
PCB footprint (Figure 2)	Pitch, pin lands	P_1	0.5	19.7	0.5	19.7
	Width, pin lands	W_1	0.32	12.7	0.25	9.8
	Length, pin lands	L_3	0.75	29.5	0.56	22
	Spacing, pin lands	S_1	6.75	266	6.2	244
	Width, PowerPAD land	Y_1	3.2	126	2.3	90
	Length, PowerPAD land	X_1	6.35	250	5.85	230

*Dimensions are in millimeters (mm) and thousandths of an inch (mils). 1 mil = 0.001 inch.
**See Figures 1 and 2.

Continued from previous page

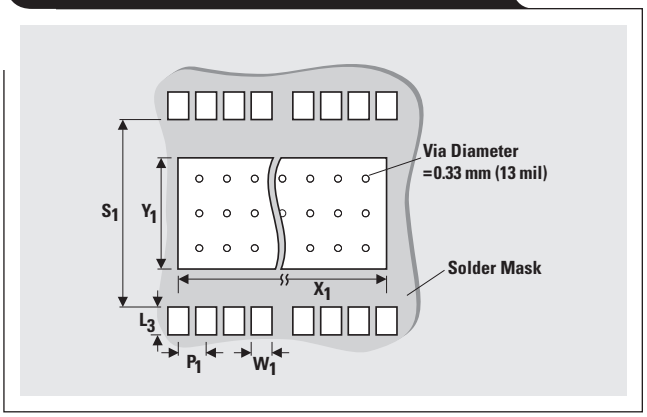
Figure 2 shows the pattern of IC pin and PowerPAD landings, called the IC footprint. These are the PCB pads that have been effectively used on the Class-D evaluation module (EVM). The PCB pad that serves as the landing for the PowerPAD should be at least the same size as the PowerPAD, but can be larger. If it is larger, the excess copper should be covered with solder mask to prevent wicking of the solder away from the PowerPAD area during assembly. The number of vias to be placed within the landing directly under the PowerPAD is determined by looking up the particular package in the *Package Outlines Reference Guide*.[2] In this case it is 21 vias spaced evenly in 3 rows of 7 vias each. These vias should be 13 mils in diameter to allow solder to be wicked into them during assembly. This serves two purposes: It vents out any air or gases that may otherwise be trapped under the package and form bubbles that reduce the contact between the PowerPAD and ground plane, potentially limiting the heat transfer; and it completely fills the vias, increasing some of the heat transfer to the ground plane. Since these vias are connected directly to a large ground plane, thermal relief such as webs or spokes should not be used. The idea is to draw the heat out, not keep it in. Additional, larger vias may be placed outside of the PowerPAD area and are not restricted to 13 mils.

Experimentation has revealed that during the assembly process, a solder paste stencil that is 6 mils thick and covers approximately 60% of the PowerPAD landing area (for a landing that is 125 mils by 250 mils) and 90% of each of the landings of the surface mount components creates an effective contact between the PowerPAD, IC pins, components and the PCB landings during the solder reflow process. Figure 1 does not show that the seating plane (distance between the foot of the IC pins and the bottom of the package) will be approximately 3 mils and that the package is approximately 43 mils in total height. The assembly, if automated, should be programmed such that it will not press down on the package too far, displacing the solder paste for the PowerPAD and possibly bending the leads.

The PCB landings for the amplifier pins should meet the minimum guidelines as set forth by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) in the standard IPC-A-610[3] and as derived from the standard IPC-SM-782.[4] According to IPC-A-610, the IC pin may overhang the PCB land, both to the sides and toward the outside edge of the pads, as long as there is proper solder wetting evident on the heel and the side contacting the pad. This is acceptable because the solder is present mainly to form a mechanical bond between the PCB and the device rather than as a conductive path for current flow. Such requirements set the minimum, and the current manufacturing techniques set the maximum, size of the footprint for the device as shown in Table 1.

During the reflow soldering process, the PowerPAD landing on the PCB acts as a heat source due to the large amount of copper attached to it. This heat source will draw, or wick, toward the center of the device footprint any solder that is on the traces or landings of nearby IC pins or components. This reduces the solder available to form the joint between the IC pins and the corresponding PCB landings and can be a real problem when a high-current

Figure 2. 48-pin HTSSOP land pattern



pin is involved. A smaller joint means greater resistance and therefore more power dissipated in the joint, and this can quickly cause the connection to fail as it is heated and reheated during repeated use.

Several steps can be taken to ensure that a good solder joint is made.

First, ensure that each landing is isolated from adjacent landings through the use of a pocket-type solder mask window rather than a gang window. A pocket window is where the mask completely surrounds each pad, effectively creating a pocket (see Figure 2). This should be done even if two pads are electrically connected to ensure that the solder properly wicks onto each pin of the device. Photo-imaged solder masks now allow solder mask back-off (swell)—the distance the mask must be from the edge of the copper to avoid bleeding onto the landing—of as little as 1 mil and mask thickness between lands of 3 mils. This type of mask leaves no residue on the surface of the lands and traces.

Second, cover the traces that connect to a pad with solder mask, especially if they extend under the chip toward the PowerPAD. This is especially true if these traces terminate at the other end in a via or pad for another component. The solder paste stencil will cover all the areas that are exposed with solder, and the mask will reduce the chance of a solder bridge forming or solder migrating down the trace away from the desired location. A swell of 1 mil can be used here also.

Third, provide directions in a text file to the PCB manufacturer that indicate the desired swell, paste stencil thickness, and area of coverage for each location (such as 90% for components, 60% on the PowerPAD). This will prevent errors introduced by the manufacturer applying "good manufacturing practices" and resetting the swell to a 15-mil back-off, which could prove troublesome.

Power and ground connections

The TPA005D1x and TPA032D0x devices all have the same general power and ground structure. The amplifier is divided into three major sections: analog circuits, power output circuit, and charge-pump/headphone circuit. Figure 3 shows a general schematic for the Class-D audio power amplifiers that may vary slightly from device to device. The upper portion of the IC contains the sensitive analog circuits for the device. The powerful H-bridge output

section is located in the middle, and the lower section consists of the charge-pump circuit for Class-D mode of operation and the headphone circuit for Class-AB mode of operation. The figure clearly shows how the ground plane should be subdivided to minimize ground loops.

The analog circuit ground is pin 47, and all the analog section capacitors and grounds should terminate as close to this pin as possible. The charge-pump and headphone circuits are not operational at the same time and thus are considered one section. Their ground pins (27 and 20, respectively) can each be considered ground for this section. The power circuit grounds are pins 12 and 13 for the left channel and pins 36 and 37 for the right channel. It is particularly important to terminate the decoupling capacitors of the power section close to these grounds and have the ground plane close to and along the entire length of the power input traces for return currents to flow back easily to the power source. This is also true for the analog input section since it has an outside source supplying the signal. The same holds true for the power pins of each of the other amplifier sections.

It is a simple matter to keep these three grounds separated when multi-layer PCBs are used for the circuit. Single-layer PCBs represent a different challenge. In this case, be sure to keep the ground return paths and ground loops of the analog section out of the path of the other two sections, primarily the output section. High currents flow through the output traces and should have a path for easy flow of the return currents. Placing the ground plane underneath these traces or alongside them will provide such a path. Figure 4 illustrates how the ground loops and return currents flow in the ground plane.

The headphone section is not as critical since it is inactive when the Class-D circuit is active. The same considerations for current return paths and ground loops still apply, however, in order to keep distortion in the circuit to a minimum.

The actual ground area should be as large as possible, no matter how many layers the PCB has. This will reduce the trace inductance of the ground plane, reducing the disturbances between amplifier sections created by current flow. The large area of the ground plane also acts as a heat sink for the device. The area required will depend upon the application and the desired thermal resistance from the sink (ground plane) to the ambient (θsa).

Sensitive nodes

All sensitive nodes for the amplifier are shown as bold lines in Figure 3. The most sensitive nodes in the Class-D circuit are the amplifier inputs and outputs. The inputs are AC coupled, and any trace between the input of the amplifier and the capacitor acts as an antenna, picking up any radiated signals that are then increased by the total gain of the audio amplifier. These capacitors should be placed as close as possible to the input pins.

The inductors in the output filter should be placed as close as possible to the IC to reduce any radiated emissions

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Figure 3. TPA032D04 Class-D audio power amplifier circuit

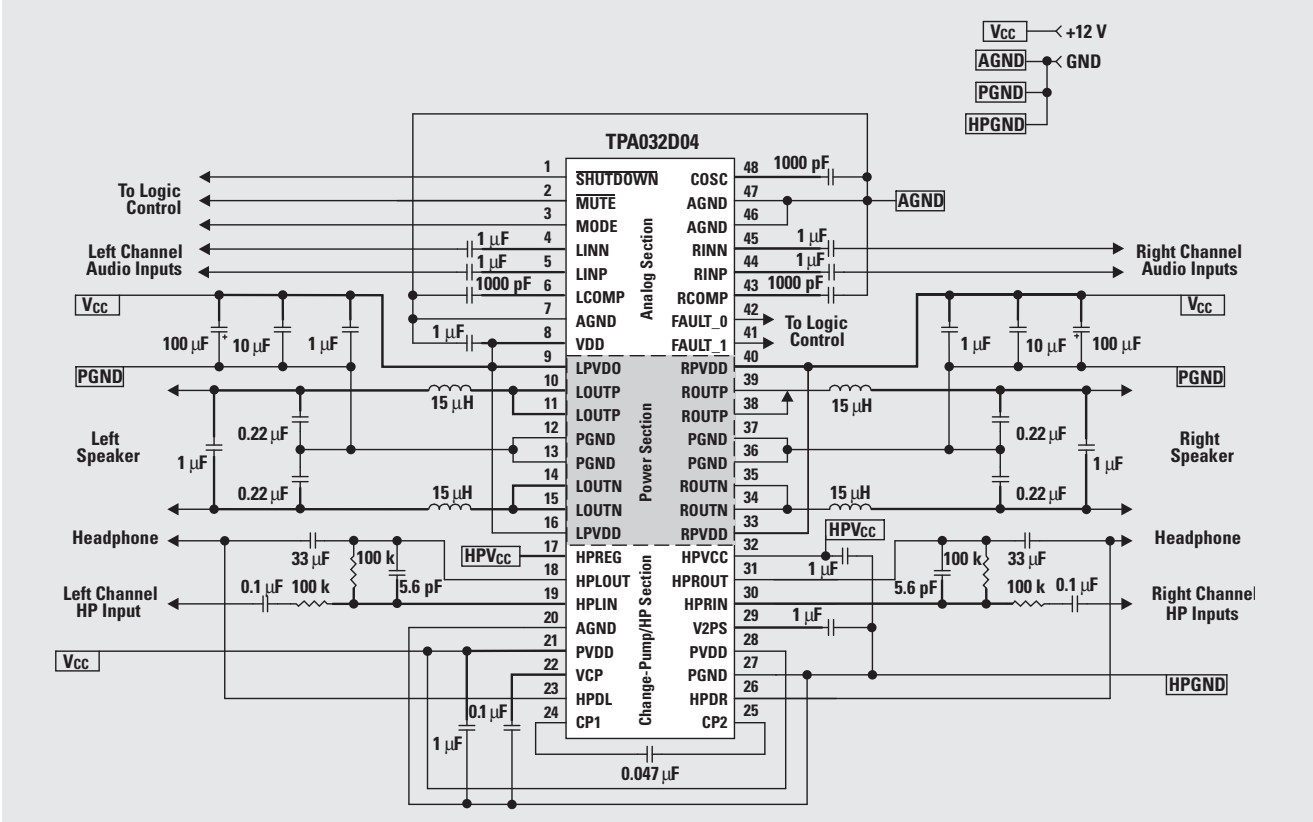

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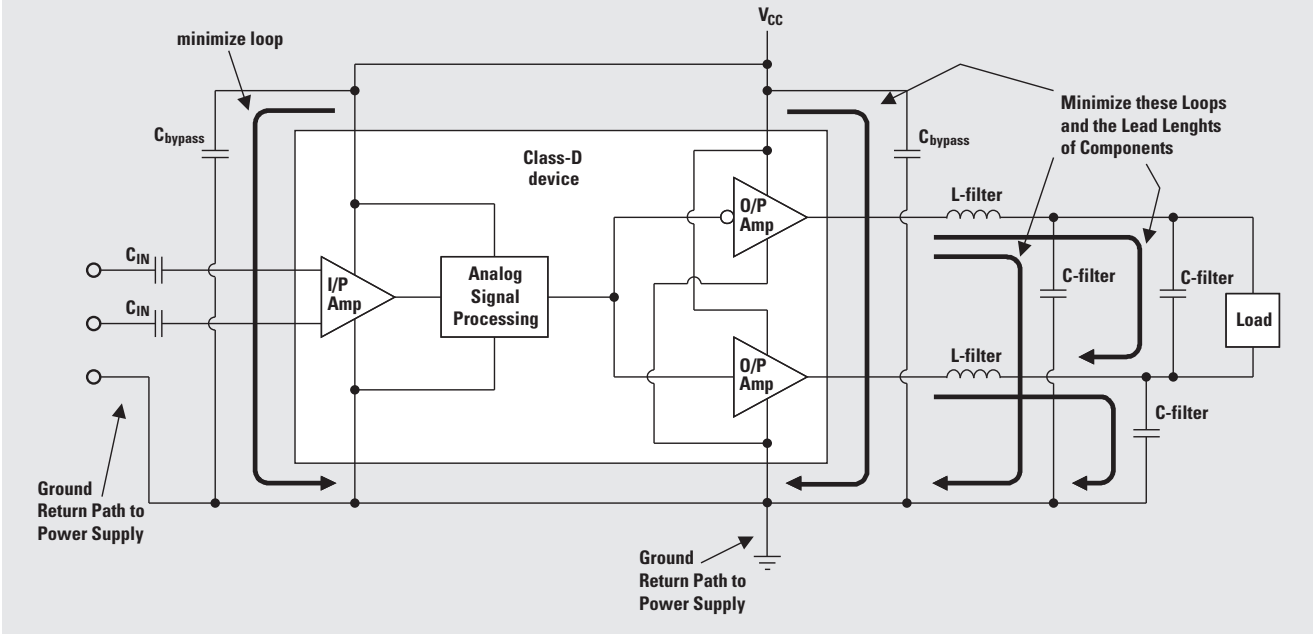
Figure 4. Output ground loops and return paths

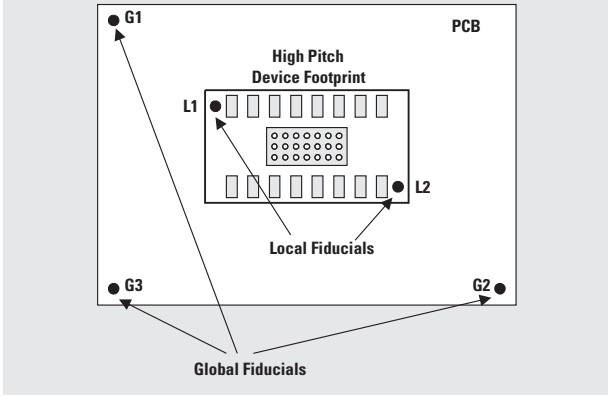


created by the rail-to-rail 250-kHz switching waveform. The signal on the load side of the inductor is mostly 20 kHz, with some 250-kHz ripple present. The output filter capacitors provide paths for the ripple and other high-frequency signals to bypass the load. These capacitors should be placed as close as possible to the inductors and should have a clear ground path back to PGND and the power-supply ground return paths.

The charge pump circuit supplies the charge for the MOSFET gates and is not particularly susceptible to distortion. It is still good practice to keep the traces to the capacitors in this circuit as short as possible.

The headphone circuit requires more consideration. The traces from the input pins for the left and right channels to the input capacitors and feedback components should be kept short to reduce noise pickup and amplification. This is due to the high input impedance of the amplifier inputs and the stray capacitance at these nodes that combine to allow signal from one channel to be injected into the other. Reducing the size of these resistors and decreasing the gain both can lower the amount of crosstalk.[5]

Figure 5. Two types of commonly used fiducials



Fiducials

The use of fiducials is recommended to increase the accuracy of part placement, particularly on boards using small-pitch surface-mount components and devices. The fiducial is a mark that is placed on a PCB during the etching process, and it can be bare copper or copper covered with various protective coatings or platings. The fiducial provides an optical reference to the manufacturing equipment that is used to align the boards properly during assembly. The information in this section can be obtained in greater detail from Reference 4.

Two types of fiducials, global and local, are commonly used, as shown in Figure 5. The global fiducials are placed on the corners of the PCB and serve to align the entire board. The number of fiducials required depends upon the type of accuracy needed. One fiducial is used to correct horizontal and vertical offset errors. Two fiducials will, in addition, correct any rotational errors. Three are used when it is also necessary to correct errors introduced by nonlinear distortions of the PCB that occur during assembly. These fiducials can be placed on any corner except when using two fiducials, in which case they should be placed in diagonally opposing corners.

The local fiducial is used when a fine pitch device is being placed on the PCB to ensure that it is accurately

positioned. A maximum of only two local fiducials is used, and they provide the same information as for the global fiducials mentioned earlier. The only differences are that these fiducials must fall within the land pattern of the device and, if only one fiducial is used, it should be placed toward the center of the land pattern if possible.

The diameter of fiducials should be between 1 mm (39.4 mils) and 1.5 mm (59 mils), with all of the fiducials the same size on a given board. A zone of at least twice the radius from the center of the fiducial should be kept clear of any other objects. They should not be any closer to the edge of the board than 5 mm (200 mils) plus the radius of the fiducial. The solder mask must be kept far enough away from the fiducial to prevent any solder mask from bleeding onto and obscuring it. If components are placed on both sides of a PCB, then fiducials can be placed on both sides. It is a good idea to keep the internal layers underneath the fiducials the same so that the appearance of the fiducials is identical to the optical device.

Trace thickness

The traces of the PCB should be wide enough so that they neither create any large voltage drops due to large trace resistance nor create large trace inductance. This will mostly impact the traces that carry larger currents, such as the power supply and output traces. The trace resistance will depend upon the thickness of the copper, given in ounces per square foot of board, and the length and width of the trace. One-ounce and two-ounce copper is commonly used in EVMs, with one-ounce copper being approximately 0.035 mm (1.4 mils) and two-ounce copper being approximately 0.07 mm (2.8 mils) thick. Table 2 shows the amount of current that can pass through a specified trace area for a given temperature rise (ΔT). This information was derived from IPC 2221[6] and has already been derated by 10% to allow for variations due to processing.

The resistance of a trace may be calculated for one-ounce copper based on the formula $R = 0.00502\Omega xL/(WxT)$, where R is the resistance in ohms, L is the length of the trace in mils, W is the width of the trace in mils, and T is the weight of the PCB copper in ounces.

Summary

PCB design can limit the performance and/or reduce the reliability of the Class-D circuit if some basic layout concepts are not followed. Modern PCB manufacturing techniques allow good, thorough isolation of the IC and component pads and vias through the accurate placement of solder mask. This in turn allows the area to which the solder paste is applied on the board to be reduced, focusing the flow of the paste during reflow soldering on the desired areas. This forms a stronger mechanical bond between the device or component and the PCB. This is particularly important when using PowerPAD devices to help counter the tendency of solder to be wicked from the IC pins toward the PowerPAD.

The reduction of ground loops and provision of current return paths for inputs and outputs enhance the isolation of these two sections, maintaining quality performance from the amplifier. The consideration of the more sensitive nodes of the TPA005D1x and TPA032D0x devices reduces noise pickup and crosstalk between the channels. The addition of a few fiducials then ensures that the parts will be where they need to be during the assembly process. See Reference 7 for more information on the Class-D audio power amplifiers.

Table 2. Current and trace area impact on temperature rise, resistance for external conductors

MAX CURRENT (A)	MAX ΔT (°C)	MINIMUM TRACE WIDTHS (in.)			1-in. TRACE RESISTANCE (mΩ)		
		0.5 oz.	1.0 oz.	2.0 oz.	0.5 oz.	1.0 oz.	2.0 oz.
1	10	0.030	0.015	0.007	335	335	359
	20	0.020	0.010	0.003	502	502	837
	30	0.014	0.007	0.002	717	717	1255
2	10	0.080	0.040	0.020	126	143	126
	20	0.050	0.025	0.014	201	201	179
	30	0.040	0.018	0.008	251	295	314
3	10	0.120	0.120	0.030	84	42	84
	20	0.080	0.080	0.020	126	63	126
	30	0.060	0.062	0.014	167	81	179

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www.ti.com/sc/docs/package/pkg_info.htm

www.ti.com/sc/docs/tools/analog/amplifiersdevelopmentboards.html

Get product data sheets at:

www.ti.com/sc/docs/products/analog/*device*.html
Replace *device* with tpa005d12, tpa005d14, tpa032d01, tpa032d02, tpa032d03, or tpa032d04

TI Worldwide Technical Support

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