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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following product categories:

- Data Acquisition
- Power Management
- Signal Conditioning (Audio Amplifiers, Op Amps, Thermistors)

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Because this book is limited in size, readers should refer to more detailed technical information, which can be found on TI's product-specific websites listed at the end of each article.

Building a simple data acquisition system using the TMS320C31 DSP

By Joselito Parguian
Application Specialist

Introduction

When design engineers are faced with challenging design issues with emerging technology, they almost always think the design solution has to be complex. This is not always the case, especially with Texas Instruments products. One of TI's objectives is to develop products that are technically competitive and easy for designers to implement. This article demonstrates this simplicity while describing the interfacing of the TMS320C31 DSP to the TLV2548 ADC and TLV5618A DAC. This hardware interface solution is efficient, inexpensive, and easily accomplished. It provides an effective and very simple system for data acquisition applications.

Serial analog-to-digital converter

The TLV2548 is a high-performance, 12-bit, low-power, CMOS analog-to-digital converter (ADC). Conversion is accomplished by successive approximation with a charge-redistribution digital-to-analog converter (DAC). This conversion process is initiated by an external trigger signal, and once conversion is complete, a 16-bit output code is generated.

Data transfer in normal operation consists of a digital signal processor (DSP) initiating a command for the ADC to start sampling and converting the signal. A specified time after sampling and conversion are completed, the ADC interrupts the DSP and notifies it that the data is ready to be read.

The DSP and ADC logic interface is described below:

- The DSP selects the ADC by asserting the $\overline{CS}$ pin of the ADC through the XF0 output of the DSP.
- The transmit clock output of the DSP, CLKX, provides a fixed data clock into the SCLK input of the ADC and into the receive clock, CLKR, of the DSP as well.
- The transmit frame-sync output, FSX, initializes every data transfer by sending a frame-sync pulse to the ADC FS input, as well as to the receive frame-sync input, FSR.
- The DSP initializes the ADC by transferring a 4-bit control word and 12 bits of data from the DX output into the SDI input of the ADC. A configuration cycle follows after initialization is complete, and then a select cycle.
- After the conversion process is complete, the ADC generates an interrupt for the DSP to read its conversion data. The falling edge of $\overline{CS}$ or FS, whichever comes first, cancels the interrupt and clears the conversion data.
- The ADC clocks the digital conversion result out at the SDO pin, and into the DR input of the DSP.

Serial digital-to-analog converter

The TLV5618A is a low-power, dual 12-bit voltage output DAC, fabricated in CMOS technology, that can operate from a wide range of single-supply voltages. The resistor string output voltage is buffered by a 2x gain rail-to-rail output buffer. The buffer features a Class-AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows for speed optimization versus power dissipation. The DAC is programmed with a 16-bit serial string containing 4 control and 12 data bits as shown in Figure 1.

Figure 1. DAC data format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	RO	MSB	12 Data bits										LSB

The DSP and DAC logic interface is described below:

- The DSP selects the DAC by asserting the $\overline{CS}$ pin of the DAC through the XF0 output gated along with FSX/FSR signals of the DSP. This is necessary because the DSP serial port is shared with another serial I/O device. In addition, the DAC does not support frame-sync pulse for data transfers, and the DSP initializes every data transfer by sending a frame-sync pulse.
- The transmit clock output of the DSP, CLKX, provides a fixed data clock into the SCLK input of the DAC and into the receive clock, CLKR, of the DSP as well.
- The DSP initializes the DAC and writes the data by transferring a 4-bit control word and 12 bits of data from the DX output of the DSP into the DIN input of the DAC.

Before the operation of the system is described, the reader should understand the internal operation of the TMS320C31 DSP standard bi-directional serial port interface.

DSP standard serial interface

The TMS320C31 DSP supports a standard bi-directional serial port interface that provides direct communication with any serial I/O devices. Before any system processes can be performed, initialization and configuration are required for all devices to be working properly. The DSP serial port requires a little more time and understanding for initializing and configuring, compared to the data converter devices. Therefore, this article explains the serial interface in some detail.

Six control lines from the DSP are used to interface to the data converters, and they are as follows:

CLKX Transmit clock input or output

This signal clocks data from the transmit shift register (XSR) to the data transmit (DX) pin. The serial port can be configured for internal clock generation

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or to accept an external clock. If the port is configured to generate the data clock on-chip, CLKX becomes an output, providing the data clock for the serial interface. If the port is configured to accept an external clock, CLKX changes to an input, receiving the external clock signal.

FSX Transmit frame synchronization input or output
FSX indicates the start of a data transfer. The serial port can be configured for internal frame-sync generation or to accept an external frame-sync signal. If the port is configured to generate the frame-sync pulse on-chip, FSX becomes an output. If the port is configured to accept an external frame-sync pulse, this pin becomes an input.

DX Serial data transmit
DX transmits the actual data from the transmit shift register (XSR).

CLKR Receive clock input
CLKR always receives an external clock for clocking the data from the data receive (DR) pin into the receive shift register (RSR).

FSR Receive frame synchronization input
FSR always receives an external frame-sync pulse to initiate the reception of data at the beginning of a frame.

DR Serial data receive
DR receives the actual data, which is clocked into the receive shift register (RSR).

In addition to these six control lines, there are control, shift, and buffer registers that are all 32 bits wide. These 32-bit-wide registers support the standard serial port interface operation of the DSP. Each of these registers, except for the two shift registers (XSR and RSR), is located in its specific address mapped in memory. Table 1 shows the register names, their respective addresses, and the values used for configuration applicable to this article.

Table 1. Registers associated with the serial port

REGISTER NAME	ADDRESS (HEX)	VALUE (HEX)
Serial port global control	808040	0C140044
FSX/DX/CLKX port control	808042	00000111
FSR/DR/CLKR port control	808043	00000111
R/X timer-control	808044	000001CF
R/X timer-counter	808045	00000000
R/X timer-period	808046	00000000
Data-transmit (DXR)	808048	Variable
Data-receive (DRR)	80804C	Variable

The control registers contain the control bits, set by the CPU, to configure the operation of the standard serial port. The addressable buffer registers, DXR and DRR, are discussed further under “Serial port operation,” which follows. See References 1 and 3 for more information about the TMS320C31 DSP serial port.

Serial port operation

During the transmit operation, the CPU loads the data transmit register (DXR), which then loads the word into the transmit-shift register (XSR), and the bits are shifted out. The word does not get loaded into the XSR until it is empty. Once the DXR is loaded into the XSR, the XRDY status bit is set, specifying that the buffer (DXR) is available to receive the next word, thus providing a double buffering function. The rising edge of the XRDY signal sets the XINT0 bit in the interrupt flag (IF) register, provided that the transmit interrupt enable (XINT) bit, in the serial port global control register, and the CPU serial port 0 transmit interrupt enable (EXINT0) bit, in the interrupt enable (IE) register, are set.

During the receive operation, the CPU reads the received data from the data receive register (DRR), which is double-buffered as well. When the serial data (such as the ADC data) is input, the receive shift register (RSR) receives the data. When the specified number of bits is shifted in, the DRR is loaded from RSR, and the RRDY status bit is set, specifying that there is new data ready to be read from the DRR. If the DRR is not yet read and the RSR is full, the receiver is frozen. Any new data coming into the DR pin is ignored until the DRR is read. RSR does not write over the DRR; therefore, DRR must be read to allow new data in the RSR to be transferred to the DRR. The rising edge of the RRDY signal sets the RINT0 bit in the interrupt flag (IF) register, provided that the receive interrupt enable (RINT) bit, in the serial port global control register, and the CPU serial port 0 receive interrupt enable (ERINT0) bit, in the interrupt enable (IE) register, are set.

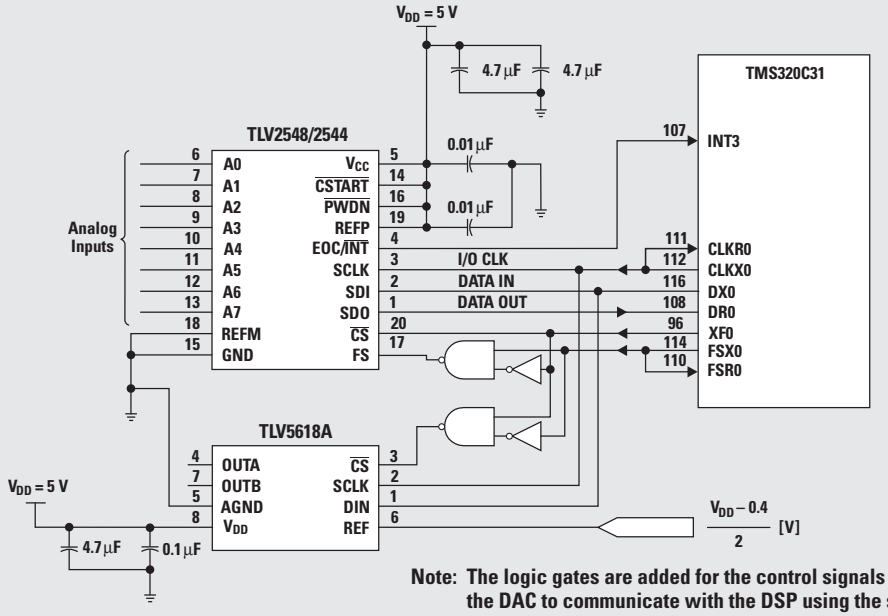
The interface operation

When only one data converter device is involved, interfacing to the DSP is a cinch. But if more than one serial I/O device is used to interface with the DSP serial port, some challenging design issues arise. The situation that needs to be addressed is that the DSP should assert only one data converter at a time, specifically with the ADC. This is because the ADC interrupt signal is canceled by the falling-edge transition of FS. If the ADC interrupt signal is canceled, the corresponding ADC conversion data is also cleared. On the other hand, the DAC write cycle starts when the device detects a falling-edge transition from its $\overline{CS}$ pin. The MSB is expected by the DAC after the falling edge of $\overline{CS}$; therefore, the DSP has to send the data instantaneously when a write to the DAC is performed. Since the DSP sends a frame-sync signal for every word transfer, the DSP has to be able to discern with which device to communicate. By gating, the required signals correctly achieve the complete isolation of the devices and ensure correct data transfer to each device.

The hardware solution in Figure 2 shows the use of multiple-gate logic to control the selection of data converters sharing the same serial port of the DSP.

The falling edge of the FS signal from the DSP is the start of the ADC cycle. The ADC cycle is normally started with an initialization cycle followed by a configuration cycle. Once the ADC is initialized and configured, the normal sample-and-convert process can be executed continuously. The ADC transmits and receives data with a 16-bit string, and the first 4 bits of data (MSB) received from the

Figure 2. Hardware configuration for DSP to ADC and DAC interface



Note: The logic gates are added for the control signals to allow the ADC and the DAC to communicate with the DSP using the same serial port.

DSP are interpreted as a command set to determine the mode of the ADC. The remaining 12 bits of data make up the configuration code. If the command set initiated is A hex for bits D[15:12], then the following 12 bits of data, D[11:0], are used to configure the ADC. Figure 3 shows the timing diagram of the ADC write cycle initiated by the DSP to configure the ADC. During the initialization and configuration cycle, no conversion cycle is initiated on either read or write. The conversion cycle is initiated only after the ADC is configured as one of the four different modes of conversion (modes 00, 01, 10, 11). These four conversion modes operate slightly differently from each other, depending on how the converter performs sampling. Although the ADC has different options to select its trigger for conversion, this article discusses only the use of $\overline{CS}$ and FS to trigger the start of conversion for the mode discussed here, mode 00 (single-shot mode). See Reference 6 for more information.

Figure 3 shows the typical data transfer sequence for the ADC input data. The first bit (MSB) of data is expected after the falling edge of FS, and all following bits are shifted in on the falling edges of SCLK. For the output data, the first bit (MSB) of data is presented to the SDO pin after the falling edge of $\overline{CS}$ and FS LOW is detected. Successive output data changes on the rising edge of SCLK and is available at the falling edges of SCLK.

The data collected by the DSP from the ADC is presented to the DAC at some certain time by the DSP. A slight adjustment to the ADC data needs to be made before it is presented to the DAC. Since the data received from the ADC has only 12 bits of usable data, the DSP has to

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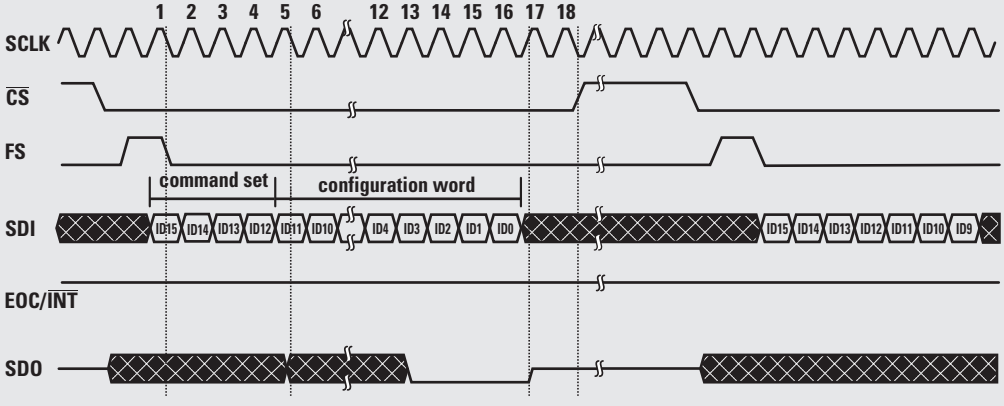
Figure 3. ADC configuration (write CFR)



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perform a shift of 4 bit positions to the right, starting from the MSB. The 4-bit control word for the DAC is then padded to the most significant nibble to make a good 16-bit string of data for the DAC. The DSP data manipulation flow, to format the ADC data to suit the DAC data format, is shown in Figure 4.

The DAC 4-bit control word, as shown in the 4 MSBs in Figure 1, is described as follows:

- R0 and R1 select all possible combinations of register-select bits (see Table 2).
- SPD controls the speed mode of the DAC.
- PWR controls the DAC to be in power-down or normal operation.

  SPD = 1 fast mode SPD = 0 slow mode
  PWR = 1 power down PWR = 0 normal operation

The DAC timing requirement is shown in Figure 5. See Reference 7 for more detailed information.

Figure 6 shows a typical timing diagram of the ADC and DAC data transfer through and from the DSP, respectively. The LOW time of ADC_CS indicates that the ADC is active, and the HIGH time indicates its inactivity. On the other hand, the LOW time of DAC_CS (HIGH time of ADC_CS) indicates the DAC active state. The specific assertion between the DAC and the ADC is made possible by the logic gates added in the hardware to share the DSP serial port.

A simple illustration of the complete data acquisition system is shown in Figure 7. The functional operation of the illustration is performed using the single-shot mode (mode 00) of the ADC for the data acquisition. Therefore, the single-shot mode will be discussed further to explain its operation.

Table 2. Register-select bits

R1	R0	REGISTER
0	0	Write data to DAC B and buffer
0	1	Write data to buffer
1	0	Write data to DAC A and update DAC B with buffer content
1	1	Reserved

Figure 4. DSP data manipulation of ADC data for DAC data format

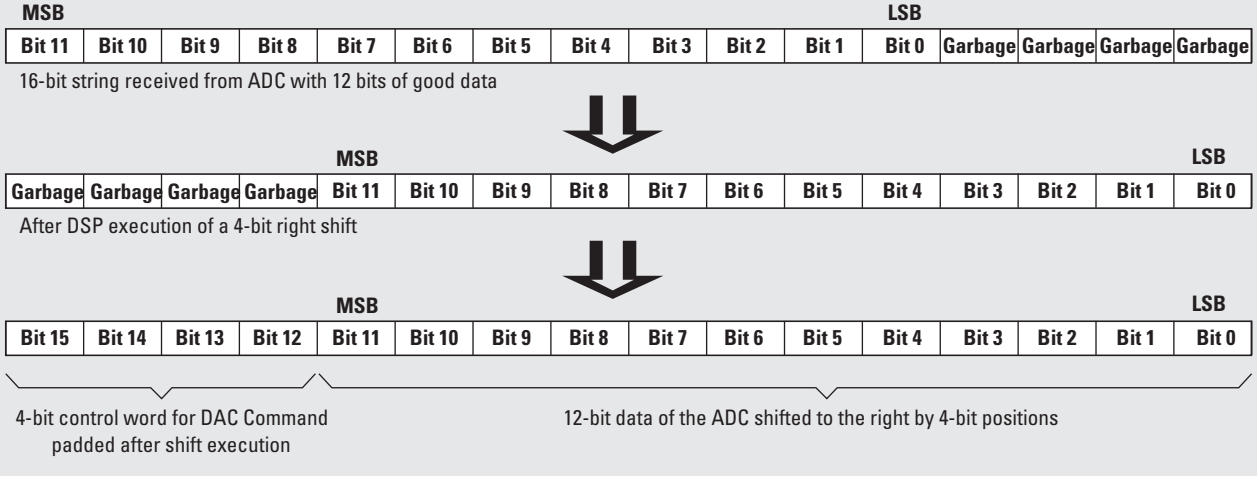


Figure 5. DAC timing diagram

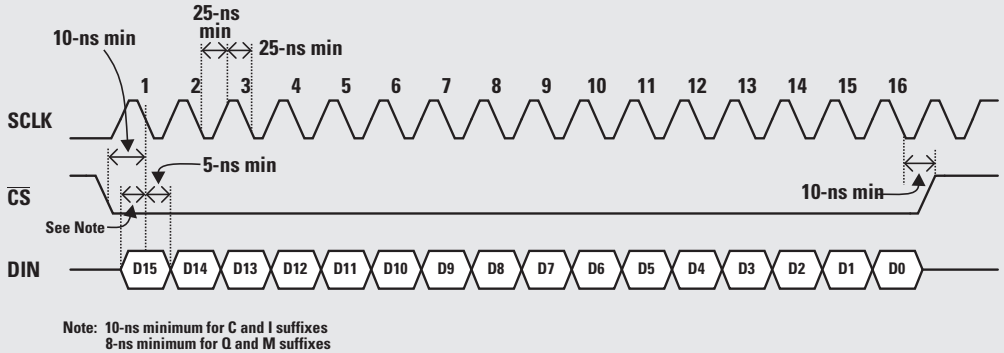
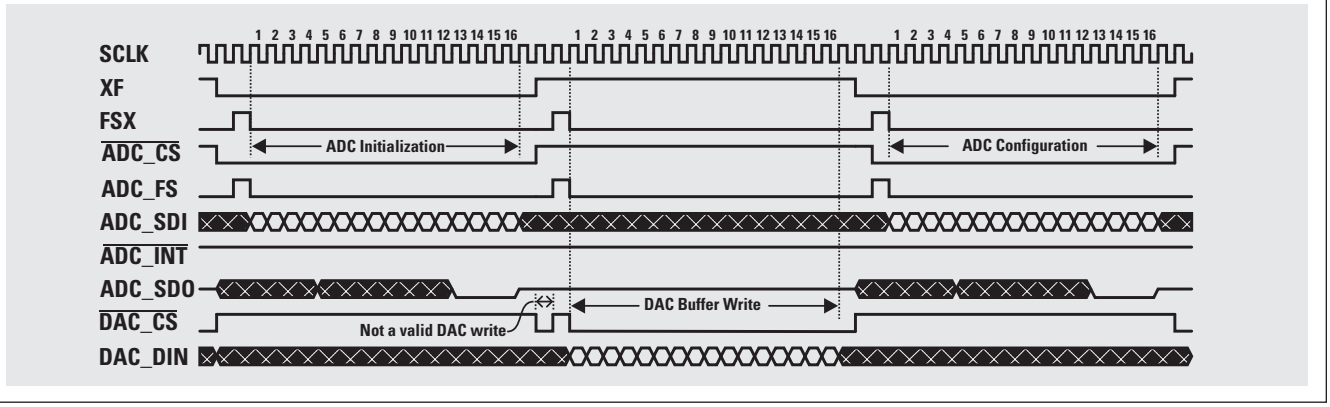


Figure 6. ADC and DAC timing diagram

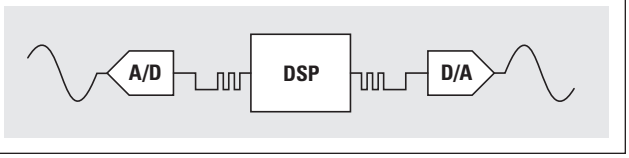


Mode 00 (single-shot mode)

The single-shot mode is the common method used for data conversion because it is easy to implement and a fairly simple process. The DSP initiates the conversion process by asserting the $\overline{CS}$ pin of the ADC through the XF0 pin and issuing the FS signal. This starts the ADC cycle. Figures 8-10 show a complete typical conversion cycle of the ADC in single-shot mode.

Figure 8 shows the initialization and configuration cycles. As discussed earlier, the initialization cycle is necessary for device performance stability. If the device is not initialized properly, it may not perform correctly. To initialize the device properly, write the configuration word A000 hex once upon power-up of the device. After initialization the device can then be configured. A000 hex was chosen for the configuration as well, since external reference, short sampling, internal oscillator for the conversion clock, single-shot mode, and interrupt pin function were selected. The DAC buffer is also initialized to zero to avoid any spurious data being written out from the DAC. This is specifically done when the first write to channel A of the DAC is initiated. The buffer content is written simultaneously to channel B of the DAC as well.

Figure 7. Illustration of the complete data acquisition system



In this article, channel selection (channel 1) is arbitrarily chosen for the ADC to sample the analog input. The channel is decoded in the first 4 SCLKs. Sampling is started at the beginning of the 5th SCLK and continues until the end of the 16th SCLK. The conversion cycle follows after the 16th SCLK, and an interrupt ($\overline{ADC\_INT}$) is generated by the ADC after the conversion is complete (or EOC is generated as the conversion is in progress), but it does not use the FIFO to store the data. The DSP must read the data out of the data converter before beginning another conversion cycle. Notice that as soon as the device is selected ($\downarrow\overline{CS}$ when FS is LOW), the previous conversion data is presented at the SDO pin and is held until the ADC sees a valid FS ($\downarrow$FS) signal. Succeeding data is available at the falling edge of SCLK. Also note that, for the first conversion cycle, the data presented at the SDO pin is garbage data. The DSP can either ignore this or perform a dummy read cycle, depending on the user's preference. If the garbage data is not read, it is simply overwritten with

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Figure 8. ADC initialization and configuration and DAC buffer write cycle for mode 00 (non-conversion cycle)

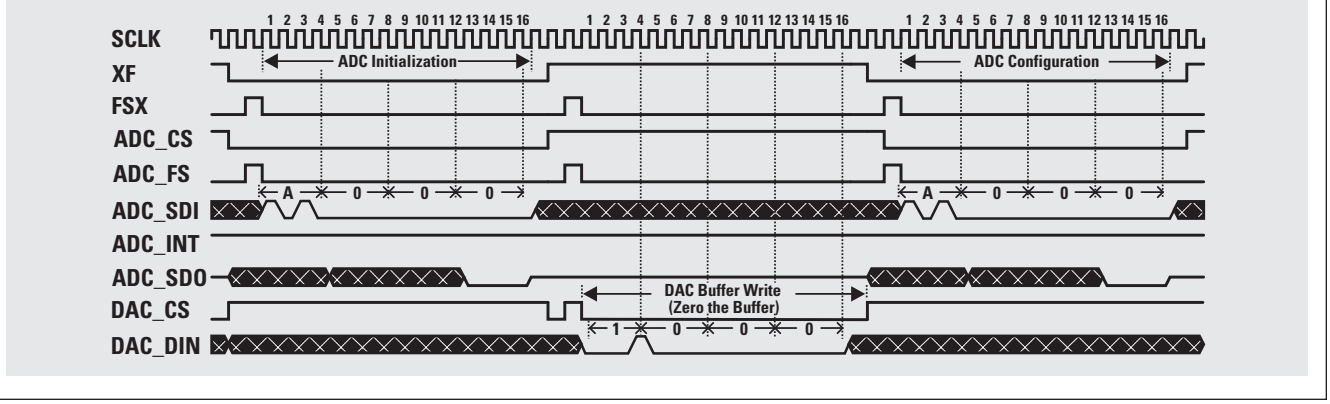


Figure 9. ADC channel select, first conversion cycle, and DAC write

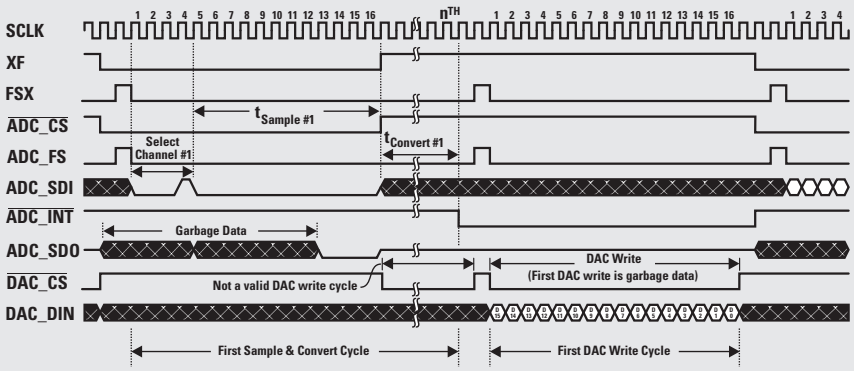
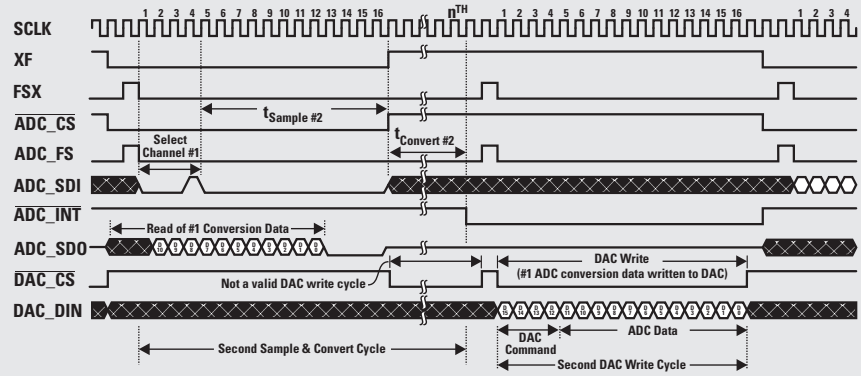


Figure 10. ADC channel select, second generation cycle, and DAC write



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the result of the simultaneous conversion process. Be aware, though, that this is also true for good data if another conversion is initiated without reading the ADC.

As soon as the DSP reads the ADC data, it adjusts the data to fit the DAC data format as discussed earlier. When the DSP has completed writing the adjusted data to the DAC, the ADC cycle is again repeated. This cycle continues until the program is aborted. A routine for the single-shot mode can be downloaded from the TI Web site at www.ti.com/sc/docs/psheets/abstract/apps/slaa101.htm

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

1. Joselito Parguian, "Interfacing the TLV2544/TLV2548 ADC to the TMS320C31 DSP," Application Report slaa101
2. Thomas Kugelstadt, "A Methodology of Interfacing Serial A-to-D Converters to DSPs," *Analog Applications Journal* (February 2000), pp. 1-9 . . . . . .slyt012
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9. "Code Composer Studio User's Guide" spru328

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www.ti.com/sc/docs/products/dsp/tms320c31.html

Using SPI synchronous communication with data converters—interfacing the MSP430F149 and TLV5616

By Mark Buccini
MSP430 Applications Manager

Introduction

Sophisticated analog waveform generation is often a requirement in modern microcontroller unit (MCU) applications. A few examples of these applications include DTMF, low-baud-rate modems, and stimulation of sensors. Most MCUs integrate some form of basic analog-to-digital converter (ADC), but few include a true digital-to-analog converter (DAC). Techniques such as pulse-width modulation (PWM) or resistor ladders can be used to generate simple analog signals, but such solutions can be resource-intensive and require complicated external filtering to smooth the final waveform. Using SPI synchronous communications, an MCU can easily interface to an external DAC that exactly matches the requirements of the application. This article describes how to interface the MSP430F149 USART serial port to the TLV5616 12-bit DAC. See Figure 1.

Serial interface

The MSP430F149 includes two identical USART modules (USART0 and USART1). The USART supports the transfer of serial data from the MSP430 to another device in either a synchronous (SPI) or asynchronous (UART) mode as a master or slave. User firmware configures the USART for the desired mode of operation as described under "Configuring USART0," which follows.

The physical interface between the MSP430F149 and TLV5616 is glueless, using three or four signal pins to communicate. The TLV5616 is a synchronous slave device requiring an external clock and data signals. USART0 on the MSP430F149 is configured for SPI operation in master mode. Serial data is output from the MSP430F149 on the slave-in/master-out (SIMO) pin and is synchronized to a clock signal generated on the USART clock (UCLK) pin. The TLV5616 receives data and clock on data-in (DIN) and serial clock (SCLK), respectively. There are two additional signals associated with the MSP430 USART in SPI mode—slave-out/master-in (SOMI) and slave-transmit-enable (STE). SOMI and STE are used with bi-directional SPI communications and are not required to communicate with the TLV5616. The TLV5616 is a slave only when receiving data and clock. No data is returned to the master. A frame-sync (FS) signal is sent to the TLV5616 with any MSP430 general-purpose port pin configured as an output (P3.0 is used in this example). A chip select ($\overline{CS}$) is also available on the TLV5616 that can place all other signal pins on the device in a high-impedance state when brought high. $\overline{CS}$ can be used in applications where several devices are present on the same bus. Using $\overline{CS}$, the MCU can directly enable and disable individual devices. In this article, it is assumed that $\overline{CS}$ is tied to ground, keeping the TLV5616 permanently enabled.

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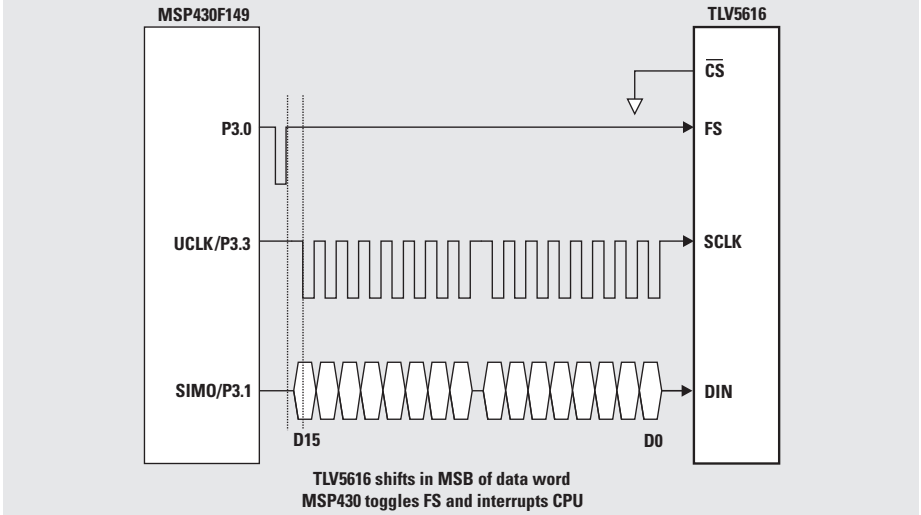
Figure 1. MSP430F149-to-TLV5616 interface



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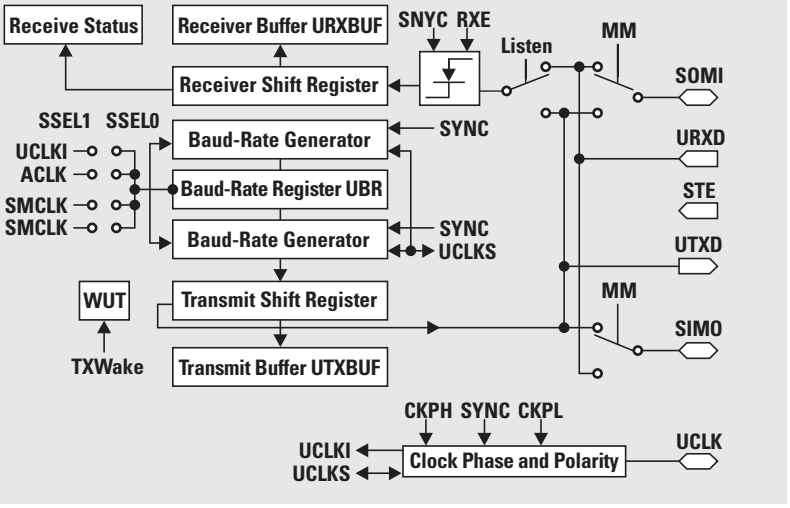
Configuring USART0

The USART is a completely independent asynchronous MSP430 module. The USART module incorporates a 16-bit baud-rate generator, 8-bit modulator, control and interrupt logic, and shift register/buffers for both transmit and receive paths. A simplified diagram of the MSP430 USART module is shown in Figure 2.

The USART first must be configured with control registers. MSP430 control registers are always collected in the lowest 256 bytes of the 64-kB memory map. The individual device data sheet will detail all peripherals and registers contained in a specific device. Three special-function, four port 3 (P3), and eight dedicated USART0-configuration registers are associated with USART0. See Table 1.

Figure 2. MSP430 USART module



The three special-function registers associated with USART0 are the interrupt enable register 1 (IE1), the interrupt flag register 1 (IFG1), and the module enable register 1 (ME1). The bit details of these registers are seen in Figure 3.

If USART0 interrupt capability is required, individual interrupt vectors are available for the transmit and receive paths and are enabled in IE1 using control bit UTXIE0 and URXIE0, respectively. As with any interrupt in the MSP430, the general interrupt enable (GIE) must also be set in the status register (SR). Interrupt capability is not used in the example given in this article, and these bits are left in their default (reset) condition. The interrupt flags for receive and transmit paths UTXIFG0 and URXIFG0 are located in IFG1. Setting USPIIE0 in ME1 enables the USART0 SPI function. This is important because USPIIE0 enables or disables all USART0 SPI functionality regardless of other bit configurations.

Figure 3. MSP430F149 special-function registers used with USART0

	7							0
IE1 00h	UTXIE0	URXIE0	ACCVIE	NMI	Unused	Unused	OFIE	WDTIE
IFG1 02h	UTXIFG0	URXIFG0	Unused	NMIIFG	Unused	Unused	OFIFG	WDTIFG
ME1 04h	UTXE0	UTXE0 USPIIE0	Unused	Unused	Unused	Unused	Unused	Unused

Table 1. MSP430F149 registers associated with USART0

REGISTER	SHORT FORM	REGISTER TYPE	ADDRESS
Interrupt enable 1	IE1	Read/write	000h
Interrupt flag 1	IFG1	Read/write	002h
Module enable 1	ME1	Read/write	004h
P3 input	P3IN	Read only	018h
P3 output	P3OUT	Read/write	019h
P3 direction	P3DIR	Read/write	01Ah
P3 select	P3SEL	Read/write	01Bh
USART control	UCTL0	Read/write	070h
Transmit control	UTCTL0	Read/write	071h
Receive control	URCTL0	Read/write	072h
Modulation control	UMCTL0	Read/write	073h
Baud rate 0	UBR0	Read/write	074h
Baud rate 1	UBR1	Read/write	075h
Receive buffer	URXBUF0	Read/write	076h
Transmit buffer	UTXBUF0	Read	077h

USART0 peripheral signals on the MSP430F149 are multiplexed on I/O port 3 (P3). It is important that the user carefully review the device-specific MSP430 data sheet to identify exactly on which port and pin a peripheral module is multiplexed. While the peripheral modules are identical on all MSP430 devices, the port pins on which the module is multiplexed may be different from device to device. On the MSP430F149, P3 pins can either be general-purpose I/O or selected as USART0 functions. There are six registers associated with port 3. In the example, user firmware selects the SIMO function multiplexed on P3.1 and UCLK on P3.3 by setting bits 2 and 4 in the P3 selection register (P3SEL). All PxSEL bits default to reset, general-purpose I/O. User firmware additionally sets the appropriate direction of USART0 pins required in the application using the P3 direction register (P3DIR). As UCLK and SIMO are both outputs from the MSP430, P3.1 and P3.4 (bits 2 and 5) are set in P3DIR. All PxDIR pins default to reset (input direction). The USART hardware will directly drive UCLK and SIMO during serial transfer. P3.0, which is used to control FS, is also set to the output direction by using P3DIR. The set/reset state of P3.0 is controlled with firmware by using the P3 output register (P3OUT).

In this example, the USART is configured as a transmit-only master in a synchronous mode using the MSP430 sub master clock (SMCLK) without interrupt capability. Only

the USART0 control register (UCTL0) and transmit control register (UTCTL0) have significance in this mode. Bit details of these two registers are shown in Figure 4.

UCTL0 configures the basic operation of USART0.

- SWRST = 1: The USART state machine is at reset, disabled.

  SWRST = 0: The USART state machine is ready.
- MM = 1: Master mode selected.

  MM = 0: Slave mode selected.
- SYNC = 1: Synchronous mode selected.

  SYNC = 0: Asynchronous mode selected.
- Listen = 1: Transmitted data is fed back to the receiver.

  Listen = 0: Receive data is received normally.
- CHAR = 1: 8 bits of data are transferred.

  CHAR = 0: 7 bits of data are transferred.

Setting the bits CHAR, SYNC, and MM in UCTL0 configures USART0 to transmit 8-bit characters in a synchronous master mode.

UTCTL0 configures the transmit operation of USART0. In the SPI master mode, the following are valid.

- TXEPT = 1: Flag is set when the transmitter shift register and UTXBUF are empty.

  TXEPT = 0: Flag is reset when data is written to UTXBUF.
- STC = 1: Four-pin mode, STE active.

  STC = 0: Three-pin mode, STE inactive.
- CKPL = 0: The inactive level is low; data is output with the rising edge of UCLK; input data is latched with the falling edge of UCLK.

  CKPL = 1: The inactive level is high; data is output with the falling edge of UCLK; input data is latched with the rising edge of SPICLK.
- CKPH = 0: Normal UCLK clocking scheme.

  CKPH = 1: UCLK is delayed by one half cycle.

  SSEL1, SSEL1: Define the clock source for baud rate clock (see Table 1).

To communicate with the TLV5616, CKPL and CKPH are both reset. As such, the USART presents data on the SIMO line synchronized on the rising edge of UCLK. The TLV5616 latches the relevant data on the falling edge of UCLK. Source select bits SSEL1 and SSEL0 select the baud rate clock (BRCLK). SSEL1 and SSEL0 are both set in the example, selecting SMCLK.

The USART0 control registers UBR10 and UBR00 concatenated define a 16-bit divider (UBR = UBR10, UBR00) such that UCLK0 = BRCLK/UBR. The maximum baud rate that can be selected for transmission in master mode is half of the BRCLK. In slave mode, the external clock applied to UCLK determines BRCLK. Modulation control is not used for serial synchronous communication. It is recommended to keep UMCTL reset.

TLV5616 configuration

Data is sent to the TLV5616 as 16 bits. The 4 most significant bits transfer the control bits as shown in Figure 4. The 12 least significant bits contain the new DAC code. The example in this article transfers all 0s for control bits. Only the DAC code is modified; thus the DAC is always powered up with 6-ms settling time.

Figure 4. USART0 control and transmit registers

	7							0
UCTL0 70h	Unused	Unused	Unused	CHAR	Listen	SYNC	MM	SWRST
UTCTL0 71h	CKPH	CKLP	SSEL1	SSEL0	Unused	Unused	STC	TXEPT

Figure 5. TLV5616 control register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	SPD	PWR	X												

- SPD = 1: 3-ms settling time

  SPD = 0: 6-ms settling time
- PWD power control 1 = Power down

  PWD power control 0 = Normal operation
- D11 ... D0 New 12-bit DAC code

USART0 operation

Once configuration is completed, using the MSP430 USART to transfer data is simple. Firmware initiates a transfer by writing a byte of data to the USART0 transmit buffer (UTXBUF0), which is automatically moved to the transmit shift register as soon as it is empty. Data is automatically shifted out at the selected baud rate. The USART will transfer data on the SIMO pin, with the most significant bit first, synchronized with UCLK. At the same time, if data is being received, it is shifted into the receive shift register; and, upon completion of receiving the selected number of bits, the received data is transferred to the USART receive buffer (URXBUF0). Receive and transmit always take place together, at opposite clock edges.

The TLV5616 requires a transfer of 16 bits of data. This can be accomplished efficiently by writing two byes back-to-back to UTXBUF0. The first byte written is loaded immediately from UTXBUF0 to the transmit shift register, making UTXBUF0 available for the second byte. The second byte can be written and will remain in UTXBUF0 until the first byte has transferred. USART0 will then automatically load the second byte to the shift register. The second byte is then transferred. Writing the two bytes back-to-back permits 16 bits to be effectively transferred in one operation. User firmware can poll the transmit-empty (TXEPT) flag in the UTXCTL0 to insure that no serial transfer takes place before data is loaded to the UTXBUF0. The TXEPT flag is set by USART hardware when both UTXBUF and the transmit shift register are empty. Writing data to UTXBUF0 clears the flag.

Description of the demonstration firmware

The demonstration firmware generates a repeating 12-bit ramp. After reset, firmware initializes the stack pointer and disables the watchdog. Port 3 and USART0 are configured, and the CPU register R4 is cleared. R4 contains the digital code 0 to 4095, which will be transferred to the

Continued on next page

Continued from previous page

TLV5616. The selection of R4 is random and not important. Any CPU register or RAM byte can be used to contain the digital code.

Inside the Mainloop program code, FS is toggled on P3.0. Toggling FS initiates the serial transfer to the TLV5616. The value from R4 is transferred to the TLV5616 as two bytes. As required by the TLV5616, the most significant byte is transferred first, followed immediately by the least significant byte. The two bytes are transferred to the TLV5616 by simply writing the individual bytes successively to UTXBUF0. The 12-bit value in R4 is then incremented and normalized to 0 to 4095. The transmit-empty (TXEPT) flag is polled to insure that the USART0 transfers all data from the transmit shift register and TXBUF before the firmware continues. This insures that the USART0 buffers are not overwritten with new data before the original data is shifted out. The loop repeats.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "MSP430x1xx Family," User's Guide	slau049
2. "MSP430x13x, MSP430x14x Mixed Signal Microcontroller," Data Sheet	slas272
3. "TLV5616C, TLV5616I 2.7 V to 5.5 V Low Power 12-Bit Digital-to-Analog Converters with Power Down," Data Sheet	slas152

Related Web sites

www.dataconverter.com
www.ti.com/sc/device/tlv5616
www.ti.com/sc/msp430

MSP430F149-to-TLV5616 example program

```
#define _CPU_ 6
#include    "STD_DEF.h" ; Standard equations
;*******************************************************************************
NAME  140_5516  ; MSP-FET430P140 demonstration program to generate a
repeating 12-bit ramp sent via USART0 to a TLV5616
;
;            M. Buccini
;            Texas Instruments Inc.
;            September 2000
;*******************************************************************************

;-------------------------------------
            ORG         0F000h                  ; Program Start
;-------------------------------------
RESET       mov         #0A00h,SP               ; Initialize stackpointer
Init_Sys    mov         #WDTPW+WDTHOLD,&WDTCTL  ; Stop WDT
SetupP3     bis.b       #00Ah,&P3SEL            ; P3.1,3 SPI option select
            bic.b       #001h,&P3OUT            ; FS reset
            bis.b       #001h,&P3DIR            ; FS output direction
SetupSPI    bis.b       #040h,&ME1              ; Enable USART0 SPI
            mov.b       #CHAR+SYNC+MM,&UCTL0    ; 8-bit SPI master
            mov.b       #CKPL+SSEL1+SSEL1+STC,&UTCTL0
                                                ; SMCLK for TX, 3-pin mode
            mov.b       #02h,&UBR00             ; SMCLK/2 for baud rate
            clr.b       &UBR10                  ; SMCLK/2 for baud rate
            clr.b       &UMCTL0                 ; Clear modulation
            clr         R4                      ;
                                                ;
Mainloop    bis.b       #001h,&P3OUT            ; Pulse FS
            bic.b       #001h,&P3OUT            ;
            swpb        R4                      ; R4 = 3412
            mov.b       R4,&TXBUF0              ; High byte to SPI TXBUF
            swpb        R4                      ; R4 = 1234
            mov.b       R4,&TXBUF0              ; Low byte to SPI TXBUF
            inc         R4                      ; Increment DAC data
            and         #00FFFh,R4              ; R4 = 0 to 4095 (12 bits)
L1          bit.b       #TXEPT,&UTCTL0          ; TXBUF/shift reg. empty?
            jnc         L1                      ; 1 = empty
            jmp         Mainloop                ; Repeat
                                                ;
;-------------------------------------
            ORG         0FFFEh                  ; MSP430 RESET vector
;-------------------------------------
            DW          RESET                   ; POR, ext. Reset, Watchdog
            End
```

A/D and D/A conversion of PC graphics and component video signals, Part 1: Hardware

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Introduction

This first part of a two-part article describes a design for the digitizing of component video signals, either sourced from a PC (PC graphics) or from a consumer video device (DVD, set-top box) that provides a component video output. First the characteristics of these signals are explained. Then we introduce the hardware of the THS8083 evaluation module (EVM) and a reference design for both A/D and D/A conversion. Finally, we explore some typical analog issues that affect the hardware, such as color spaces, video clamping, and its dependence on the color space used. We show an analog color space conversion circuit as a practical design example.

In the next issue of Analog Applications Journal, we will examine the functionality of the programmable logic device (PLD) on this board, the functionality of the PC configuration software, and its communication protocol with the board.

Figure 1. Composite video waveform

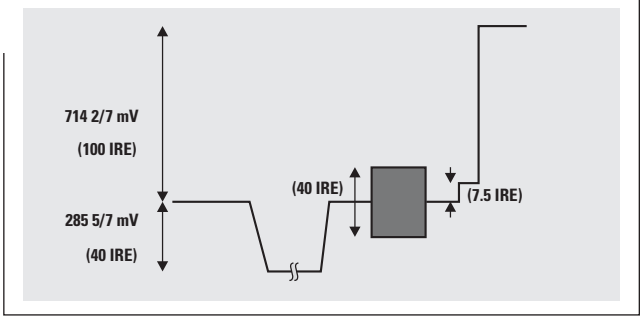
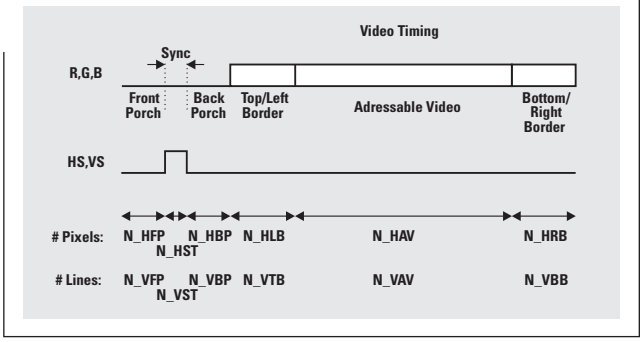


Figure 2. PC graphics timing definitions



Video signal characteristics

There are two possibilities for analog video representation: composite vs. component video. In composite video, as shown in Figure 1, the color information is phase modulated onto a subcarrier such that the complete color spectrum is represented by a 360-degree phase shift. The luminance of the video signal is amplitude-modulated, while the color information is added by phase modulation of a subcarrier.

This is the classical representation of NTSC/PAL or SECAM standard-definition TV. This video representation will not be discussed further here. PC graphics and high-definition TV (HDTV), on the other hand, use a component video format: the amplitude of three color component signals represents the relative intensities of three primary colors (Red/Green/Blue). This will be described later in this article.

A second characteristic of video signals is the way their timing is transferred—either as dedicated timing signals, signaling horizontal (Hsync) and vertical (Vsync) synchronization, or embedded within at least one of the color components. In the latter case, the sync information is composite; i.e., it contains both horizontal and vertical sync information. In order to synchronize the receiver, sync extraction is required of the composite sync from the color component (typically the Green or luminance channel) that embeds it. Subsequently this composite sync is separated into Hsync and Vsync.

Dedicated timing is used in PC graphics environments, while embedded composite sync is generally used for analog component video, including the analog representation of an HDTV signal.

Furthermore, in the case of PC graphics, Hsync and Vsync can differ in polarity. Figure 2 shows the nomenclature for defining typical timings for PC graphics signals. Each horizontal line is composed of FP, ST, BP, LB, AV, and RB, which denote, respectively: front porch (of sync), sync tip, back porch (of sync), left border, active video, and right border. Replace “left” and “right” with “top” and “bottom” for the vertical timing definitions. Tables 1 and 2

Continued on next page

Table 1. Frame rate/line rate/pixel clock, sync polarities and horizontal parameters for XGA (1024 x 768) PC graphics formats

RESOLUTION	F_{vert} (Hz)	F_{hor} (kHz)	F_{pixel} (MHz)	HS POLARITY	VS POLARITY	H_FP (pixels)	H_ST (pixels)	H_BP (pixels)	H_AV (pixels)	H_TOT (pixels)
1024 x 768	60.004	48.363	65.000	neg	neg	24	136	160	1024	1344
1024 x 768	70.069	56.476	75.000	neg	neg	24	136	144	1024	1328
1024 x 768	75.029	60.023	78.750	pos	pos	16	96	176	1024	1312
1024 x 768	84.997	68.677	94.500	pos	pos	48	96	208	1024	1376

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Table 2. Vertical parameters of XGA (1024 x 768) PC graphics formats

RESOLUTION	V_FP (lines)	V_ST (lines)	V_BP (lines)	V_AV (lines)	V_TOT (lines)
1024 x 768	3	6	29	768	806
1024 x 768	3	6	29	768	806
1024 x 768	1	3	28	768	800
1024 x 768	1	3	36	768	808

define these parameters for the popular XGA (1024 x 768) PC formats (the border parameters are all 0 and therefore not listed). We can see that, depending on the vertical rate (frame rate, refresh rate), the total number of pixels per line (H_TOT) or total number of lines per frame (V_TOT) can be different and also that the sync polarities are different. Fvert, Fhor, and Fpixel show the vertical (frame) rate, horizontal (line) rate, and pixel clock of the video format.

THS8083EVM features

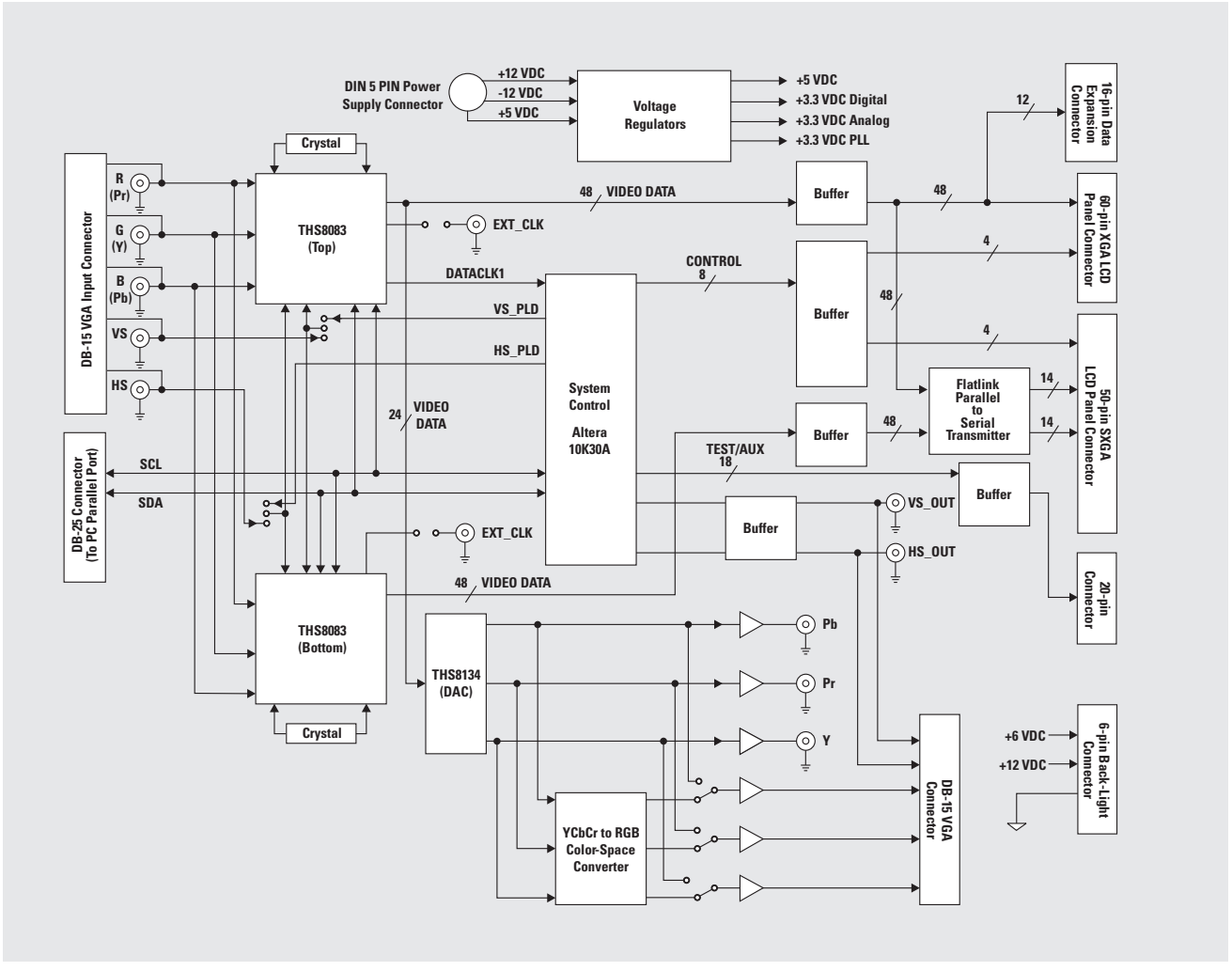
Video input
- Analog PC-type input from standard VGA connector or 5 BNC-type connectors (R or Pr, G or Y, B or Pb, Hsync, Vsync).

Video output
- Analog PC-type output to standard VGA connector or to 5 RCA-type connectors (R or Pr, G or Y, B or Pb, Hsync, Vsync).
- Video output carries separate sync signals (HS, VS) and Data Enable outputs, programmable in position, width, and polarity.
- Digital 3-V TTL/CMOS output to a flat-panel XGA-resolution display.
- Digital LVDS (FlatlinkTM) output to a flat-panel XGA- or SXGA-resolution display (not currently stuffed on board).

Control
- I^2C control via interface to standard PC parallel port for configuration and control.

Video processing
- A/D of PC graphics and component video input. All image formats up to 4096 pixels/line are supported.
- Programmable digital timing generation to flat-panel display for image centering of the active video window.
- D/A conversion of digitized input video image for monitoring image quality on a regular display accepting analog signals.
- Optional YCbCr to RGB color space conversion on the analog output.

Figure 3. THS88083EVM block diagram



THS8083EVM—a reference platform for component video and PC graphics A/D and D/A conversion

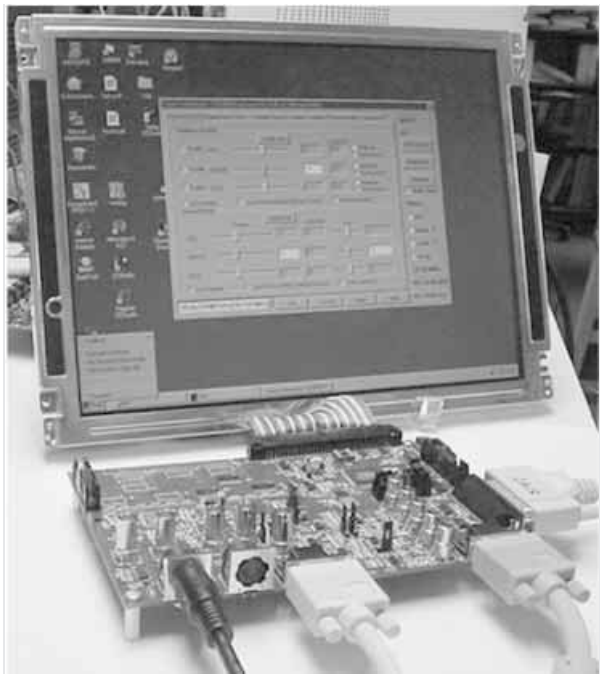
Figure 3 shows the block diagram of an evaluation module built around the THS8083, a triple 8-bit, 95-MSPS ADC for digitizing PC graphics or component video, and THS8134, a triple 8-bit video DAC.

The block diagram shows two ADCs, designated "Top" and "Bottom," for a "ping-pong" approach in which each ADC takes up the digitization at half the pixel clock, essentially boosting supported input format pixel clocks to 2x the maximum speed of the ADC. While the EVM board is provided for this, currently only a single ADC is stuffed. The output data of the THS8083 is fed via damping series resistors to limit switching noise of the digital output drivers from coupling back into the analog input, which would otherwise cause reflections on the display. Buffers feed the digital output connector from the top part. The video data is also sent to the serializing LVDS transmitter that feeds a second digital output; therefore, this board can be hooked up to LCD panels accepting parallel data as well as panels accepting LVDS serial data (there is no single standard for LCD panel interfaces in practice*).

An LCD panel also typically requires Hsync, Vsync, and Data Enable signals. Data Enable frames the active video window of the complete frame; i.e., only the viewed portion of the video frame is actually driven (unlike CRT tubes, there is no blanking time on LCD panels). These control signals are generated in the complex programmable logic device (CPLD) on the board. This design will be described in more detail later in this article.

*The current EVM version available from TI is populated for XGA/HDTV resolution only, without LVDS output.

Figure 4. THS8083EVM with LCD panel



The data of the top ADC also feeds the THS8134 DAC. Note that 48 signal lines are provided from each ADC, since each ADC has three double-pixel-width buses (3 channels x 8 bits x 2). The DAC has only 3 x 8 input signals. For the DAC to work, the 24-bit output needs to be selected.

The DAC's output is either fed directly to the VGA output connector, in case the RGB input was converted, or sent through an analog color space conversion circuit. This circuit implements a conversion from the YPbPr to the RGB domain, and its design is discussed in more detail in the next paragraph. The intended use is for applications in which YPbPr analog video (as available from, for example, a DVD player or set-top box with component output), is sent to the board and an RGB output is desired.

While not shown in Figure 3, the THS8083 has built-in functionality for separating the embedded composite sync from the Y channel. Note that the ADC only extracts the sync. In video terminology, it "slices" the Y channel at a level below blanking to extract the sync; it does not separate the composite sync into Hsync and Vsync components. Since the extracted sync can be fed through the CPLD, and the CPLD can be used as a source for the Hsync/Vsync to THS8083, it is in principle possible to design this function into the CPLD. However, the current firmware does not implement this. Figure 4 shows a picture of this EVM hooked up to a flat-panel display.

Video clamping and color space conversion

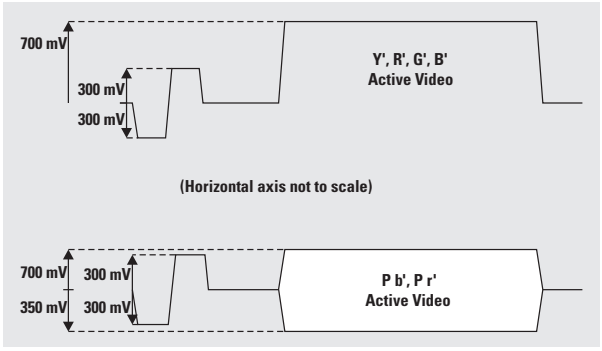
Video clamping and color space conversion are two video processing functions implemented on the analog video input by the THS8083EVM.

Clamping refers to a dc restoration of an ac-coupled signal. The circuit receiving the ac-coupled signal provides a dc bias to the signal in such a way that, during a period in which the amplitude of the signal is known, its dc level is fixed. In the case of video signals, the amplitude is known during the blanking period. Figure 5 shows the position of the blanking level during the back porch of the horizontal sync in the case of the R'G'B'Y' signals** and in the case of the color difference signals Pb'Pr'. Since by definition the color differences can go higher or lower than the blanking level, a circuit that is designed to receive both color spaces (R'G'B' vs. Y'Pb'Pr') needs to have a configurable blanking level on at least two channels. THS8083 has an

**The ' (prime) notation indicates that these signals are gamma-corrected.

Continued on next page

Figure 5. HDTV waveform (active video)



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internal clamping circuit for either bottom-level (R'G'B'Y') or mid-level (Pb'Pr') clamping, selectable via an I^2C register. Therefore, on the THS8083EVM, R'G'B' or Y'Pb'Pr'-type input component video signals can be fed directly to the device's input channels by using coupling capacitors with no additional processing.

How do we convert between both color spaces? We will look at the case converting Y'Pb'Pr' HDTV signals to an R'G'B' format suitable for display on an LCD panel or CRT display.

The matrix to convert from Y'Pb'Pr' to R'G'B' is:

$$E'_R = E'_Y + 1.575\ E'_{Pr}, \quad \textbf{(1)}$$

$$E'_G = E'_Y - 0.468\ E'_{Pr} - .187\ E'_{Pb}, \text{ and} \quad \textbf{(2)}$$

$$E'_B = E'_Y + 1.856\ E'_{Pb}, \quad \textbf{(3)}$$

where E' denotes a gamma-corrected normalized intensity level between 0 and 1.

Using the following notes, the user can verify that the circuit implements this conversion.

Red channel

In Figure 6,
X = Pr(1 + R2/R1), and [(R – X)/R3] + [(R – 2Y)/R3] = 0.
Therefore, R = Y + Pr/2(1 + R2/R1). From comparison to Equation 1, we need R2/R1 = 2.15. If we let R2 = 1300, R3 = 499, and R4 = 649, then R1 = 604.

Blue channel

Use the same circuit to arrive at B = Y + Pb/2(1 + R2/R1). From comparison to Equation 3, we need R2/R1 = 2.71. If we let R2 = 1300, R3 = 499, and R4 = 649, then R1 = 475.

Green channel

We derive Thevenin equivalents for both circuits in Figure 7, as shown. The top equivalent is straightforward. The bottom equivalent becomes
W2 = R9/(R8 + R9)W1 = –(R7 R9)/[R6(R8 + R9)]Pb.
Z = (R8 || R9)+R5. If we let R3 and Z = 1000, then
(G – W2)/1000 + [G + (R2/R1)Pr]/1000 + (G – 2Y)/499 = 0.
Therefore,
G = Y – R2/(4R1)Pr – {(R7 R9)/[4 R6(R8 + R9)]}Pb.

By comparison to Equation 2, we have the equalities –0.468 = –R2/(4R1); –0.187 = –R7 R9/[4 R6(R8 + R9)]; and Z = [(R8 R9)/(R8 + R9)] + R5 = 1000 as previously assigned. Therefore, if we let R8 = 768 and R9 = 1430, then R5 = 499. If R1 = 499, then R2 = 931; and if R6 = 931, then R7 = 1430.

Conclusion

This article introduced a generic hardware platform for digitizing PC graphics and component video built around THS8083 and THS8134. It also described the hardware of the EVM and gave a design example of a color space conversion circuit implemented in the analog domain (obviously, the 3 x 3 matrixing could also be implemented in the digital domain prior to D/A conversion).

In the next issue of Analog Applications Journal, we will discuss the CPLD design, the communication protocol and PC software, and the software implementation of a white-balance control mechanism for accurate channel-to-channel gain and offset matching.

Figure 6. Color space conversion (red and blue)

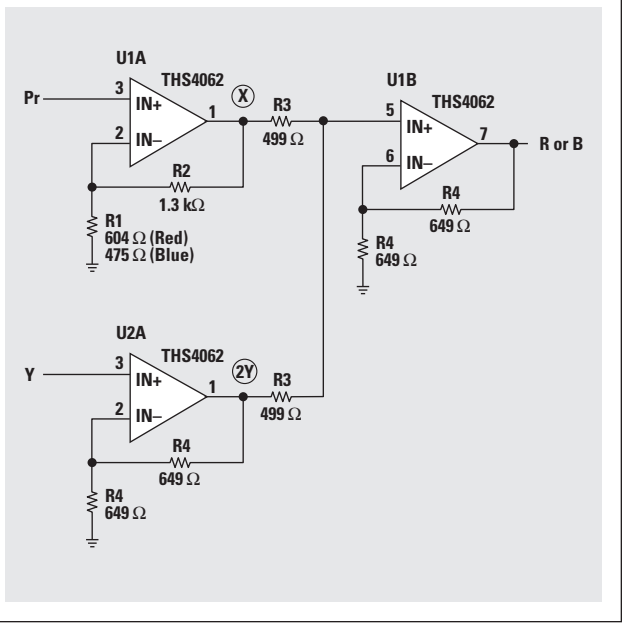
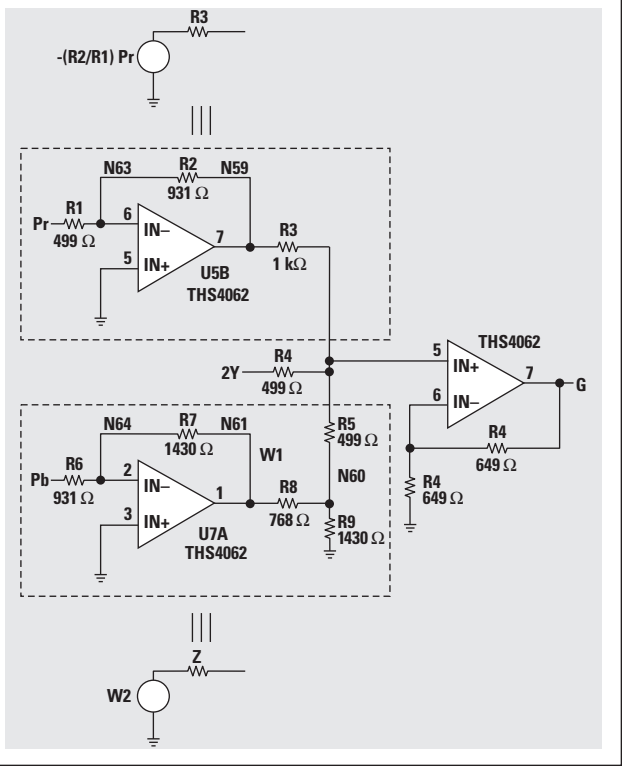


Figure 7. Color space conversion (green)



Related Web sites

www.dataconverter.com
www.ti.com/sc/device/ths8083
www.ti.com/sc/device/ths8134
www.ti.com/sc/ths8083evm

Optimal design for an interleaved synchronous buck converter under high-slew-rate, load-current transient conditions

By Rais Miftakhutdinov
System Engineering, Power Management Products

Introduction

The core voltages and currents of next-generation, high-performance microprocessors are approaching 1 V and 130 A.[1] At the same time, tight steady-state and dynamic tolerance requirements for core voltages present a big challenge for powering this type of load. To decrease the impact of PCB board and component parasitics during high-slew-rate microprocessor transients, the dedicated power supply and decoupling capacitors have to be placed as close as possible to the microprocessor.

The interleaved synchronous buck converter is a popular solution to supply high-current microprocessors because of the lower input and output current ripple and higher operating frequency of input and output capacitors in comparison with the one-channel solution.[2,3] Interleaving also enables spreading components and dissipated power over the PCB area, but it requires equal current sharing between the channels. Different control approaches to achieve good current sharing and fast transient response for interleaved microprocessor power supplies are suggested in References 2–5. Meanwhile, to determine an optimal application area for one-channel and interleaved solutions, an analysis and output filter selection procedure needs to be developed for the interleaved regulator to handle high-slew-rate, load-current transients.

The analysis and optimization procedure for the one-channel synchronous buck converter to handle high-slew-rate, load-current transients is described in References 6–8. This article extends this analysis to n-channel, interleaved synchronous buck converters. The analysis assumes that all channels are phase-shifted and that they share current equally during steady-state operation. During the load-current transient, all channels turn their FETs to the proper state simultaneously, providing the fastest transient response and recovery. This article describes procedures for minimizing cost and optimizing output filter design. A design example illustrates the analysis and compares an output filter selection of interleaved and one-channel converters for popular 12-V-input, 1.5-V, 50-A output applications.

Transient analysis for power systems with an n-channel interleaved buck converter

Model selection

The power delivery system considered in the analysis is shown in Figure 1. The model includes an n-channel, interleaved synchronous buck converter with controller, output inductors L_O...L_N, output bulk capacitor C_O with parasitics ESR and ESL, and supply path parasitics R_B and L_B. The equivalent resistor R_B characterizes resistive voltage drop through the supply paths and is the resistance of traces and connectors. The equivalent inductor L_B characterizes summarized inductive voltage drop through the traces and connectors. For the best transient response of an interleaved power supply, its control signals do not

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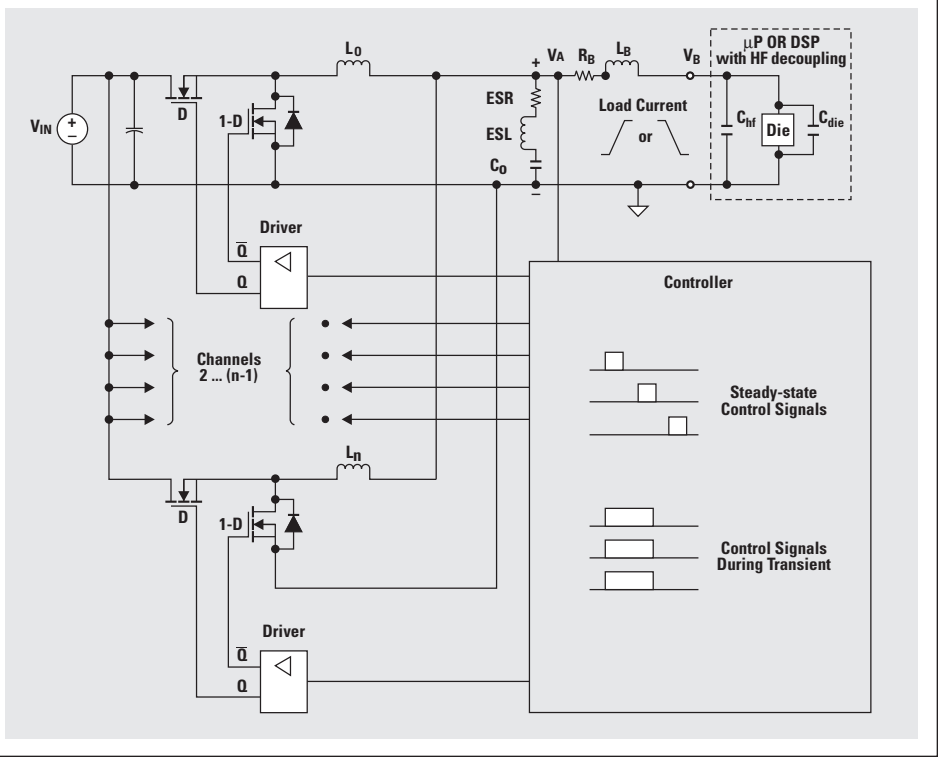
Figure 1. Model of interleaved synchronous buck converter to be analyzed



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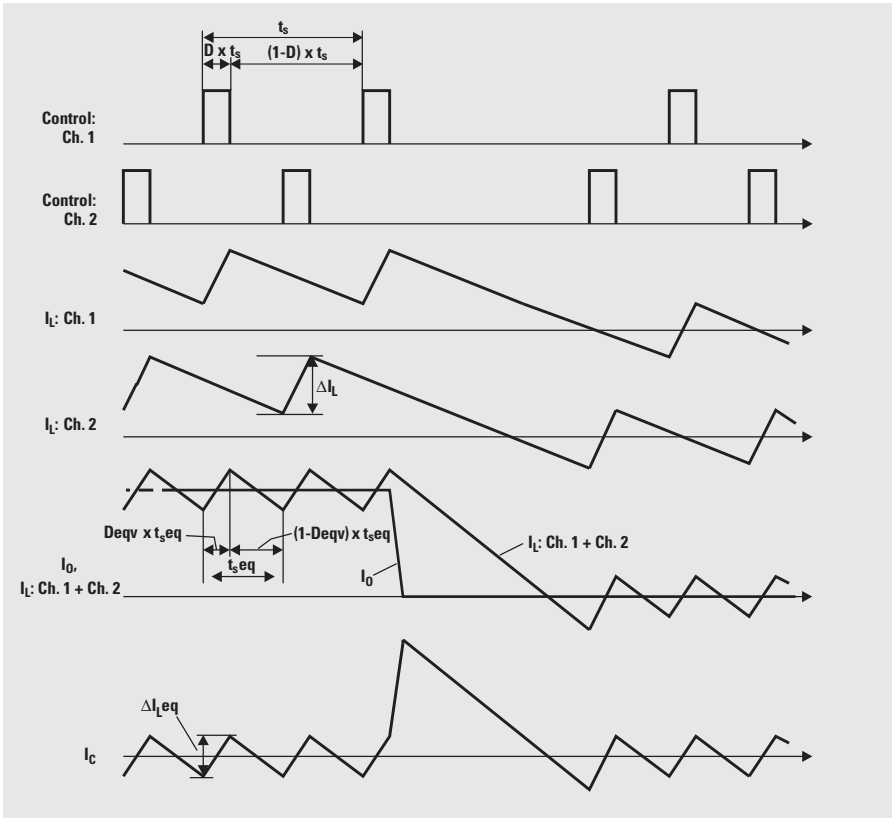
have to have delays and limitations on the duty cycle covering the range from zero to one. The controller operates in a phase-shifted manner under steady-state conditions, sharing current equally between channels. During transients, all channels simultaneously turn the high-side FETs on at load-current step-up or off at step-down, thus allowing the fastest recovery and minimum dynamic tolerance of the output voltage. When the output voltage reverts to the steady-state level, the channels revert to a phase-shifted operation with the same sequence they had before entering the transient. This "ideal" control algorithm for the best transient response is illustrated in Figures 1 and 2.

Figure 2. "Ideal" control algorithm for best transient response



Analysis approach

The analysis is based on an approach described in References 6–8 for a one-channel, synchronous buck converter; but first it is shown that any n-channel, interleaved synchronous buck converter can be considered, for analysis purposes, as some equivalent one-channel converter.

Assume that 1 – D > nD, where n is the number of channels and D = V_{OUT}/V_{IN} is a duty cycle. This condition is fulfilled for most microprocessor power supplies that have an output voltage below 2 V. For example, the popular 12-V-input and 1.6-V-output synchronous buck converter with four channels has D = 0.13, 1 – D = 0.87, and nD = 0.52; thus 0.87 > 0.52. This example confirms the previous assumption, meaning that for a steady-state analysis, the interleaved converter can be considered an equivalent one-channel converter operating at switching frequency nf_s and having the input voltage V_{IN}/n and output inductor L_O/n. At the same time, each channel of the interleaved converter uses output inductor L_O and operates at input voltage V_{IN}, with switching frequency f_s. The waveforms in Figure 2 illustrate this statement. It can be shown that the current through the inductors and output capacitor of an n-channel, interleaved converter has the same waveforms as an equivalent one-channel converter with the following parameters:

$$Deqv = nD,\ f_seqv = nf_s,\ t_seqv = t_s/n,\ L_Oeqv = L_O/n,$$
$$V_{IN}eqv = V_{IN}/n, \text{ and } \Delta I_Leqv = \Delta I_L(1 - nD)/(1 - D),$$

where D is the duty cycle, f_s is the switching frequency, t_s is the switching period, L_O is the output inductor, V_{IN} is the input voltage, and ΔI_L is the peak-to-peak inductor-current ripple of each channel of the interleaved buck converter. Deqv, f_seqv, t_seqv, L_Oeqv, $V_{IN}eqv$, and ΔI_Leqv are, respectively, the duty cycle, switching frequency, switching period, output inductor, input voltage, and peak-to-peak inductor-current ripple of a one-channel, equivalent buck converter. Because all channels turn to the same state simultaneously in accordance with the proposed control algorithm, during the transients the interleaved converter can be considered to have one channel, with the input voltage V_{IN} as the original interleaved one and the output inductor L_O/n. Considering parameters of an equivalent one-channel converter helps the reader understand what advantages to expect from the interleaved converter. The interleaving gives the same effect as the one-channel converter operating at higher frequency and at lower input voltage with the lower ripple and inductor value. All this works only if a good current sharing is provided between the channels both at steady-state and dynamic conditions.

The control signals, inductor currents through each channel and summarized inductor current, along with the capacitor and load current under the load-current step-down transient conditions, are shown in Figure 2.

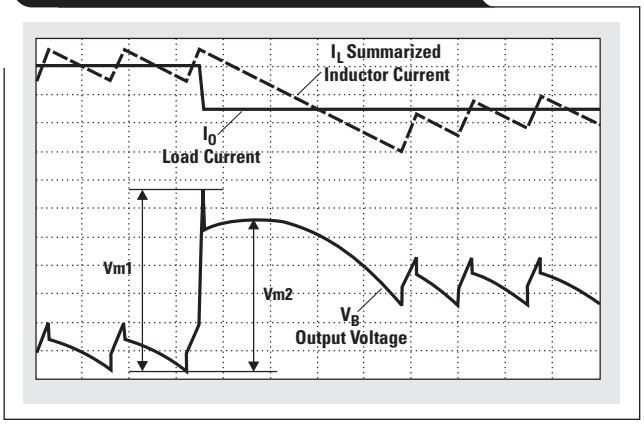
For analysis it is assumed that the output current has a linear waveform with a constant slew rate (SR) during the transient and that it changes between $I_{O(max)}$ and $I_{O(min)}$ (see Figure 2 for the current I_O). The analytical equations for the voltages and currents were derived through the main components of the equivalent one-channel model as a function of time for both the load-current step-down and step-up transients. Assuming an "ideal" control, the transient response of an interleaved converter is defined by the output filter characteristics, including the inductor-current slew rate. It is important to mention that for the step-down

transient, when all the low-side switches are turned on, the inductor current has the same slew rate as during the 1 – Deqv part of the switching cycle and equals $(V_{OUT} \times n)/L_O$. For the step-up transient, however, when all the high-side switches are turned on, the inductor-current slew rate is $[(V_{IN} - V_{OUT}) \times n]/L_O$, which is much higher than in steady-state operation during the Deqv part of the switching cycle, where the slew rate is only $(V_{IN} - V_{OUT} \times n)/L_O$.

Optimal output filter selection

Typical waveforms during the load-current step-down transient are shown in Figure 3. Usually there are two peak-to-peak values, Vm1 and Vm2. The first peak-value, Vm1, depends on ESR, R_B, ESL, and L_B (Figure 1) but not on the controller, because usually the controller's transient response is much slower than the duration of the first peak. The second peak value, Vm2, depends on ESR, R_B, L_O, C_O, and controller characteristics. References 6–8 show that the transient response depends on the position of the switching cycle when the load-current transient occurs. The worst case for the step-down transition is if the transient occurs at the end of an upper FET conduction time when the inductor current and output ripple are at their maximum. In contrast, the worst case for the step-up transition is if the transient happens at the end of the switching cycle while the inductor current and output voltage ripple are at their minimum. The same conclusion applies to the interleaved converter. The only difference is

Figure 3. Typical waveforms during load-current step-down transient



that the summarized inductor current and lower output voltage ripple need to be considered as they relate (in this analysis) to the equivalent one-channel converter. For accurate analysis, the worst condition of the transient has to be estimated.

The following equations have been derived for the number of output paralleled capacitors, N1 and N2, to meet the conditions Vm1 = ΔVreq and Vm2 = ΔVreq, respectively, as a function of switching frequency f_s, equivalent output inductor $L_O$eqv, and number of interleaved channels n:

$$N1 = \frac{\frac{ESL1}{t_O} + ESR1 + \frac{t_O}{2 \times C_O1} + \left(ESR1 + \frac{t_O}{2 \times C_O1}\right)\left(1 - \frac{t_O f_s n}{m}\right)KL}{\frac{\Delta Vreq}{\Delta I_O} - \frac{L_B}{t_O} - R_B}, \text{ and} \quad (1)$$

$$N2 = \frac{\frac{1}{2}\left[\frac{m}{C_O1 \times f_s \times n} - \frac{t_O}{C_O1} + \left(ESR1 + \frac{ESR1^2 \times C_O1 \times f_s \times n}{m} + \frac{m}{4 \times C_O1 \times f_s \times n}\right)KL + \frac{m}{C_O1 \times f_s \times n} \times \frac{1}{KL}\right]}{\frac{\Delta Vreq}{\Delta I_O} - R_B}, \quad (2)$$

where

$$KL = \Delta I_L eqv/\Delta I_O \text{ or} \quad (3)$$

$$KL = \frac{V_{OUT}(1 - Dn)}{L_O eqv \times \Delta I_O \times f_s \times n}. \quad (4)$$

Parameter m depends on the type of transient:

$$m = 1 - nD \quad (5)$$

for the worst-case step-down transient, and

$$m = \frac{D(1 - nD)}{n(1 - D)} \quad (6)$$

for the worst-case step-up transient.

The second peak-to-peak value, Vm2, exists only if the following condition is fulfilled:

$$\frac{m}{f_s \times n}\left(\frac{1}{KL} + \frac{1}{2}\right) - ESR \times C_O > t_O, \quad (7)$$

where t_O is load-current transition time.

If the second peak Vm2 does not exist, only the first peak Vm1 has to be considered during the selection of output capacitors. It might happen that N1 is significantly higher than N2, which means that the parasitic inductance ESL and L_B are too large for this application. In this case, the converter has to be located closer to a microprocessor, or an additional high-frequency decoupling is required. For the optimal design, the values N1 and N2 have to be almost equal.

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Design examples using different types of capacitors

To illustrate the theoretical analysis, different types of capacitors (aluminum electrolytic, OS-CON, specialty polymer, and ceramic) are compared in Table 1.

The design is satisfied for the following requirements, which are typical for a modern, high-end microprocessor: V_{IN} = 12 V, V_{OUT} = 1.5 V, I_O(max) = 50 A, I_O(min) = 0 A, ΔI_O = 50 A, ΔVreq = 100 mV, SR_{IO} = 50 A/µs, R_B = 0.4 m**Ω**, and L_B = 0.2 nH.

It is obvious that, for this application, the output filter design depends primarily on load-current step-down transients. This is because the inductor current has a much lower slew rate during the step-down transient than during step-up. Use of voltage positioning or droop compensation techniques only verifies this statement. Therefore, the following design example is focused on the load-current step-down transient.

The output filter selection curves have been plotted based on Equations 1 and 2 for different numbers of channels and different types of capacitors as a function of an equivalent output inductance $L_O$eqv (Figures 4-7). To obtain the actual inductance value for each channel of the interleaved converter, the equivalent inductance needs to be multiplied by the number of channels. The step in the curves for the number of capacitors N2 identifies the boundary where the peak Vm2 does not exist (Figure 3). If, for the selected type of capacitor and equivalent inductor, the number of capacitors N1 related to the peak Vm1 (Figure 3) is much greater than the number N2, parasitic ESL and L_B are significant. The additional high-frequency decoupling might help in this situation by decreasing the load-current slew rate applied to the output bulk capacitors.[8] The other solutions are layout improvement to decrease L_B or choosing the different capacitors with the lower ESL.

The number of capacitors has been obtained for the "ideal" controller, assuming that it has equal current sharing, the optimal control algorithm described earlier, and no delays. The practical implementation might require additional capacitors, but this analysis sets the target to achieve and show the relationship between the number of capacitors; the number of channels; the switching frequency; and the inductance value, including parasitics.

The curves are shown for 1-, 2-, 3-, and 4-channel interleaved converters (from top to bottom) for the aluminum electrolytic (Figure 4), OS-CON (Figure 5), specialty polymer (SP) (Figure 6), and ceramic (Figure 7) capacitors. Table 1 shows the required number of capacitors N2 and the inductance value L_O at different switching frequencies for this application. The following is a comparison summary:

1. The aluminum electrolytic and OS-CON capacitors require significant additional high-frequency decoupling at a slew rate of 50 A/µs because N1 >> N2.
2. Interleaving for aluminum electrolytic and OS-CON capacitors does not significantly decrease the number of output capacitors; only its lowering of the input filter ripple needs to be considered.
3. The 2-channel interleaving is optimal for the SP capacitors. They require much lower high-frequency decoupling at a 50-A/µs load-current slew rate.
4. The most significant effect of interleaving is that the required number of ceramic capacitors drops in inverse proportion to the number of interleaved channels. Ceramic capacitors do not require additional decoupling at a 50-A/µs load-current slew rate.

Table 1. Comparison of capacitor types

TYPE	VENDOR	PART NUMBER	f_s PER CHANNEL (kHz)	PARAMETERS OF EACH CAPACITOR			NUMBER OF CAPACITORS FOR DIFFERENT NUMBERS OF INTERLEAVED CHANNELS/L_O PER CHANNEL			
				C_O1 (µF)	ESR1 (mΩ)	ESL1 (nH)	1 CHANNEL	2 CHANNELS	3 CHANNELS	4 CHANNELS
Aluminum electrolytic	Rubycon	6.3ZA1000	200	1000	24	4.8	18/0.8 µH	16/1.6 µH	16/2.4 µH	15/3.2 µH
OS-CON	Sanyo	4SP820M	200	820	8	4.8	8/0.25 µH	7/0.5 µH	6/0.75 µH	6/1.0 µH
Specialty polymer (SP)	Panasonic	EEFCD0D101R	300	100	20	3.2	28/0.1 µH	18/0.2 µH	15/0.3 µH	13/0.4 µH
Ceramic, 1210	Murata	GRM235Y5V226Z10	400	22	20	0.5	60/0.05 µH	30/0.1 µH	20/0.15 µH	16/0.2 µH

Figure 4. Number of aluminum electrolytic capacitors as function of $L_O$eqv

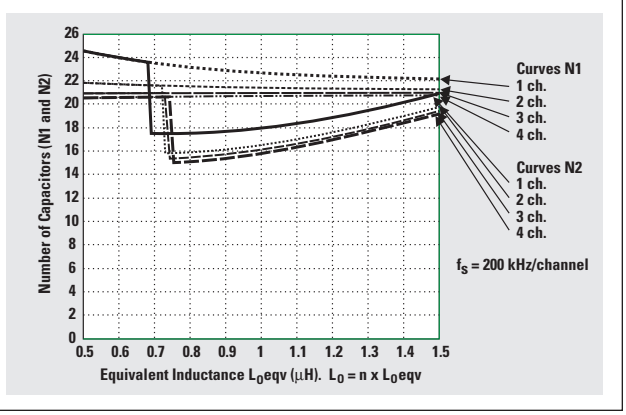


Figure 5. Number of OS-CON capacitors as function of $L_O$eqv

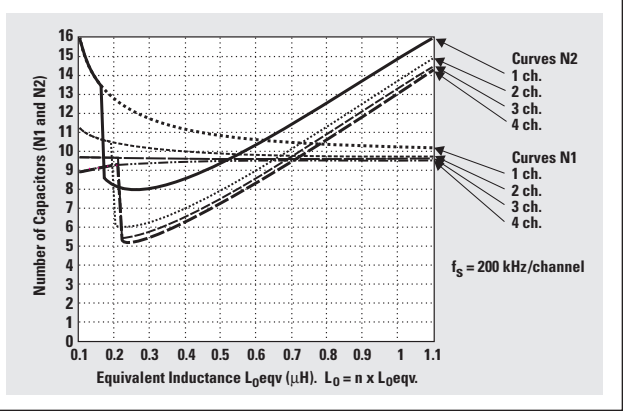


Figure 6. Number of SP capacitors as function of $L_O$eqv

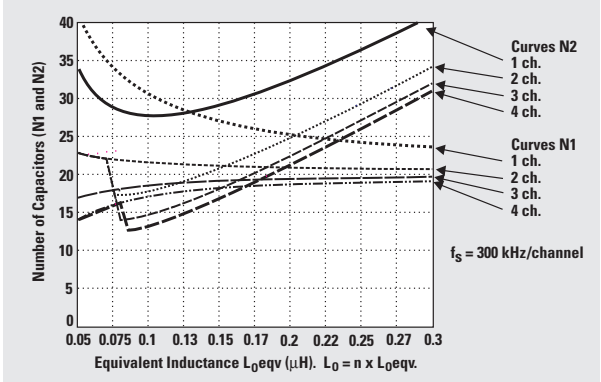
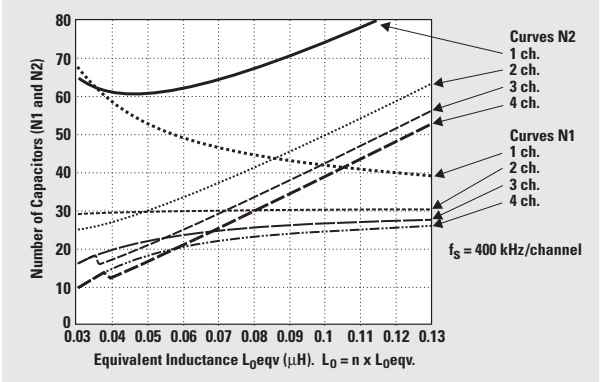
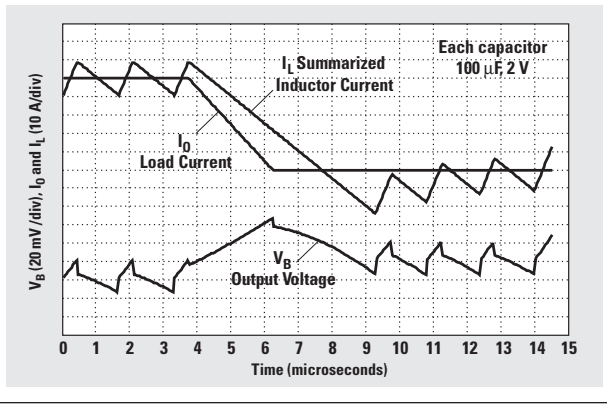


Figure 7. Number of ceramic capacitors as function of $L_O$eqv



A transient example for the 2-channel interleaved buck converter based on the suggested optimization procedure is shown in Figure 8. The switching frequency of each channel is 300 kHz. Eighteen SP capacitors (100 µF) have been used in parallel in this example in accordance with Table 1. The output inductance of each channel is 0.2 µH.

Figure 8. Step-down transient for 2-channel converter with 18 SP capacitors in parallel



Conclusion

Power-supply systems for high-slew-rate transient loads like microprocessors using an interleaved synchronous buck converter are analyzed. The selected model, based on practicality and sufficient accuracy, includes an interleaved synchronous buck converter with optimal control, output inductors L_O...L_N, output bulk capacitors, and power-supply plane parasitics. Analytical equations for the voltages and currents through components of the model were derived for any number of interleaved channels. An optimal output filter selection procedure is suggested based on the presented analysis and optimization curves for different types of capacitors and any number of interleaved channels. The design example compares aluminum electrolytic, OS-CON, SP, and ceramic capacitors for powering a 50-A microprocessor with an interleaved regulator.

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–48-V/+48-V hot-swap applications

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Introduction

The rapid growth of telecommunications and Internet access systems that run continuously has increased the need for hot-swap solutions that are more reliable and easier to upgrade and repair. Redundant systems or modules are required to prevent the systems from crashing. While redundant systems have been proven to be feasible, they may be costly. Furthermore, the use of a simple redundancy scheme as a backup may not be enough, as overall system integrity may be compromised even though the system is designed to handle such faults. In the end, we have to find a way to update the system regularly by removing redundant parts and/or inserting new modules while the system is still running. That is why hot-plug or hot-swap capability is required in today's high-availability electronic systems.

Realizing the needs of hot-swap applications, Texas Instruments has put a great deal of effort into providing solutions for a variety of end equipment requiring hot-swap capability. TI's hot-swap controllers provide inrush current control during hot insertion and fault protection during operation. They also prevent backplane power disruption during hot removal or insertion.

In particular, the TPS2300/01, TPS2310/11, TPS2320/21, and TPS2330/31 from TI (see References 1–4) cover a variety of hot-swap applications and were primarily designed for 3-V to 13-V applications. TI has already released and is planning several hot-swap devices targeting PCIx, CompactPCI®, and other mass-market applications. Devices like the UCC3913, UC3914, UCC3917, and UCC3921 operate across very wide voltage ranges, from large negative voltages to large positive voltages.

Most telecommunications applications use –48-V or +48-V power supplies, which are then distributed to the cards via the system's backplane. As there are many ways to implement hot-swap in a 48-V system, it is very important to understand the exact requirements of the system before selecting a power management solution. Certain features on some devices may no longer function at higher (or lower) voltage levels, although controlled ramp of power to the card during hot insertion/removal is still possible. By fully understanding the implementation requirements, you may find that there is a larger number of devices available, at a wide variety of price points, depending on the feature set required. The following discussion addresses different topologies in the TPS23xx series of TI's hot-swap controllers.

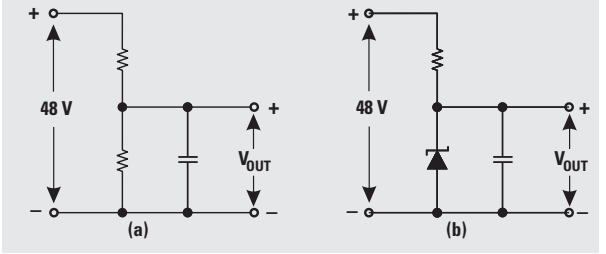
–48-V hot-swap application with low-side NMOSFET

Due to process limitations, the input voltage of the TPS23xx devices must be limited to 13 V (15 V maximum, dynamic). To manage higher voltages, some type of divider or converter is required to reduce the input voltage (48 V) to somewhere below 13 V.

There are several implementations that will keep the TPS23xx input voltage below the maximum limit. Figure 1a demonstrates the simplest topology. Two resistors are used to divide the higher input voltage into a lower voltage. However, in this implementation, the voltage at the output of the divider will track all changes in the 48-V input supply. Because the fluctuations and tolerances of the 48-V supply may vary not only from system to system but also based on the operating mode of the system, use of this scheme may affect the functionality of the controller, or possibly damage the device if large variations, or spikes, occur.

A much better, very simple solution consists of a Zener diode in series with a resistor to get a very steady output voltage from the 48-V source (see Figure 1b). This implementation will allow the voltage to be controlled at the divider to match the input voltage requirements of almost any hot-swap power manager. To eliminate noise or control the ramp-up rate of the output voltage, a capacitor should be added as shown in the figure.

Figure 1. Simple voltage dividers

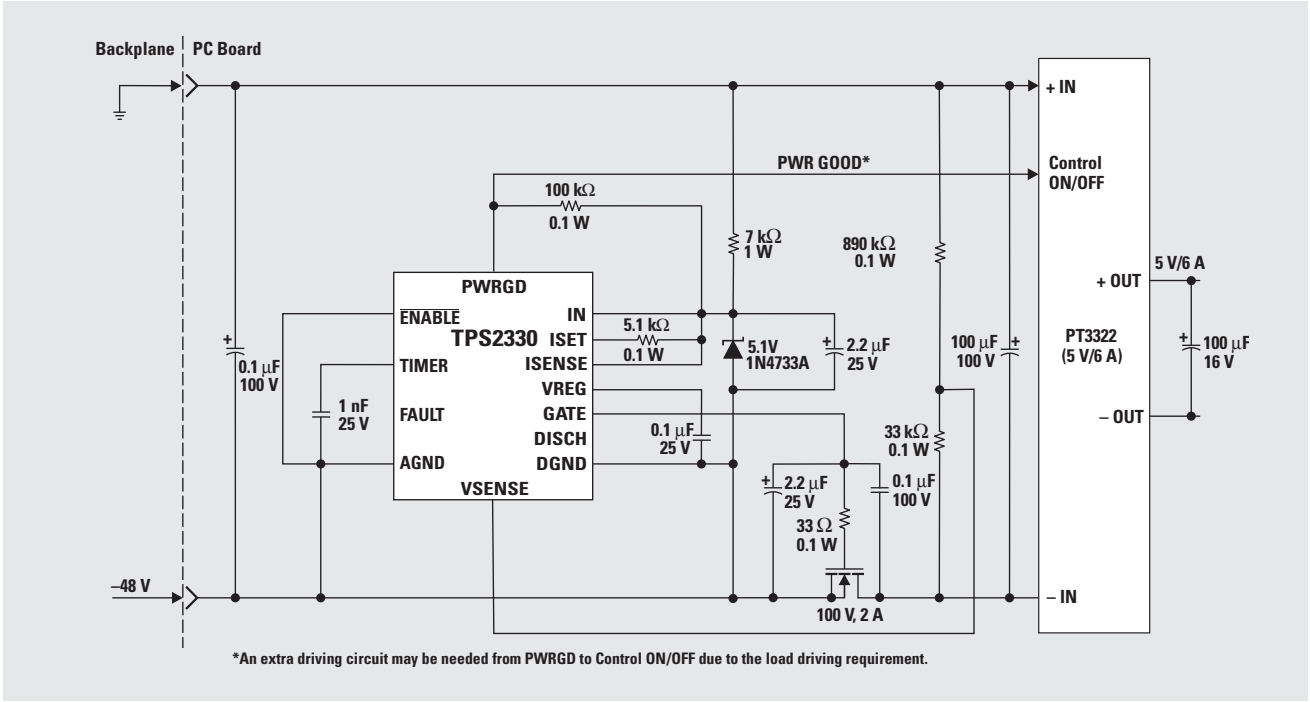


Of course, the performance of many other methods can equal or even surpass that of the Zener diode divider, but such methods tend to be more complicated and more expensive, and may be unnecessary for the –48-V applications. This is why the Zener diode divider is typically used in many 48-V hot-swap applications.

For –48-V hot-swap applications, the plug-in board can be configured as in Figure 2.

In this topology, the Zener diode is a 5.1-V 1N4733A, but higher-voltage (up to 10-V) Zener diodes can be used if desired. Since the TPS2330 consumes very little power for operation, the resistor (in series with the Zener diode) can be as large as 10 kΩ, depending on the threshold voltage desired. The load of the hot-swap control stage is a DC/DC converter—in this case, a Power Trends™ module

Figure 2. TPS2330 for –48-V hot-swap



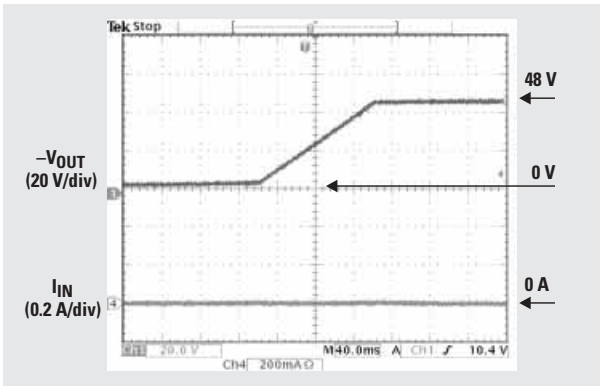
from TI. The main switch is a 100-V N-channel MOSFET, such as IRF530N.

With the component values shown in Figure 2, this circuit can work for –36-V to –72-V applications, which happens to cover the broad range of voltages in telecommunications applications. To make the voltage range wider, the 33-kΩ sensing feedback resistor can be increased.

The curves in Figure 3 show the performance of the TPS2330 during a hot-insertion event. Even though there is a 100-µF capacitor in the output circuit as a load, the inrush current during hot insertion is kept to less than 0.1 A. In a 48-V telecommunications system, a 0.1-A inrush current is negligible and will not cause any problems. If the output capacitance is much bigger than 100 µF, then the value of the 4.7-µF capacitor between the TPS2330 GATE output and the –48-V rail should be increased accordingly. The output voltage curve seems to ramp up from low to high voltage because the output voltage was measured at ground opposed to –48 V to keep measurement simple and safe. Therefore, what we see on the curve is actually $-V_{OUT}$.

One shortcoming of this implementation is that the hot-swap controller loses the circuit breaker capability because the TPS23xx cannot sense current at voltages above 13 V. Since most implementations use some type of current-limited regulation scheme to bring the 48 V down to more useful voltages like 3.3 V and 5 V, the circuit breaker capability is merely redundant.

Figure 3. Hot-insertion of –48-V system: output voltage ($-V_{OUT}$ and input inrush current (I_{IN})



Other high-voltage hot-swap applications

If a hot-swap board has two inputs—for example, one at +3.3 V (potentially a V_{AUX} rail) and the other at –48 V—the TPS23xx family can still be used as shown in Figure 4. The trick here is to use a high-voltage PNP to drive the gate of the main power MOSFET. This minimizes the voltage levels applied to the TPS2300, thereby keeping them well within its operating range. In this example the TPS2300 can control the switching and the inrush current during hot insertion of both the low-voltage (+3.3-V) rail and the higher-voltage (–48-V) rail. The TPS2300 will not sustain any high voltage from the –48-V input, and the +3.3-V rail will still have circuit breaker capability.

However, the first input (+3.3 V) of this hot-swap board can operate only between 3.0 to 5.5 V because the IN2 maximum voltage rating is 5.5 V. To get the IN1's operation range up to 13 V, the connection between IN1 and IN2

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must be broken. With a method similar to that previously described, the IN2 input voltage can be limited to well under +5.5 V by a Zener diode so that channel 1 can run up to +13 V.

If a high-side switch is desired, such as in +48-V applications, an NPN bipolar can be used to drive the high-side MOSFET switch, similar to that shown in Figure 4.

Conclusion

A fuller understanding of the overall power management requirements and limitations of the system reveals a greater number of solutions available for managing hot insertion/removal. It is important to understand exactly what the hot-swap power manager needs to provide to the system. The needs include: inrush current limiting, fault current limiting, an electronic circuit breaker, controlled rise/fall time for insertion/removal events, Power Good reporting and supervisor functions, and sequencing control.

Knowing exactly what you need the hot-swap power manager to do allows you to tailor many devices into an effective solution. For example, with the simple addition of a few external components, the TPS23xx hot-swap controllers can be used in very high-voltage hot-swap applications, negative or positive. Likewise, solutions using the UCC3921 or UCC3917 can be simplified greatly by removal of external components that are not required.

References

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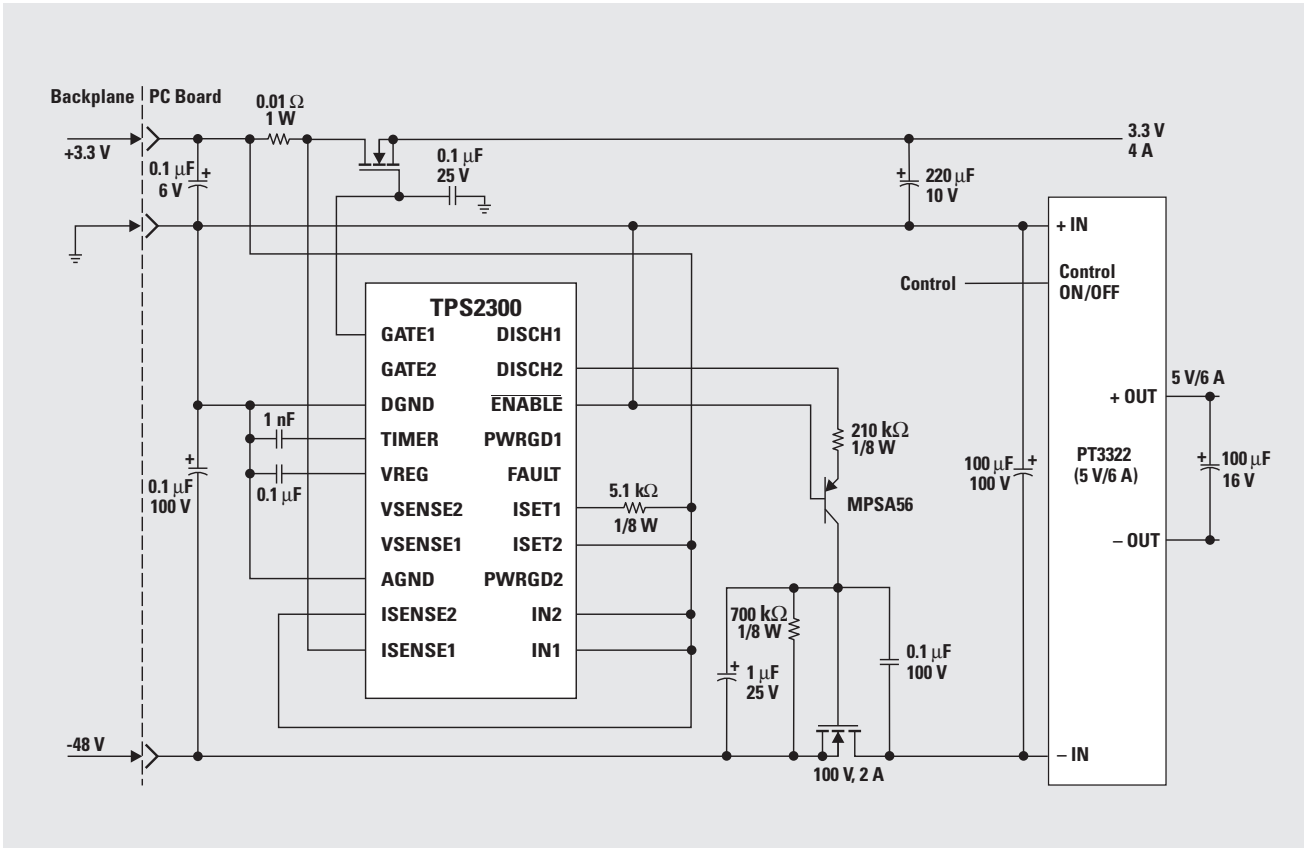
Replace *device* with tps2300, tps2301, tps2310, tps2311, tps2320, tps2321, tps2330, tps2331, ucc3913, ucc3914, ucc3917, or ucc3921

Figure 4. +3.3-V and –48-V hot-swappable supplies



1.6- to 3.6-volt BTL speaker driver reference design

By Ryan Kehr
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Introduction

As supply voltages decrease, there is a need for low-voltage analog solutions to real-world design problems. Consider a system that operates directly from the voltage provided by two single-cell alkaline batteries. When the batteries are fresh, the voltage may be as high as 1.8 V per cell. After depletion, the voltage across a cell may be as low as 0.8 V. While there are many solutions that work above the 2.5-V supply threshold, few amplifiers operate as low as 1.6 V to fully utilize the potential of the battery. The TPA610xA2 family of headphone audio power amplifiers, however, provides adequate output power levels at these low voltages. By bridging the outputs from the two linear amplifiers within the TPA610xA2 device across the speaker load, it is possible to get an increase in output power without increasing the supply voltage. This configuration (shown in Figure 1) is called a bridge-tied load (BTL).

While the schematic in Figure 1 is typical of the output architecture for a dedicated BTL amplifier like the TPA7x1 family of audio power amplifiers, the output structure is not the same in the TPA610xA2 family of devices. Figure 1 shows a non-inverting amplifier driving the high side of the load and an inverting amplifier driving the low side. In contrast, Figure 2 shows the internal circuitry of the TPA6101A2 with two inverting amplifiers driving the differential output.

For the remainder of this article, two different BTL configurations that can be implemented with the TPA610xA2 family will be presented. The first configuration works with a differential-input signal applied to the inputs of the amplifier, while the second configuration is suited for a single-ended input signal applied to one input of the amplifier. Also, thermal considerations need to be addressed with the increase in output power that the BTL configuration provides. Finally, the effect of offset voltages in this configuration will be discussed.

Figure 1. BTL driver

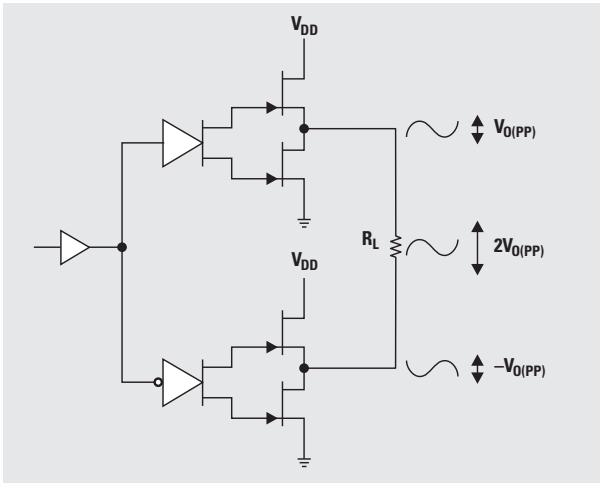
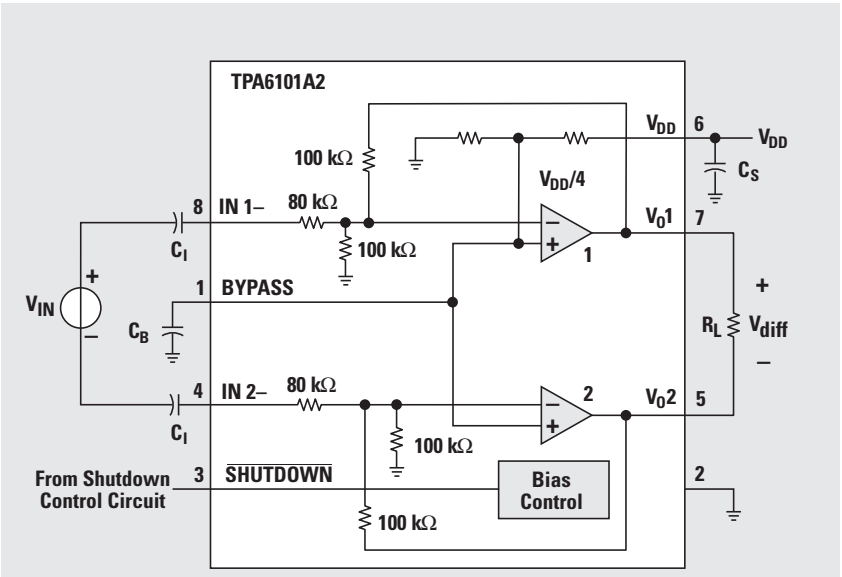


Figure 2. TPA6101A2 configured as a differential-input BTL Driver



Note: All internal resistor values can vary ±20% but will remain matched.

BTL configuration for a differential input

The circuit shown in Figure 2 utilizes the TPA6101A2, which has internal gain-setting resistors for an inverting gain of 2 dB. Since the input signal is connected differentially across the inputs, the outputs are 180° out of phase with respect to each other. With the load connected across the outputs, the differential drive across the load means that one output is moving in the positive direction while the other output is moving in the negative direction. This effectively produces a voltage swing across the BTL that is two times the voltage swing seen across a

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ground-referenced load. Inserting $2V_{O(PP)}$ into Equation 1 and substituting V_{rms} into Equation 2 shows that the power to the load (P_L) increases to four times the power seen across a ground-referenced load. Theoretically, this is four times the power to the load from the same supply voltage and load impedance. In actuality, current limiting and thermal considerations will limit the actual power realizable in this configuration.

$$V_{rms} = \frac{V_{O(PP)}}{2\sqrt{2}} \quad (1)$$

$$P_L = \frac{(V_{rms})^2}{R_L} \quad (2)$$

BTL configuration for single-ended (SE) input

If the inverted output signal of amplifier 1 is connected to the inverting input terminal of amplifier 2, the TPA6100A2 can take an SE audio input and provide an inverted signal to the top side of the resistive load and a non-inverted signal to the low side of the bridge-tied load.

Figure 3 shows an SE input that is capacitively coupled through C1 and connected to the inverting terminal of amplifier 1 through R_I1. Since the positive terminal of amplifier 1 is internally connected to a bias voltage of $V_{DD}/4$, the following transfer function for amplifier 1 is obtained based on an inverting gain of the ac-coupled input signal and a non-inverting gain of the internal bias voltage.

$$V_O1 = V_{IN}\left(\frac{-R_f1}{R_I1}\right) + \left(\frac{V_{DD}}{4}\right)\left(1 + \frac{R_f1}{R1}\right) \quad (3)$$

Therefore, if $R_f1 = R_I1 = R1$, the result is an inverted representation of the input signal biased at $V_{DD}/2$. The gain can be increased to a value greater than 1 by adjusting the ratio of R_f1 and R_I1. However, R1 must be set equal to R_f1 in order to bias the output at mid-rail, maximizing output swing. Notice the connecting wire between the output of amplifier 1 and the input of amplifier 2. Once again, this input is capacitively coupled through C2 to remove the $V_{DD}/2$ bias and is connected to the inverting input of amplifier 2 through R_I2. The feedback network must be set with $R_f2 = R_I2 = R2$ so that amplifier 2 provides an inverting gain of 1 and the output of amplifier 2 is a non-inverted representation of the input multiplied by any gain established by amplifier 1, G_1.

$$G_1 = \frac{R_f1}{R_I1} \quad (4)$$

$$V_O1 = -V_{IN}G_1 + \frac{V_{DD}}{2} \quad (5)$$

$$V_O2 = V_{IN}G_1 + \frac{V_{DD}}{2} \quad (6)$$

$$V_{diff} = V_O1 - V_O2 = -2G_1V_{IN} \quad (7)$$

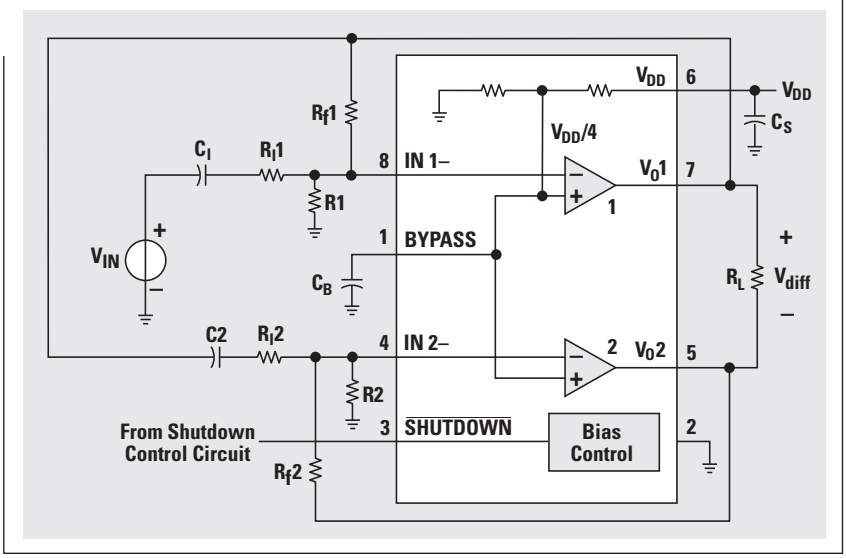
Note that only the TPA6100A2 can be used in this configuration because the gain of the internal amplifiers can be externally set. The remaining members of the device family, the TPA6101A2 and the TPA6102A2, have a fixed gain of 2 dB and 5 dB, respectively. Since the gain is greater than 1, a gain mismatch will exist between the non-inverted and inverted output signals. In the case of the TPA6102A2 with 5 dB of gain, this configuration could cause some large voltage swings across the load with an additional gain of 5 dB in amplifier 2. The differential input configuration (shown in Figure 2) can be constructed with all members of the TPA610xA2 family. The TPA6100A2 device will simply require the use of external resistors, while the other devices will not.

Thermal considerations

Although the bridged amplifier pair will provide four times the power to the load, the power dissipated in the amplifier package will be greater than the normal power dissipated when operated with a ground-referenced load. More power dissipated by the amplifier pair results in more heat that can lead to reliability problems over time. Using maximum allowable junction temperature values for a given power to the load, we can solve for the maximum recommended ambient temperature. Table 1 lists the maximum $I_{DD(rms)}$ for a given junction temperature based on the TPA610xA2 architecture. It also lists the maximum power output for an 8-ohm load where $P_L = I_{DD(rms)}^2 \times R_L$.

By choosing a P_L value from Table 1 that is close to the power desired in the system, we can use Equation 8 to calculate the power dissipated in the amplifier, given a supply voltage (V_{DD}) and load (R_L). For example, if $V_{DD} = 3$ V, $R_L = 8$ ohms, and a desired power of 0.146 W is chosen, we can calculate $P_{dis} = 0.219$ W. By inserting this value into Equation 9 and using the θ_{JA} value for the two available packages, we find that the maximum ambient temperature

Figure 3. TPA6100A2 configured as a SE-input BTL driver



for reliable operation is 58.1°C for the MSOP package and 76.5°C for the SOIC.

$$P_{dis} = \frac{4V_{DD}\sqrt{(2P_L R_L)}}{2\pi R_L} - P_L, \text{ and} \quad (8)$$

$$T_{a(max)} = T_j - \theta_{jA} P_{dis}, \quad (9)$$

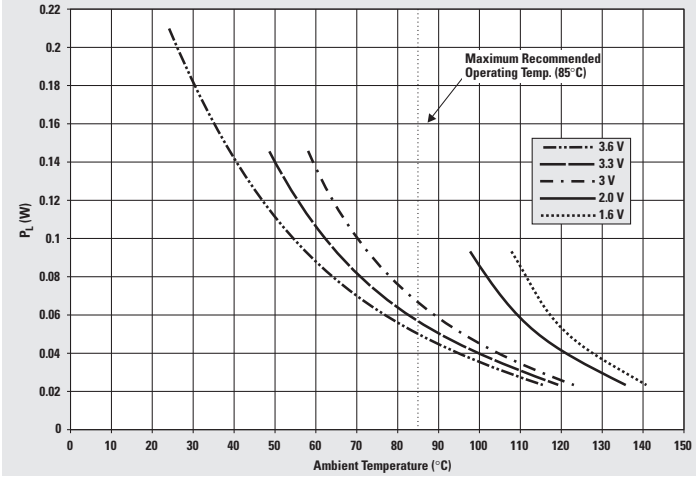
where θ_{jA} = 260°C/W (MSOP) and
θ_{jA} = 176°C/W (SOIC).

Figure 4 is a plot of the maximum ambient temperature vs. power in an 8-ohm load for given supply voltages. The curves are limited to show only the power output possible with the TPA610xA2 configured as a BTL driver. These curves can be used to determine safe operating points for the long- term reliability of the device. Ambient temperatures to the left of the curve represent the "safe zone," while temperatures to the right of the curve are not recommended. The dotted line labeled "maximum recommended operating temperature" indicates that, for proper device functionality, the ambient temperature must not exceed 85°C for the TPA610xA2 family. Using Equations 8 and 9, the circuit designer can generate curves for different loads and a different package.

Table 1. Junction temperature as it relates to P_L

JUNCTION TEMP. MAXIMUM (°C)	$I_{DD(rms)}$ MAXIMUM (mA)	P_L MAX. (8-ohm LOAD) (W)
89	270	0.583
102	189	0.286
106	162	0.210
115	135	0.146
124	108	0.093
137	81	0.052
150	54	0.023

Figure 4. Power vs. maximum ambient temperature for an 8-ohm load (MSOP package)

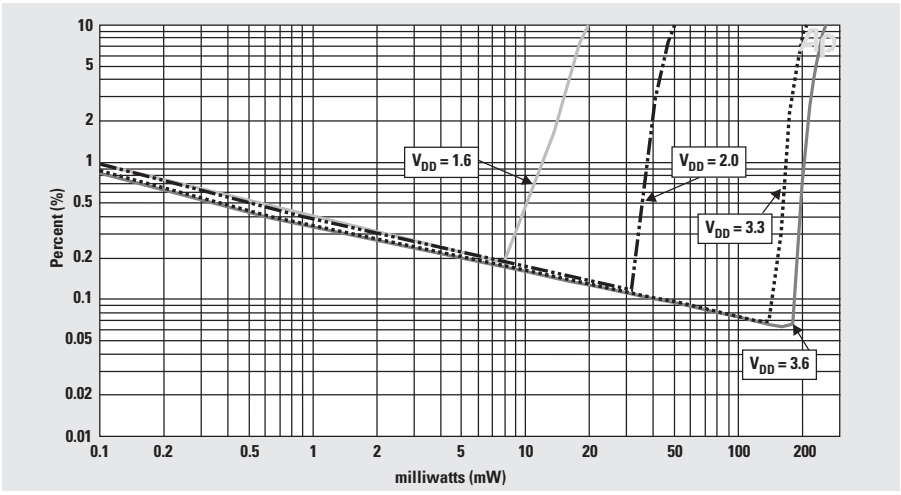


DC offsets in the BTL

Each amplifier in the TPA610xA2 will have an inherent offset voltage associated with it. If the offsets are of equal magnitude and sign, they will cancel across the BTL just like the $V_{DD}/2$ bias. However, the worst-case scenario for the differential input configuration is an offset of equal and opposite sign. In this case, the dc offsets will add across the load. The offset of the TPA610xA2 is typically 2 mV. With the worst-case scenario, that would result in 4 mV across the load. The worst-case in the single-ended case is also an offset of equal magnitude and opposite sign in each amplifier. Since the output of channel 1 is connected to the input of channel 2 through a series capacitor, the worst-case offset is again equal to 4 mV.

The offset for this particular device is not of great concern. If the offset was larger, it could cause overheating in the speaker voice coil due to the constant power dissipated in the coil. A large offset will also cause displacement of the speaker cone from the normal rest position, which could cause distortion and damage the speaker in the long term.

Figure 5. THD+N vs. power for an 8-Ω load at V_{DD} = 1.6, 2.0, 3.3, and 3.6 V



Results

The differential circuit shown in Figure 2 and the single-ended circuit shown in Figure 3 were examined in the lab with an Audio Precision™ (AP) instrument to measure total harmonic distortion plus noise (THD+N) vs. power across the load. Both circuits produced nearly identical results, so only the single-ended input circuit plots are shown. The plots in Figures 5-7 show data taken with an 8-, 16-, and 32-ohm load, respectively. There are four traces within each plot that represent 1.6-, 2-, 3.3-, and

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3.6-V supply voltages. As shown in Figure 7, the maximum power achieved with 0.1% distortion into a 32-ohm load is approximately 110 mW at 3.3 V and 16 mW at 1.6 V. It is expected that as the load decreases, the power should increase based on Ohm's law. However, the curves in Figure 5 show a decrease of about 8 mW going from 32 ohms to 8 ohms for a 1.6-V supply.

This can be explained by understanding the maximum voltage swing possible at the different supply voltage rails and the current necessary to drive the BTL configuration. Since each amplifier in the BTL configuration is effectively driving half of the load resistance, each amplifier must source 2x the current sourced when the load was referenced to ground. Each amplifier is capable of driving within a few hundred millivolts of each rail for a 10-kΩ load. As this load decreases, the amplifier can no longer source the current necessary to drive the signal to the rail, and clipping will occur at some voltage from the rail. The voltage drop from the rail will continue to increase as the load decreases. Reducing the supply voltage to 1.6 V further complicates the problem because, as V_{DD} decreases, the available voltage to enhance the MOSFET output drivers also decreases. This results in higher $r_{DS(on)}$ values and larger voltage drops from the rail. With all of this in mind, it is a good idea to set the gain of the amplifier to a level that will limit clipping at the lowest expected supply voltage.

Figure 6. THD+N vs. power for a 16-Ω load at V_{DD} = 1.6, 2.0, 3.3, and 3.6 V

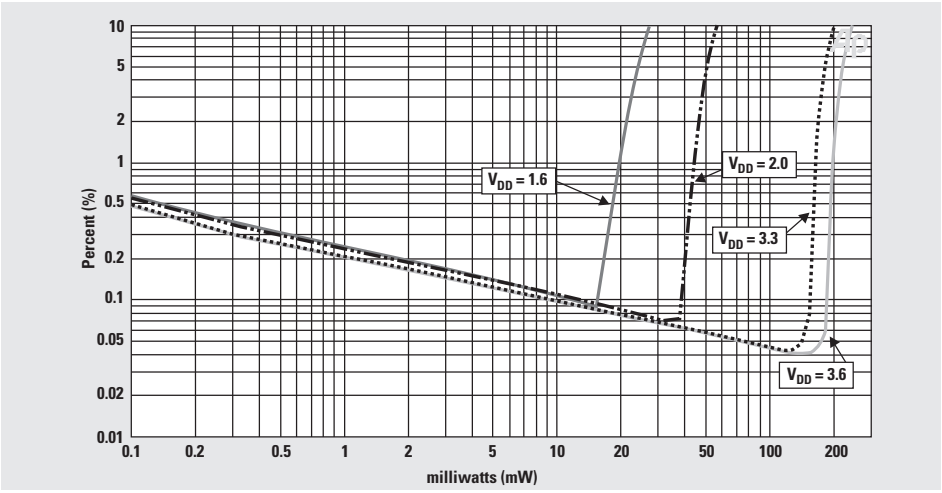
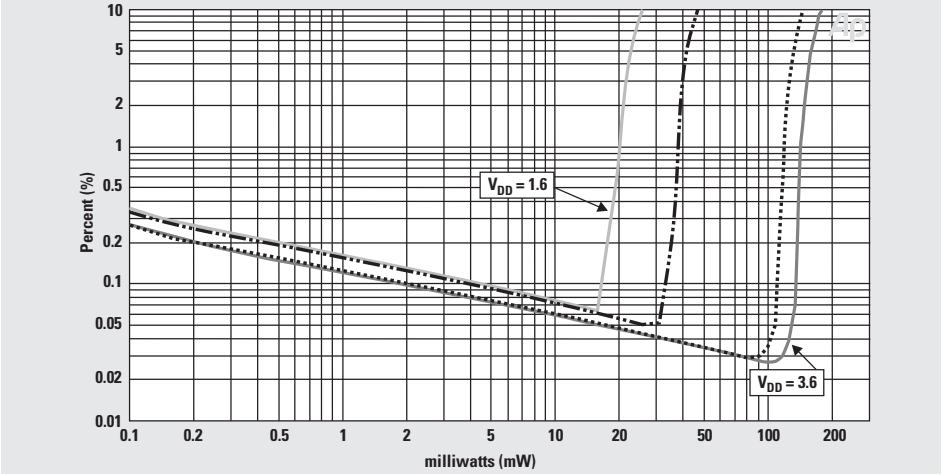


Figure 7. THD+N vs. power for a 32-Ω load at V_{DD} = 1.6, 2.0, 3.3, and 3.6 V



Conclusion

While the TPA610xA2 family was not originally designed as a BTL driver, it can be configured as such for both single-ended and differential inputs and used over the full range of two single-cell alkaline batteries. Careful consideration should be given to the thermal limitations of the package chosen and the power desired across the load. For supply voltages that are held above 2.5 V, the TPA7x1 family of audio power amplifiers or the TPA0211 is recommended to provide better drive capability at 2.5 V and up to 5.5 V. These devices are also available in the PowerPAD™ package to alleviate some of the thermal stresses on the device at these power levels.

Related Web sites

www.ti.com/sc/amplifiers

www.ti.com/sc/docs/package/pkg_info.htm

www.ti.com/sc/docs/tools/analog/amplifierdevelopmentboards.html

Get product data sheets at:
www.ti.com/sc/docs/products/analog/*device*.html
Replace *device* with tpa6100a2, tpa6101a2, tpa6102a2, tpa741, tpa731, tpa721, tpa711, tpa701, or tpa0211

Notebook computer upgrade path for audio power amplifiers

By Richard Palmer
Application Specialist, Audio Amplifiers

Introduction

Notebook PCs are constantly changing, and their requirements for audio power amplifiers (APAs) are also changing. TI has been releasing new APAs for notebook PCs to meet the market's needs. New features added to the original innovative device, the TPA0102, have improved system functionality and performance.

The TPA0212/0312 offer internal gain settings to reduce external components; differential inputs for noise reduction; and lower supply currents. The TPA0232 adds dc volume control, while the TPA0252 has digitally controlled volume control. The newest device, the TPA2000D4, is a filterless class-D device with an integrated headphone drive. It offers higher efficiency for extended battery runtimes, as well as reduced thermal dissipation.

A simplified block diagram of a notebook computer is shown in Figure 1. There are several ways to configure and interface the APA, each discussed later in this article. For more information on the audio or overall PC system, see Reference 1. Each of the devices listed in this article is suitable for use in notebook PCs, sub-notebooks, or personal digital assistants (PDAs).

External gain amplifiers (TPA0102 and TPA0202)

These devices can take the audio signal directly from the AC '97 Codec, conditioning the signal gain and enabling it to drive low-impedance speakers. Optional equalization can be added between the AC '97 Codec and the APA to improve speaker fidelity by electronically flattening its response. This equalization can be done either with analog techniques using operational amplifiers, or digitally with a device like the TAS3002 digital EQ IC from TI. Figure 2 on the following page shows the TPA0202 set up in the optimal circuit configuration.

There are two sets of inputs (RLINEIN/LLINEIN and RHPIN/LHPIN) feeding an input MUX. The HP/$\overline{\text{LINE}}$ terminal controls the input MUX. This allows independent gain settings for the internal speakers and the headphones, which allows the loudness to be matched between the speakers and the headphones. Alternately, one set of inputs can be connected to the AC '97 Codec, and the other set can be connected to the analog output of the CD-ROM, allowing a mode of operation where audio CDs may be played without powering the entire notebook. Another option is to use one set of inputs for the equalized signal and the other set for the flat signal for the headphones, as they should not be equalized.

The SE/$\overline{\text{BTL}}$ terminal controls the negative output amplifier stage. In BTL mode, this amplifier is enabled, driving the speaker in BTL mode. In SE mode, the negative output amplifier is in a high-impedance state, effectively muting the internal speakers so no sound is heard from them when the headphones are in use.

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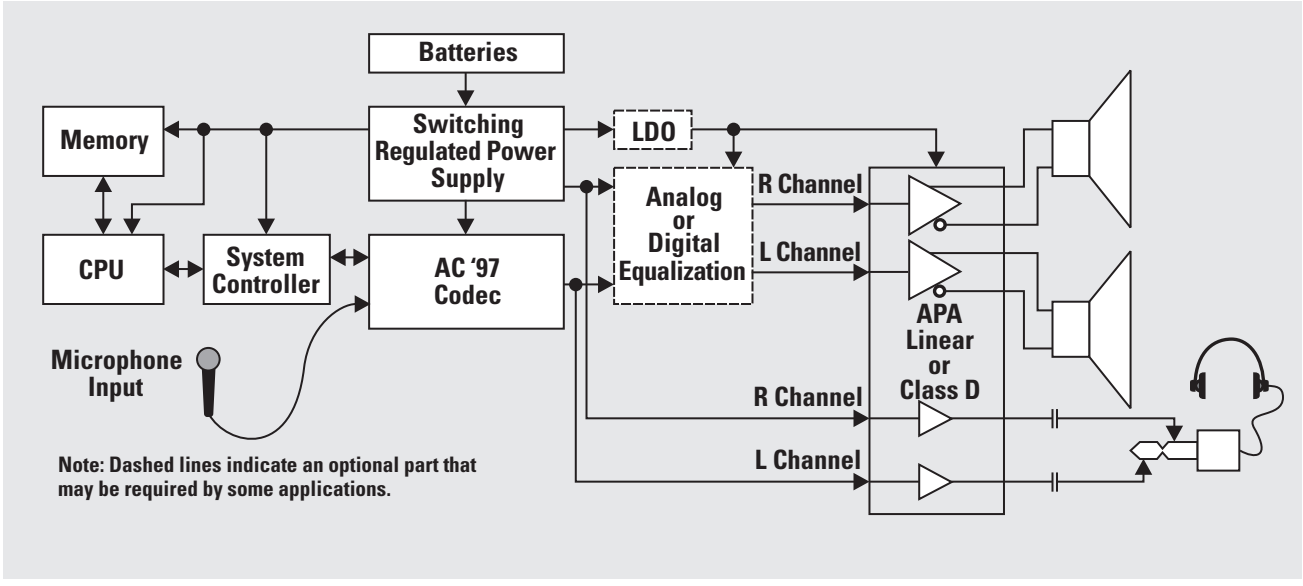
Figure 1. Simplified block diagram of the audio portion of a notebook PC



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The TPA0102 and TPA0202 use one internal stage for amplification and power output. Minimum distortion is therefore achieved by keeping the gain as low as possible, with a gain of –2 V/V (BTL) providing the highest SNR and lowest distortion in the load. The speaker gain is set by Equation 1, and the headphone gain is set by Equation 2. There are three considerations when choosing these resistors. The first is that high resistance values create a large time constant with the input ac-coupling cap, C_{IN}. When the amplifier is placed in shutdown mode, the midrail dc biasing voltage (BYPASS) drifts to ground. If Equation 4 is not satisfied, the start-up pop will increase. The second consideration is that the larger the gain of the circuit, the larger the start-up pop. The third consideration is the creation of a pole at $f = (2\pi R_{IN}C_{IN})^{-1}$. This cutoff frequency must be set to pass the desired low-end audio frequencies.

$$\text{Gain (speaker)} = -2\left(\frac{R_{F(Line)}}{R_{IN(Line)}}\right) \quad (1)$$

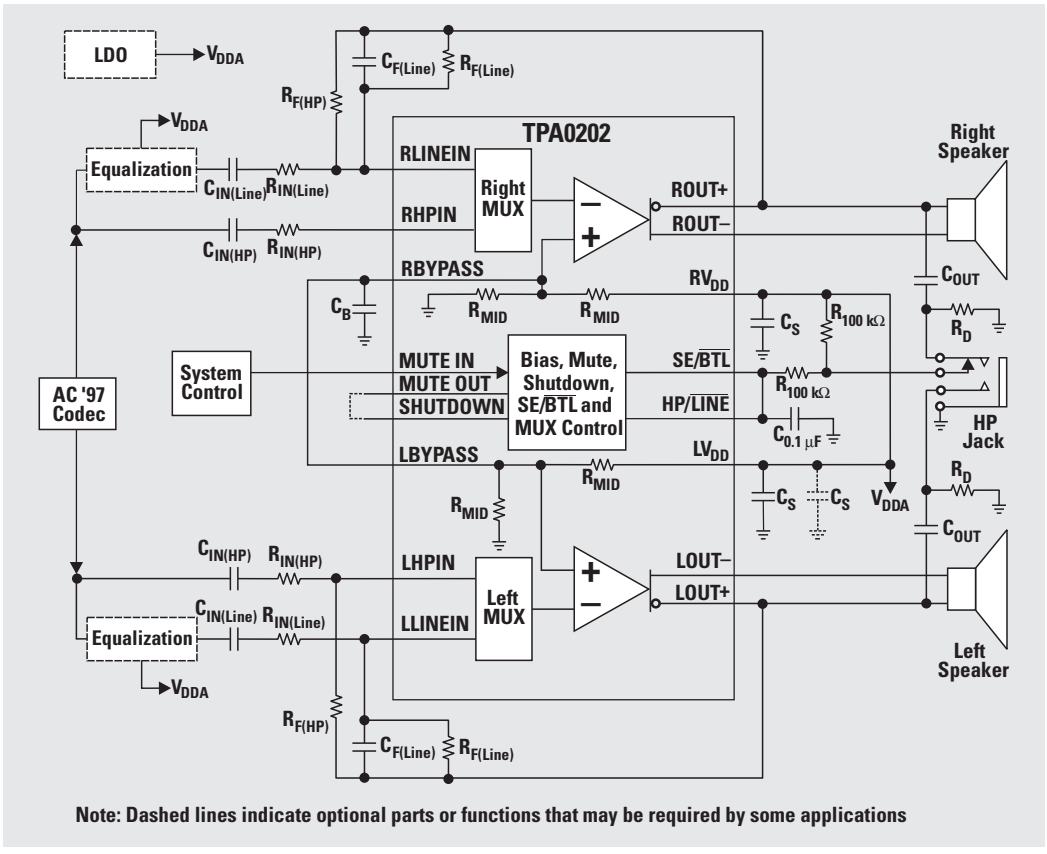
$$\text{Gain (HP)} = -\left(\frac{R_{F(HP)}}{R_{IN(HP)}}\right) \quad (2)$$

The major differences between the two amplifiers are that the TPA0102 is capable of driving 1.5 W into a 4-Ω load, while the TPA0202 can drive 2 W into a 3-Ω load and has internal de-pop circuitry added to reduce start-up popping in the speakers. The remaining features are virtually identical, so the consideration becomes the selection of the capacitors for the circuit: ac coupling, bypass, and bulk decoupling of the power supply.

The AC '97 Codec's outputs may not be biased at the same voltage as the APA inputs; thus dc blocking capacitors are required to ac-couple the two ICs to prevent distortion in the APA. Single-ended inputs are sensitive to noise since any common-mode noise will be amplified by the APA. Careful layout reduces noise pickup. Shield the input traces from noisy digital signals, and keep the input and feedback resistors as close as possible to the APA inputs, since their high-impedance nodes are likely to pick up noise. The outputs to the single-ended load must be ac-coupled (C_{OUT}) to block any dc component from the APA, preventing a dc current from flowing through the speaker. In both cases, these capacitors combine with the series resistance (C_{IN} with R_{IN}, and C_{OUT} with the headphone resistance) to create a high-pass filter with a cutoff frequency of $(2\pi RC)^{-1}$. Ceramic capacitors are used at the inputs since R_{IN} is large. The SE output requires an electrolytic capacitor because the small resistance of the headphones requires a large capacitance to get a low cutoff frequency.

The supply decoupling capacitors (C_S) are located at the power-supply pins (RV_{DD} and LV_{DD}). The C_S capacitors decouple high-frequency signals, such as transients and spikes, from the power supply. The C_B capacitors decouple high-frequency signals that couple into the midrail biasing circuit, and help minimize the startup pop by controlling the voltage on the non-inverting terminal. Each capacitor should be a low impedance over the expected noise frequency range. The range of noise is determined by the noise sources in the system. In a notebook PC, the primary source is the hard-disk drive (HDD). The noise is caused by the rise time of the digital components as they switch on and off. According to Reference 2, the maximum frequency of this noise is calculated with Equation 3, where t_r is the rise time of the digital pulse. Periodic signals

Figure 2. TPA0202 application circuit



Note: Dashed lines indicate optional parts or functions that may be required by some applications

require filtering from their frequency up to this maximum frequency. Non-periodic signals should be filtered from dc up to f_{max}.

$$f_{max} \approx \left(\frac{1}{\pi t_r}\right) \quad (3)$$

Two capacitors may be required to implement effective noise decoupling with C_S, depending upon the range of the noise. If there is low-frequency noise, then bulk capacitance may be required and is placed in parallel with the high-frequency capacitor. In this case the high-frequency capacitor must be placed closer to the pin. Capacitor C_B acts as a virtual ac ground, allowing operation from a single supply. The selection of C_B is based on two criteria—it should be a low impedance over the expected noise frequency range, and it must satisfy Equation 4.

$$\left(\frac{1}{2\pi C_B \times 100\ k\Omega}\right) \leq \left[\frac{1}{2\pi C_{IN}(R_{IN}+R_F)}\right] \quad (4)$$

The relationship shown in Equation 4 reduces the pop as much as possible. The size of the capacitor directly influences PSRR, particularly at frequencies of less than 1 kHz. The larger the capacitor, the better the PSRR, but the longer the start-up time. See Figure 12 in Reference 3 as an example. Keep in mind that the noise introduced at the bypass pins will manifest as degraded PSRR and increased THD+N in the APA. R_{IN} and R_F may be increased if a larger value of C_B is required for noise decoupling. For the power supply and bypass pin decoupling, good-quality ceramic capacitors effectively decouple noise in the range of tens of kilohertz to hundreds of megahertz. Tantalum or aluminum electrolytic capacitors are good for decoupling frequencies from the tens of kilohertz down to a few hertz.

Internal selectable fixed gain (TPA0212 and TPA0312)

The TPA0212 and TPA0312 have features similar to the TPA0202 and, in addition, have the following enhancements.

- Fully differential or single-ended inputs
- Selectable, internal gains
- Improved depop
- PC-BEEP option
- Compatible with PC2001 Desktop Line-out into a 10-kΩ load

The TPA0312 has gains that are compatible with audio Codecs operating at 3 V but is otherwise similar to the TPA0212.

Figure 3 shows the TPA0212 configured for differential inputs. The line inputs can be configured as fully differential if the positive input terminal is connected to the RIN or LIN pins, the negative terminal is connected to the RLINEIN and LLINEIN pins, and the HP terminals are left

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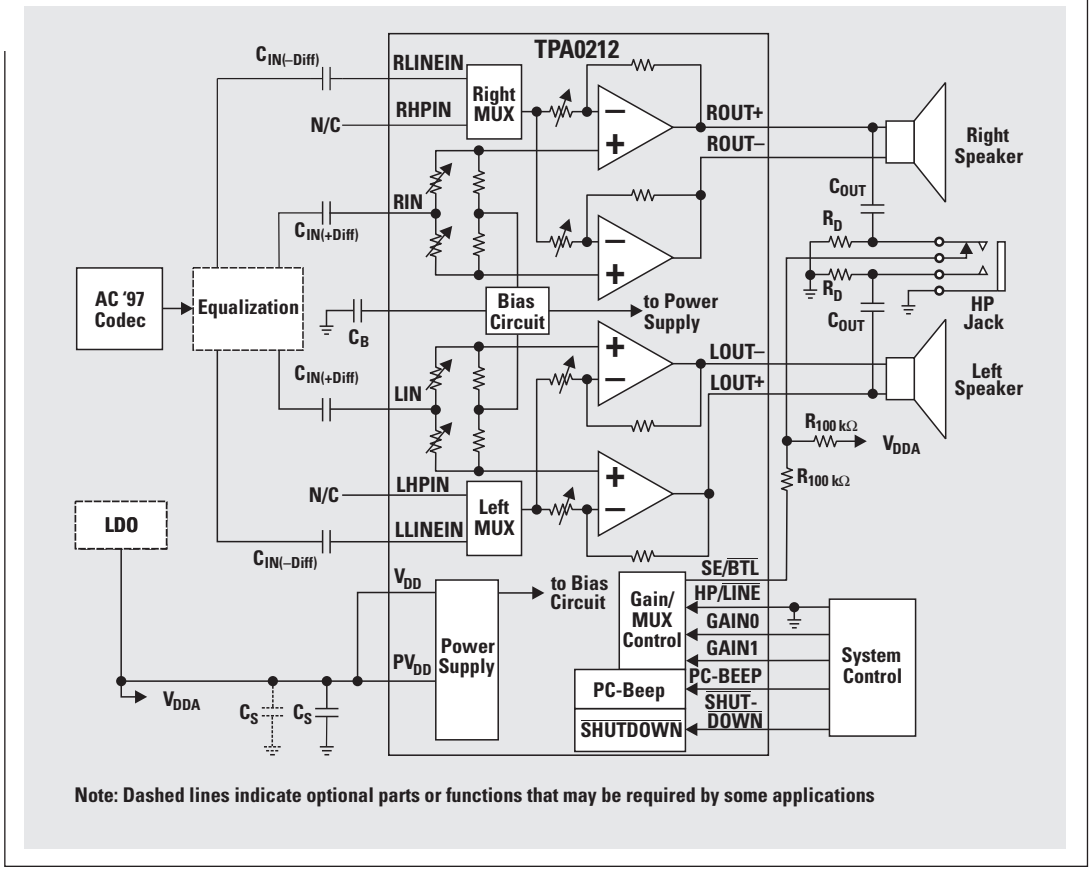
Figure 3. Simplified TPA0212 application circuit using differential inputs



Note: Dashed lines indicate optional parts or functions that may be required by some applications

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floating. This is done because the RHPIN/LHPIN and RLINEIN/LLINEIN inputs go to the MUX and then are applied to the inverting input of the internal amplifier, while the RIN/LIN inputs are tied to the non-inverting input. When single-ended inputs are used, the RIN/LIN pins are grounded through a capacitor of the same value as the audio signal inputs.

Table 1. Variable gain settings of the TPA0212 and TPA0312

GAIN0	GAIN1	SE/$\overline{\text{BTL}}$	GAIN (dB)	
			TPA0212	TPA0312
0	0	0	6.0	5.6
0	1	0	15.5	9.5
1	0	0	21.5	15.1
1	1	0	27.6	21.1
X	X	1	0.0	4.1

The internal gain control is selected by the combination of two input terminals (GAIN0 and GAIN1) used in conjunction with the SE/$\overline{\text{BTL}}$ pin. Table 1 shows the gain combinations available for both the TPA0212 and TPA0312. The gain is variable for the BTL output to allow for varying efficiencies of different speaker types and varying input amplitudes from the equalization circuitry or some other signal conditioning. The gain can also be used as a limited volume control. The SE gain provides the optimal level of sound in headphones. It also minimizes start-up pop and allows a large output signal swing from the AC '97 Codec, maximizing the SNR. The input impedance varies with gain and will impact the cutoff frequency of the input filter. Assume a worst-case minimum of 10 kΩ to calculate C_{IN}.

The depop circuitry is improved and does not require any special circuits or considerations to minimize it. Choice of C_B is not directly linked to the input filter components. C_B is recommended to be between 0.47 µF and 1 µF for minimum THD+N.

The PC Beep allows the system processor to send a tone signal to the speaker through the PC-BEEP pin. The amplifier output is switched to BTL when the input is a pulse train or square wave signal of 1 V_{PP} or greater, with rise and fall times of less than 1 µs and a minimum of 8 rising edges. This signal is passed to the speaker with a fixed gain of 0.3 V/V, independent of the gain setting. The PC-BEEP pin is dc-biased at midrail. When it is ac-coupled, the value of the beep coupling capacitor (C_{PCB}) should be calculated with Equation 5, where R_{PCB} = 100 kΩ is the input impedance of the PC-BEEP pin and f_{PCB} is the frequency of the control signal.

$$C_{PCB} \geq \left(\frac{1}{2\pi f_{PCB} R_{PCB}} \right) \quad (5)$$

DC or digital gain control (TPA0232 and TPA0252)

The TPA0232 provides all the features of the TPA0212 plus a dc gain (VOLUME) control. Refer to Figure 3. The GAIN0 pin becomes HP/$\overline{\text{LINE}}$, the GAIN1 pin becomes the VOLUME, and the old HP/$\overline{\text{LINE}}$ pin becomes the CLK. A dc voltage applied directly to the VOLUME pin controls the amplifier gain. The dc level sets the gain from –40 dB to +20 dB in 31 discrete steps. The gain is 20 dB for 0 V to 0.15 V and decreases in 2-dB increments for approximately every 120 mV. The volume is muted when the output exceeds 3.54 V. The precise values are listed in the application section of Reference 4.

The CLK pin requires a fixed 0.47-nF capacitor to ground for optimal circuit performance when the internal clock is used, which sets the clock frequency to 100 Hz. The maximum internal clock frequency is 500 Hz. The formula for calculating either C_{CLK} or f_{CLK} is shown in Equation 6.

$$f_{CLK} = \frac{4.7 \times 10^{-6}}{C_{CLK}} \quad (6)$$

An external clock can override the internal clock by removing the capacitor and applying it directly to the CLK terminal. The maximum input frequency is 10 kHz, though it should be kept at less than 200 Hz for normal operation to prevent the gain from increasing too quickly and creating pop or zipper noise in the speaker. The waveform should be a 5-V, 50%-duty-cycle square wave to operate the 4.5-V and 0.5-V trip points. In notebook PC applications, internal speakers must be driven using the single-ended (SE) mode. The device automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ pin is pulled high and the gain is reduced by 6 dB from the BTL setting. See the application section of Reference 4 for more information.

The TPA0252 also provides the features of the TPA0212 plus a two-pin digital input volume control and an auxiliary volume control memory pin (V_{AUX}). The digital input volume control has two active low-input control pins (UP/DOWN). The default volume is initially set at –10 dB and is increased or decreased in 31 discrete, 2-dB steps over a range from –40 dB to +20 dB in BTL mode. When in SE mode, the gain is 6 dB lower than the BTL gain for the same input. An active low voltage on the UP pin causes the gain to increase, and on the DOWN pin causes the gain to decrease. When the UP/DOWN pin is held low, the gain will increase/decrease by 2 dB per clock cycle.

The volume control works in conjunction with the CLK, which functions as described for the TPA0232. The V_{AUX} terminal is used to maintain power to the volume control memory. The device will remember the last volume setting when a voltage of greater than 3 V is applied to the V_{AUX} terminal, even when the device is powered down or in shutdown mode. When V_{AUX} is pulled low, the device resets to a volume setting of –10 dB in BTL mode. See the application section of Reference 5 for more information.

Class-D high-efficiency APA (TPA2000D4)

The TPA2000D4 is a class-D APA capable of filterless operation and offers many of the features of the TPA0212, with some additional benefits:

- Greater efficiency: 70% filterless vs. 25% class-AB APA, providing these benefits:
  - longer battery life
  - lower supply-current demand from LDO
  - less heat due to less internal power dissipation
- Multiple internal BTL gains
- Fully differential inputs with SE HP inputs
- Lower shutdown current: 1 µA vs. 150 µA

The efficiency of the TPA2000D4 is its greatest advantage, offering longer battery life, lower supply current, and less

heat. These are important factors as the notebook computer market struggles to attain longer operation for the system. The new modulation scheme and filterless operation allow great reductions in size and cost as well as in the quiescent current and supply current drawn while playing audio.

The TPA2000D2, which is a similar part but without the headphone amplifier, passed FCC- and CE-radiated emissions with no shielding and a speaker wire 8" long or less. This is ideal for the notebook computer, where trace/wire length is short. For longer leads, the device can be used with a ferrite bead or complete LC filter. See the application section of Reference 6 for more details.

The differential inputs can be configured for SE operation by ac grounding the RINP and LINP pins with the same capacitance used on the audio inputs. The same considerations apply as for the TPA0212 amplifier already discussed, with the exception of the input capacitor, which must be at least 10 times smaller than the midrail capacitor on the bypass pin, C_B, to reduce the startup popping. The values that change are the input impedance, which is a minimum of 20 kΩ, and the actual gain levels. The gain is set with 2 input terminals similar to those for the TPA0212. The midrail bypass capacitor, C_B, also performs the same function and should be 1 µF. The power-supply pin decoupling now requires two capacitors, one high- and one low-frequency, to filter out the noise of the system. The same rules apply as before for the placement and type of capacitor chosen. It is critical that the high-frequency decoupling capacitor(s) be placed as close as possible to the IC pins.

Acknowledgments

I would like to thank the following people for their time, assistance, and patience, which made this article possible: Don Dapkus, APA Section Manager, Applications and Product Definition; Mike Score, APA Systems Engineer and Member, Group Technical Staff; and Eric Droge, APA Marketing Manager.

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1. Intel Corporation and Microsoft Corporation, “PC 2001 System Design Guide” (November 2, 2000), www.pcdesguide.org/pc2001/default.htm
2. Henry W. Ott, Noise Reduction Techniques in Electronic Systems (John Wiley & Sons, 1976).

For TI information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *“litnumber”* with the **TI Lit. #** for the following document.

Document Title	TI Lit. #
3. “TPA0213 2-W Mono Audio Power Amplifier with Headphone Drive,” Data Sheet	slos276
4. “TPA0232 Stereo 2-W Audio Power Amplifier with DC Volume Control and MUX Control,” Data Sheet	slos286
5. “TPA0252 Stereo 2-W Audio Power Amplifier with Digital Volume Control,” Data Sheet	slos288
6. “TPA2000D4 Stereo 2-W Class-D Audio Power Amplifier with Stereo Headphone Amplifier,” Data Sheet	slos337
7. “TPA0212 Stereo 2-W Audio Power Amplifier with Four Selectable Gain Settings and MUX Control,” Data Sheet	slos284
8. “TPA0312 2-W Stereo Audio Power Amplifier with Four Selectable Gain Settings and MUX Control,” Data Sheet	slos335

Related Web sites

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Replace *device* with tpa0102, tpa0202, tpa0212, tpa0232, tpa0252, tpa0312, tpa2000D2, or tpa2000D4

Fully differential amplifiers applications: Line termination, driving high-speed ADCs, and differential transmission lines

By Jim Karki
Systems Specialist, High-Performance Linear

Introduction

The August 2000 issue of *Analog Applications Journal* introduced the fully differential amplifiers from Texas Instruments and illustrated their basic operation. In the November 2000 issue we delved into the topic more deeply by analyzing gain and noise. In this issue we investigate some typical applications like transmission lines and driving ADC inputs.

To simplify calculations and formulas, we will assume that the amplifier is being used at frequencies where the open-loop gain is very large ($A_F >> 1$) and will not include its effects in the analysis.

The circuit analysis assumes that symmetrical feedback is being used ($\beta 1 = \beta 2$). Before going into the application circuits, we will detour briefly into how termination affects the feedback factor and how to account for it.

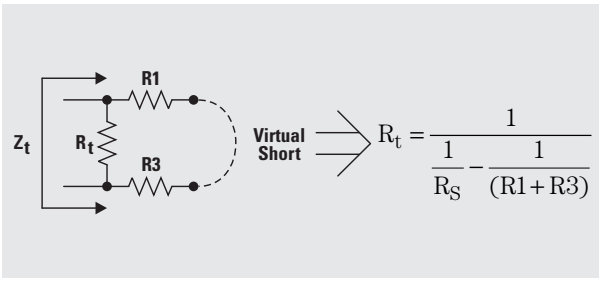
Terminating the input source

Double termination is typically used in high-speed systems to reduce transmission-line reflections. With double termination, the transmission line is terminated with the same impedance as the source. Common values are 50 W, 75 W, 100 W, and 600 W. When the source is differential, the termination is placed across the line. When the source is single-ended, the termination is placed from the line to ground.

Figure 1 shows an example of terminating a differential signal source. The situation depicted is balanced so that half of V_S and half of R_S is attributed to each input, with V_{IC} being the center point. R_S is the source impedance and Rt is the termination resistor. The circuit is balanced, but there are two issues to resolve: (1) proper termination and (2) gain setting.

As long as $A_F >> 1$ and the amplifier is in linear operation, the action of the amplifier keeps $V_N \approx V_P$. Thus, to first-order approximation, a virtual short is seen between the two nodes as shown in Figure 2. The termination impedance is the parallel combination: $R_t \parallel (R1+R3)$. The value of Rt for proper termination is calculated as shown in Figure 2.

Figure 2. Differential termination impedance



Once R_t is found, the required gain is found by generating a Thevenin equivalent circuit. The circuit is broken between R_t and the amplifier input resistors R1 and R3. V_{IC} does not concern us at this point, so we will leave it out. Then

$$V_{TH} = V_S \times \frac{R_t}{R_t + R_S},$$

and $R_{TH} = R_S \parallel R_t$ (half is attributed to each side). The resulting Thevenin equivalent is shown in Figure 3. The proper gain is calculated by

$$\frac{V_{OUT}}{V_{TH}} = \frac{R_F}{R_G + \frac{R_S \parallel R_t}{2}},$$

where $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$.

Figure 1. Terminating a differential input signal

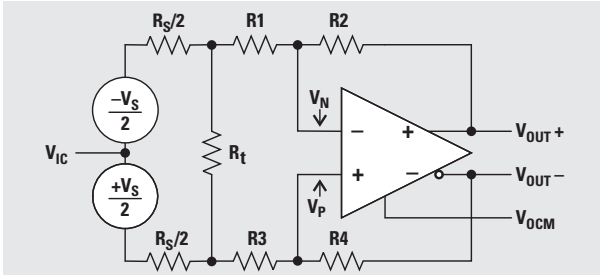
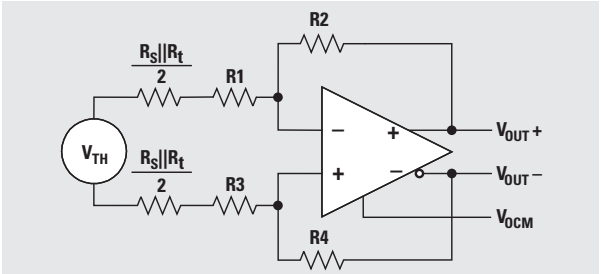


Figure 3. Differential Thevenin equivalent



Substituting for V_{TH}, this becomes

$$\frac{V_{OUT}}{V_S} = \frac{R_F}{R_G + \frac{R_S \parallel R_t}{2}} \times \frac{R_t}{R_S + R_t},$$

where R_F is the feedback resistor (R2 or R4), and R_G is the input resistor (R1 or R3). Remember: for symmetry, keep the gain equal on the two sides with

R2 = R4 and R1 = R3.

As an example, suppose you are terminating a 50-Ω differential source that is balanced, and you want an overall gain of 1 from the source to the differential output of the amplifier. Start the design by first choosing the values for R1 and R3, then calculate R_t and the feedback resistors.

With the voltage divider formed by the termination, it is reasonable to assume that a gain of about 2 will be required in the amplifier. Also, feedback resistor values of approximately 500 Ω are reasonable for a high-speed amplifier. Using these starting assumptions, choose R1 and R3 equal to 249 Ω. Next calculate R_t from the formula:

$$R_t = \frac{1}{\frac{1}{R_S} - \frac{1}{(R1 + R3)}} = \frac{1}{\frac{1}{50} - \frac{1}{(249 + 249)}} = 55.6\ \Omega$$

(the closest standard 1% value is 56.2 Ω). Then set the gain by calculating the value of the feedback resistors:

$$R_F = \frac{V_{OUT}}{V_S} \times \left(R_G + \frac{R_S \parallel R_t}{2} \right) \times \frac{R_S + R_t}{R_t}$$

$$= 1 \times \left(249 + \frac{50 \parallel 56.2}{2} \right) \times \frac{50 + 56.2}{56.2} = 495.5\ \Omega$$

(the closest standard 1% value is 499 Ω). The solution is shown in Figure 4 with standard 1% resistor values.

Figure 4. Differential solution for gain = 1

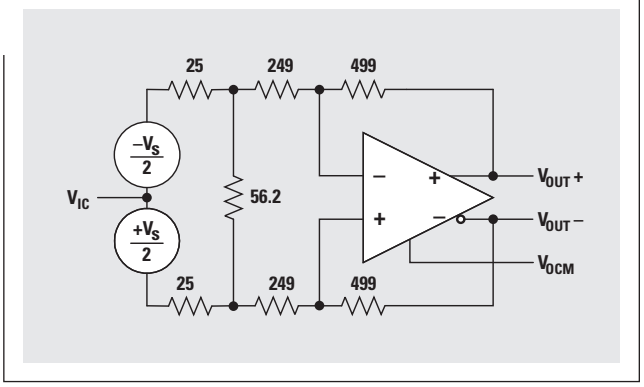


Figure 5. Terminating a single-ended input signal

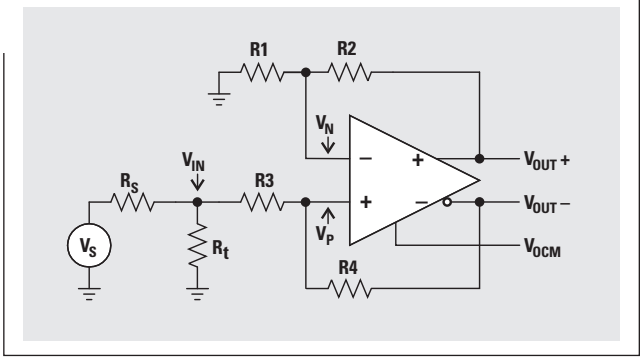
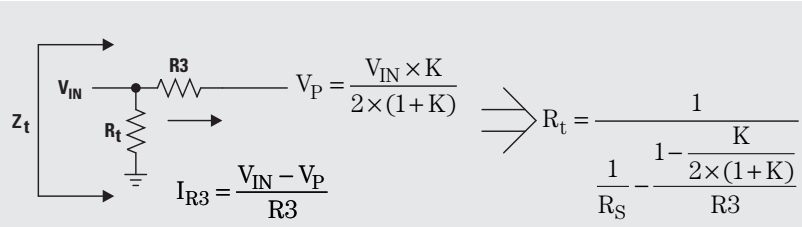


Figure 5 shows an example of terminating a single-ended signal source. R_S is the source impedance, and R_t is the termination resistor. The circuit is not balanced, so there are three issues to resolve: (1) proper termination, (2) gain setting, and (3) balance.

Figure 6. Single-ended termination ac impedance



To determine the termination impedance seen from the line looking into the amplifier's input at V_{IN}, remove V_S and R_S and short all other sources. As long as $A_F >> 1$ and the amplifier is in linear operation, the action of the amplifier keeps $V_N \approx V_P$. V_N will see the voltage at $V_{OUT}+$ divided by the resistor ratio

$$\frac{R1}{R1 + R2}.$$

Assuming that the amplifier is balanced,

$$V_{OUT}+ = K \times \frac{V_{IN}}{2},$$

where K is the closed-loop gain of the amplifier ($V_{OCM} = 0$). The termination impedance is the parallel combination: R_t in parallel with

$$\frac{V_{IN}}{I_{R3}} = \frac{R3}{1 - \frac{K}{2 \times (1 + K)}}.$$

The value of R_t for proper termination is then calculated as shown in Figure 6.

Once R_t is found, the required gain is found by generating a Thevenin equivalent circuit. The circuit is broken between Rt and the amplifier's input resistor R3.

$$V_{TH} = V_S \times \frac{R_t}{R_t + R_S},$$

and $R_{TH} = R_S \parallel R_t$.

Continued on next page

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The resulting Thevenin equivalent is shown in Figure 7. The gain is set by

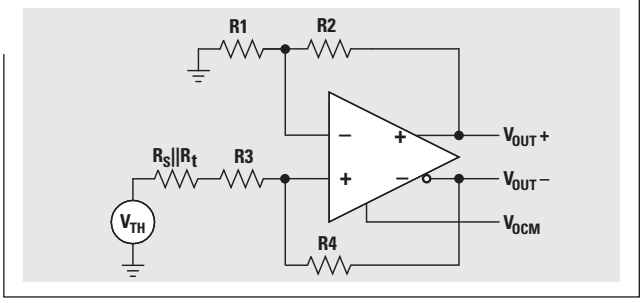
$$\frac{V_{OUT}}{V_{TH}} = \frac{R_F}{R_G},$$

where R_F = R2 = R4, R_G = R1 = R3 + $R_S \parallel R_t$, and V_{OUT} = (V_{OUT}+) – (V_{OUT}–). Substituting for V_{TH}, this becomes

$$\frac{V_{OUT}}{V_S} = \frac{R_F}{R_G} \times \frac{R_t}{R_S + R_t}.$$

Remember, for symmetry: R2 = R4 and R1 = R3 + ($R_S \parallel R_t$).

Figure 7. Single-ended Thevenin equivalent



As an example, suppose you are terminating a 50-Ω single-ended source and want an overall gain of 1 from the source to the differential output of the amplifier. Start the design by first choosing the value for R3, then calculate R_t and the feedback resistors. This will be an iterative process, starting with some initial assumptions that are then refined.

Start with the assumptions that R_t = 50 Ω and that a gain of 2 will be required in the amplifier. Also, feedback resistor values of approximately 500 Ω are reasonable for a high-speed amplifier. Using these starting assumptions, choose R1 = 249 Ω and R3 = R1 – $R_S \parallel R_t$ = 249 Ω – 25 Ω = 224 Ω. Next calculate R_t from the formula:

$$R_t = \frac{1}{\frac{1}{R_S} - \frac{1 - \frac{K}{2(1+K)}}{R3}} = \frac{1}{\frac{1}{50} - \frac{1 - \frac{2}{2(1+2)}}{224}} = 58.7\ \Omega.$$

Then calculate the value of the feedback resistors:

$$R2 = \frac{V_{OUT}}{V_S} \times R1 \times \frac{R_S + R_t}{R_t} = 1 \times 249 \times \frac{50 + 58.7}{58.7} = 460.9\ \Omega,$$

$$\text{and } R4 = \frac{V_{OUT}}{V_S} \times (R3 + R_S \parallel Rt) \times \frac{R_S + R_t}{R_t}$$

$$= 1 \times (224 + 50 \parallel 58.7) \times \frac{50 + 58.7}{58.7} = 464.7\ \Omega.$$

It can be seen that the process is iterative because the gain is not 2, but rather

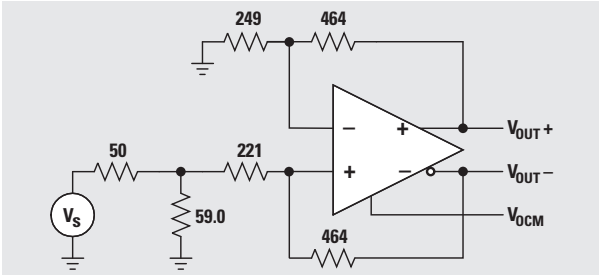
$$\frac{460.9}{249} = 1.85;$$

and R_t is calculated to be 58.7 Ω, not 50 Ω. Iterating through the calculations two more times results in:
R3 = 221.9 Ω (the closest standard 1% value is 221 Ω),
R_t = 59.0 (which is a standard 1% value), and
R2 = R4 = 460.9 (the closest standard 1% value is 464 Ω).
The solution is shown in Figure 8 with standard 1% resistor values.

Use of a spreadsheet makes the iterative process very simple. Also, component values can be easily adjusted to find a better fit to the standard available values.

From the foregoing it is seen that, although the idea of terminating the load may seem trivial, a bit of work is required to get it right.

Figure 8. Single-ended solution for gain = 1



Active anti-alias filtering

A major application for fully differential amplifiers is low-pass anti-alias filters for ADCs with differential inputs.

Creating an active first-order low-pass filter is easily accomplished by adding capacitors in the feedback as shown in Figure 9. With balanced feedback, the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{R_G} \times \frac{1}{1 + j2\pi f(R_F C_F)},$$

where V_{OUT} = (V_{OUT}+) – (V_{OUT}–) and V_{IN} = (V_{IN}+) – (V_{IN}–). The pole created in the transfer function is a real pole on the negative real axis in the s-plane.

To create a two-pole low-pass filter, a passive real pole can be created by placing R_O and C_O in the output, as shown in Figure 10. With balanced feedback, the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F}{R_G} \times \frac{1}{1 + j2\pi f(R_F C_F)} \times \frac{1}{1 + j2\pi f \times 2 \times R_O C_O},$$

where V_{OUT} = (V_{OUT}+) – (V_{OUT}–)
and V_{IN} = (V_{IN}+) – (V_{IN}–).

The second pole created in the transfer function is also a real pole on the negative real axis in the s-plane. The capacitor C_O can be placed differentially across the outputs

as shown in solid lines; or two capacitors (of twice the value) can be placed between each output and ground as shown in dashed lines. Typically, R_O will be a low value; and, at frequencies above the pole frequency, the series combination with C_O will load the amplifier. The extra loading will cause extra distortion in the amplifier's output. To avoid this, you might stagger the poles so that the R_OC_O pole is placed at a higher frequency than the R_FC_F pole.

The classic filter types like Butterworth, Bessel, Chebyshev, etc. (second-order and greater), cannot be realized by real poles—they require complex poles. The multiple feedback (MFB) topology is used to create a complex pole pair and is easily adapted to fully differential amplifiers as shown in Figure 11. A third-order filter is formed by adding R4s and C3 at the output.

Capacitors C2 and C3 can be placed differentially across the inputs and outputs, as shown in solid lines. Alternatively, for better common-mode noise rejection, two capacitors of twice the value can be placed between each input or output and ground, as shown in dashed lines.

The transfer function for this filter circuit is

$$\frac{V_{OUT}}{V_{IN}} = \left[\frac{K}{-\left(\frac{f}{FSF \times f_C}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times f_C} + 1}\right] \times \frac{1}{1 + j2\pi f \times 2 \times R4C3},$$

where $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$ and $V_{IN} = (V_{IN}+) - (V_{IN}-)$,

$$K = \frac{R2}{R1},\ FSF \times f_C = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}},$$

$$\text{and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}.$$

K sets the pass-band gain, f_C is the cut-off frequency of the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2},\ \text{and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re},$$

where Re is the real part of the complex pole pair and Im is the imaginary part. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in

$$FSF \times f_C = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and}$$

$$Q = \frac{\sqrt{2 \times mn}}{1 + m(1 - K)}.$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired f_C.

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Figure 9. First-order active low-pass filter

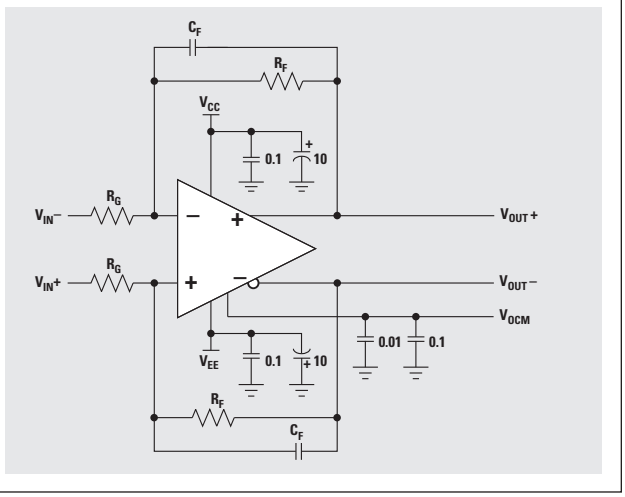


Figure 10. First-order active low-pass filter with passive second pole

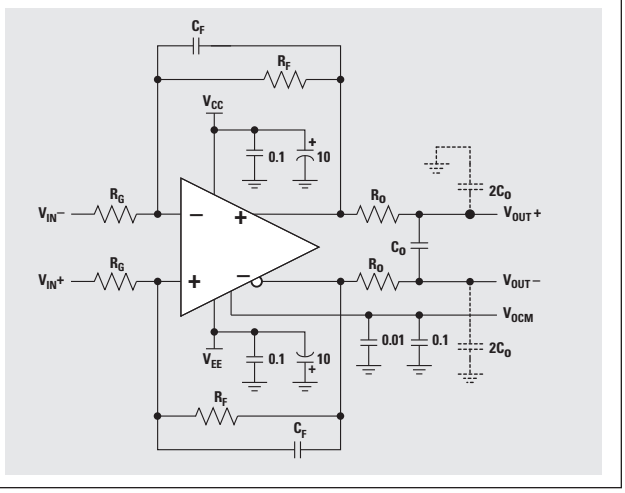
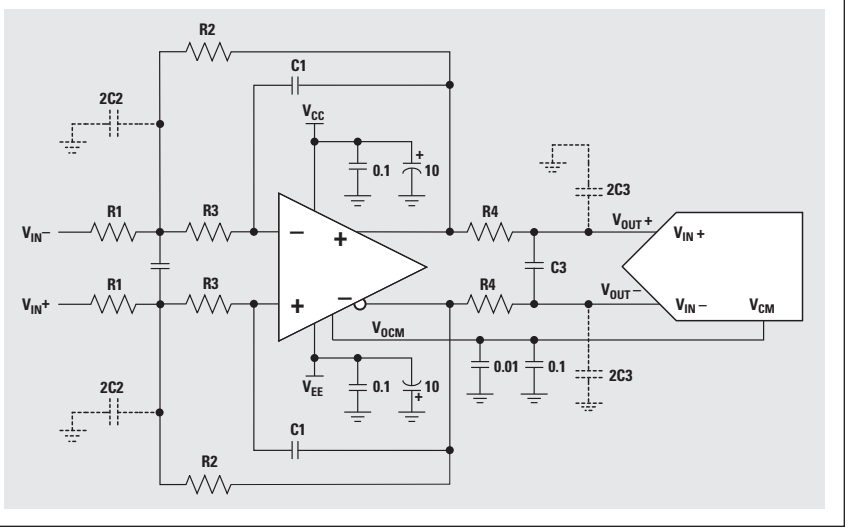


Figure 11. Third-order low-pass filter driving an ADC



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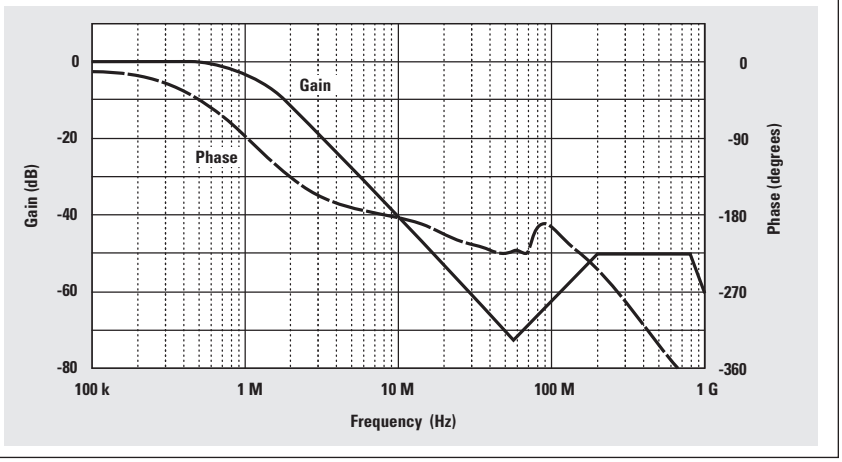
R4 and C3 are chosen to set the real pole in a third-order filter. Care should be exercised with setting this pole. Typically, R4 will be a low value; and, at frequencies above the pole frequency, the series combination with C3 will load the amplifier. The extra loading will cause extra distortion in the amplifier's output. To avoid this, place the real pole at a higher frequency than the cut-off frequency of the complex pole pair.

Figure 12 shows the gain and phase response of a second-order Butterworth low-pass filter, with corner frequency set at 1 MHz and the real pole set by R4 and C3 at 15.9 MHz. The components used are: R1 = 787 Ω, R2 = 787 Ω, R3 = 732 Ω, R4 = 50 Ω, C1 = 100 pF, C2 = 220 pF, C3 = 100 pF, and the THS4141 fully differential amplifier. At higher frequencies, parasitic elements allow the signal to feed through.

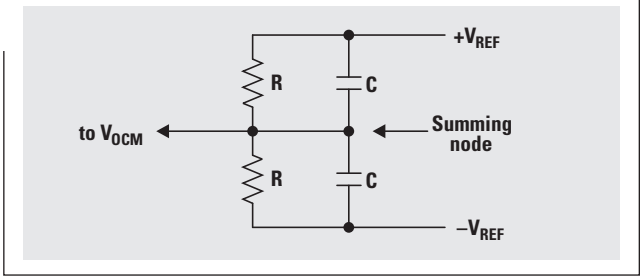
Figure 12. 1-MHz, second-order Butterworth low-pass filter with real pole at 15.9 MHz



V_{OCM}

The proper V_{OCM} is provided as an output by many ADCs with differential inputs. Typically, all that needs to be done is to provide bypass capacitors; 0.1 µF and 0.01 µF are useful choices. If V_{OCM} is not provided, it can be created by forming a summing node with the ADC's plus and minus reference voltages to drive V_{OCM}, as shown in Figure 13. The voltage at the summing node is the midpoint value between $+V_{REF}$ and $-V_{REF}$. Depending on the loading of the V_{OCM} input, the summing node voltage may need to be buffered.

Figure 13. Driving V_{OCM} from ADC's reference voltage



Power-supply bypass

Each power rail should have 6.8-µF to 10-µF tantalum capacitors located within a few inches of the amplifier to provide low-frequency power-supply bypassing. A 0.01-µF to 0.1-µF ceramic capacitor should be placed within 0.1 inch of each power pin on the amplifier to provide high-frequency power-supply bypassing.

Layout considerations

As with all high-speed amplifiers, you should minimize parasitic capacitance at the amplifier's input by removing the ground plane near the pins and near any circuit traces. Also, make trace routing as direct as possible and use surface-mount components.

Using positive feedback to provide active termination

Driving transmission lines differentially is a typical use for fully differential amplifiers. Using positive feedback with amplifiers can provide active termination, as shown in Figure 14. Because of the positive feedback, the output line impedance appears larger than the value of output resistor R_O. Still, the voltage dropped across the resistor depends on its actual value, resulting in increased efficiency.

It is important to use symmetrical feedback with this application.

With double termination, the output impedance of the amplifier, Z_O, will equal the characteristic impedance of the transmission line; and the far end of the line will be terminated with the same value resistor, i.e., $R_t = Z_O$. For proper balance, half of Z_O is placed in each half of the differential output, so that $Z_O = 2 \times Z_{O\pm}$.

To calculate the output impedance, ground the inputs and insert either a voltage or current source between $V_{OUT}+$ and $V_{OUT}-$.

Due to symmetry, $Z_O+ = Z_O-$, $V_{OUT}+ = -(V_{OUT}-)$, and $V_O+ = -(V_O-)$. Calculating the impedance of one side provides the solution.

$$Z_O+ = \left(\frac{V_{OUT}+}{I_{OUT}+}\right) \| R_P,\ I_{OUT}+ = \frac{(V_{OUT}+) - (V_O+)}{R_O},$$

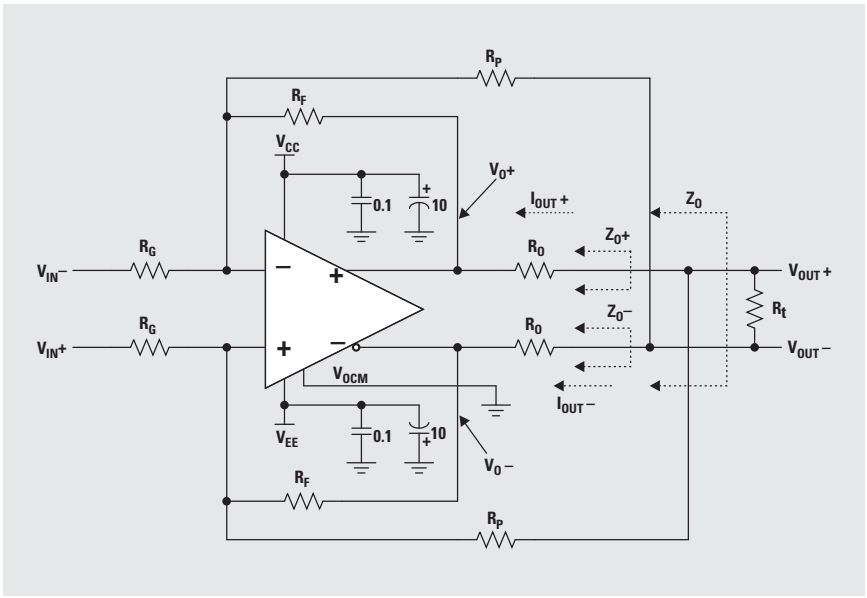
$$\text{and } V_O+ = (V_{OUT}-) \times \left(\frac{-R_F}{R_P}\right).$$

The amplifier's output impedance on each side of the line will be R_O divided by 1 minus the gain from the opposite line:

$$Z_{O\pm} = \left(\frac{R_O}{1 - \frac{R_F}{R_P}}\right) \| R_P. \qquad (1)$$

The positive feedback also affects the forward gain. Accounting for this effect and the voltage divider between

Figure 14. Using positive feedback to provide active termination



R_O and $R_t \parallel 2R_P$, the gain from $V_{IN} = (V_{IN}+) - (V_{IN}-)$ to $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$ is

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_F}{R_G} \times \frac{1}{\frac{2R_O + R_t \parallel 2R_P}{R_t \parallel 2R_P} - \frac{R_F}{R_P}}. \qquad (2)$$

Design is easily accomplished if you first choose the value of R_F and R_O. Then calculate the required value of R_P to give the desired Z_O. Then calculate R_G for the required gain.

For example: It is given that you want a gain of 1, and you want to terminate a 100-Ω line properly with R_F = 1 kΩ and R_O = 10 Ω. The proper value for Z_O and R_t is 100 Ω ($Z_O\pm$ = 50 Ω). Rearranging Equation 1 yields

$$R_P = \frac{R_F - R_O}{1 - \frac{R_O}{Z_O \pm}} = \frac{990\ \Omega}{1 - \frac{10\ \Omega}{50\ \Omega}} = 1.24\ \text{k}\Omega.$$

Then, rearranging Equation 2 gives us

$$R_G = \frac{R_F}{A} \times \frac{1}{\frac{2R_O + R_t \parallel 2R_P}{R_t \parallel 2R_P} - \frac{R_F}{R_P}}$$

$$= \frac{1\ \text{k}\Omega}{\frac{20\ \Omega + 100\ \Omega \parallel 2.48\ \text{k}\Omega}{100\ \Omega \parallel 2.48\ \text{k}\Omega} - \frac{1\ \text{k}\Omega}{1.25\ \text{k}\Omega}} = 2.49\ \text{k}\Omega.$$

The circuit is built and tested with the nearest standard values to those previously computed:
R_F = 1 kΩ, R_P = 1.24 kΩ, R_G = 2.49 kΩ, R_t = 100 Ω, and R_O = 10 Ω. Compare the output voltage waveforms ($V_{OUT} = 2V_{PP}$) with active termination and standard termination shown in Figure 15
[$V_O = (V_O+) - (V_O-)$, and $V_{OUT} = (V_{OUT}+) - (V_{OUT}-)$].

For standard termination,
R_F = 1 kΩ, R_P = open, R_G = 499 Ω, R_t = 100 Ω, and R_O = 50 Ω.

With standard termination, 20 mW of power is dissipated in the output resistors, as opposed to 6.25 mW with active termination, which wastes 69% less power.

Another feature about active termination that is very attractive, especially in low-voltage applications, is the effective increase in output-voltage swing for a given supply voltage.

Conclusion

In high-speed systems, proper line termination requires considering the termination resistors and adjusting the gain-setting resistors to maintain symmetrical feedback.

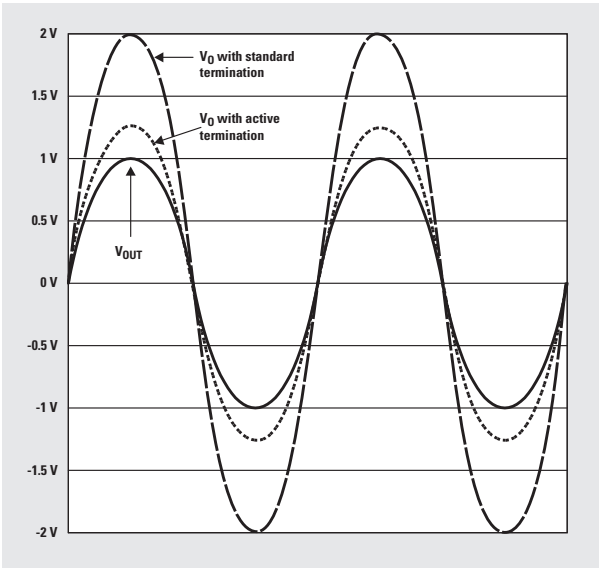
Integrated, fully differential amplifiers are well suited for driving differential ADC inputs. They provide an easy means for anti-alias filtering and for setting the common-mode voltage.

Integrated, fully differential amplifiers are also well suited for driving differential transmission lines, and active termination provides for increased efficiency.

Related Web sites

www-s.ti.com/sc/techlit/slyt018
www.ti.com/sc/amplifiers

Figure 15. Output waveforms with active and standard termination



Pressure transducer-to-ADC application

By John Bishop
Application Specialist, Advanced Analog Products/Op Amp Applications

Introduction

A major application of operational amplifiers (op amps) is converting and conditioning signals from transducers into signals that other devices such as analog-to-digital converters (ADCs) can use. Conversion and conditioning are usually necessary because the transducer and ADC ranges and offsets are rarely the same. Op amp circuits are also useful in signal filtering for compatibility with ADC circuits.

This article shows how to use a bridge-type transducer for measuring gas or liquid pressure, and for measuring strain in mechanical elements. A basic understanding of active and passive analog devices and their use is helpful to use this article to complete a design.

Transducer information

The sensor tested in this application is a pressure transducer SX01 produced by SenSym Inc. It is one of a set of solid-state pressure sensors with available full-scale ranges of 1 to 150 psi (7 kPa to 1 MPa). Three types of pressure measurement are available: gauge, differential, and absolute. See SenSym's data sheet at www.sensym.com/to5.htm.

TRW, another supplier of such sensors, has an on-line product catalog with a link to data sheets at www.novasensor.com/catalog/catalog.html

The device evaluated here has a full-scale pressure of 1 psig (7 kPa). Its price is low relative to other devices in this range; however, the low price comes at the expense of no temperature compensation, a drawback that can be overcome by adding inexpensive, external compensation components. The SenSym data sheet defines three circuits for this purpose; the method chosen here uses an NPN bipolar transistor and two resistors.

Excitation source information

For a bridge transducer to work, it must be excited by a voltage source. Because the stability of the excitation voltage affects the accuracy of the measurement signal, a regulated voltage source is necessary. This application assumes the availability of a regulated 5-V supply.

Choice of ADC

For this design, the TLV2544 ADC was selected because it has an analog input range of 0 to 5 V (see Reference 1). Ideally, the span of the amplified sensor signal should fill this range. The voltage needed to power this device is a single 5-V supply.

Choice of op amp

The ADC's 0- to 5-V analog-input range and the use of a single 5-V power supply required a rail-to-rail output device. The op amp also needed to be able to handle the full input range of the transducer. For these reasons, the TLV2474 was chosen (see Reference 2).

Defining the circuit

The amplified pressure transducer signal is connected to an ADC. Since the ADC connects to a microprocessor or DSP, final calibrations can be done in software. Therefore, the 0- to 1-psi range should span the center of the ADC's range. For calculating gain, the output range of the amplifier is 1.25 to 3.75 V. Figure 1 is the schematic of the amplifier circuit for this application.

The output of the circuit is

$$V_{OUT} = V_{IN2}\left(\frac{2R_4 + R_3}{R_3}\right)\left(\frac{R_7}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right) - V_{IN1}\left(\frac{2R_1 + R_3}{R_3}\right)\left(\frac{R_6}{R_2}\right) + V_{REF}\left(\frac{R_5}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right). \quad (1)$$

When $R_7 = R_6$, $R_5 = R_2$, and $R_4 = R_1$, Equation 1 reduces to

$$V_{OUT} = (V_{IN2} - V_{IN1})\left(\frac{2R_1}{R_3} + 1\right)\left(\frac{R_6}{R_2}\right) + V_{REF}. \quad (2)$$

Solving for R_3 yields

$$R_3 = \frac{2R_1}{\frac{(V_{OUT} - V_{REF})R_2}{(V_{IN2} - V_{IN1})R_6} - 1}. \quad (3)$$

The sensitivity of the bridge is typically 4.0 mV/V/psi. The pressure is 1 psi and the excitation voltage is 5 V. Therefore, the differential output of the sensor (V_{IN2}–V_{IN1}) from 0 to 1 psi is 20 mV. Setting $R_1 = R_4 = R_6 = R_7 =$ 20.0 kΩ (1% value) and $R_2 = R_5 = 2.0$ kΩ results in a full-scale output range of 2.5 V when $R_3 = 3.478$ kΩ.

A unique feature of this precision instrumentation amplifier is the ability to control the total gain of the amplifier with one resistor.

Calibration devices

The resistor that controls gain is R_1. A potentiometer has a larger temperature coefficient and is more likely to drift over time than a fixed resistor. Placing a fixed resistor in series with a potentiometer minimizes this problem. The values calculated in the following equations are based on about 10% gain adjustment.

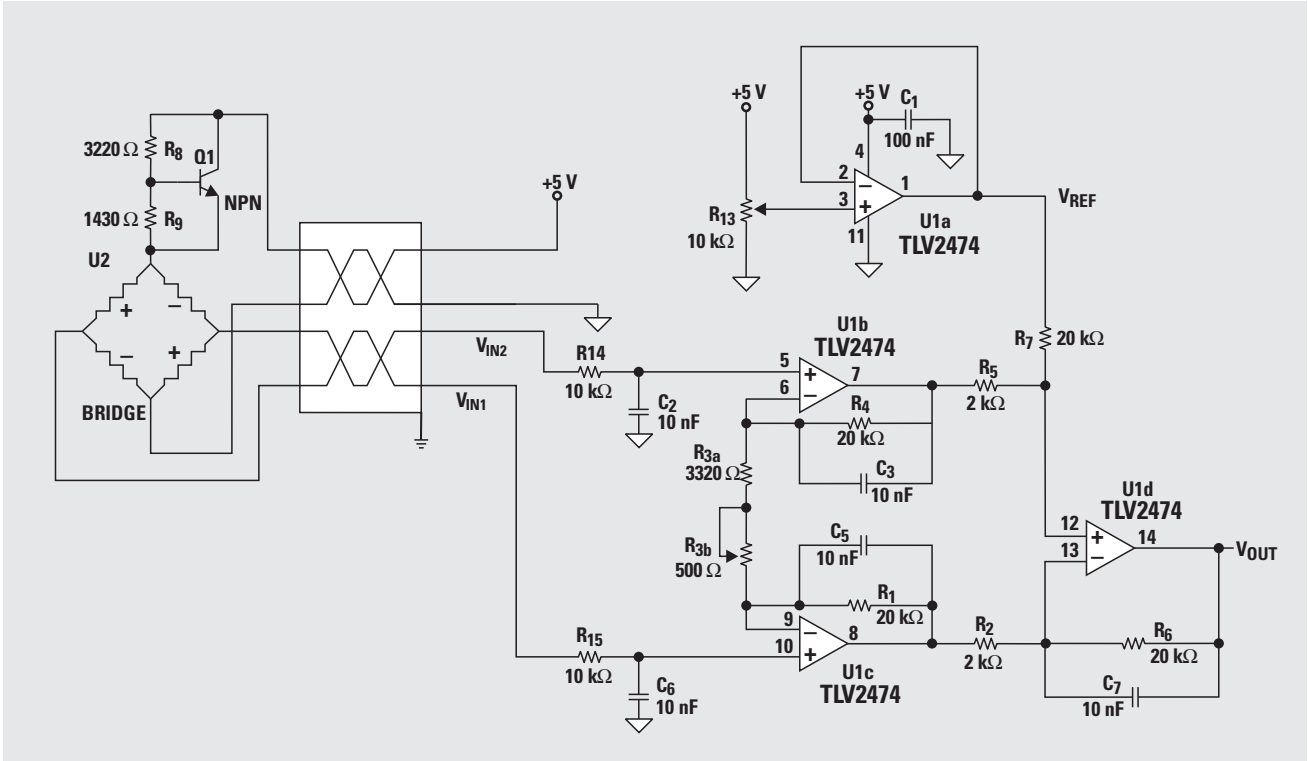
$R_{3A} = R_1 - R_1(5\%) = 143$ kΩ (1% resistor) **(4)**

$R_{3B} = R_3(10\%) = 50$ kΩ (Cermet potentiometer) **(5)**

The potentiometer for adjusting offset, R_{13}, is not critical; but a 10-kΩ multiturn potentiometer uses 0.5 mA.

One of the goals of design is to reduce components without compromising function. If the offset voltage of the op amps is low enough, replacing potentiometers with fixed resistors is possible. Offset and gain calibration

Figure 8. Op amp circuit for the pressure transducer-to-ADC application



would then be done using software in a DSP or microprocessor. This is possible because the bottom and top 25% of the input range of the ADC are not presently used. In this condition, V_{REF} would be initially set by replacing R_{13} with a voltage divider. The offset drift of the op amps causes the output to move up or down into the unused areas. Variations on the resistors cause small gain errors, but these should be of less concern than the offset voltage. Instead of calibrating with potentiometers, using the offset and gain variables in calculations can generate a calibrated output.

Signal filtering

If the transducer is installed on the amplifier board, the input filter circuits and shielded wires are not needed.

Connecting a transducer to an input subjects the wiring to noise signals because of the surrounding electrical and magnetic environment. To prevent this noise from interfering with the measurement signals, some shielding is necessary. Using a twisted pair from the transducer to the conversion circuit and shielding this pair (grounding the shield at the instrument) reduces the noise.

Even when the transducer is connected through correctly shielded cabling, some noise is brought into the amplifier along with the measurement signal. Without an input filter, the op amp would act as an RF detector, converting high-frequency signals from other devices into signals with low-frequency components. Placing a resistor and capacitor on the input forms a low-pass filter and prevents radio-frequency signals from interfering with the measurement signal. The frequency response of this filter is

$$f_C = \frac{1}{2\pi RC}. \quad \textbf{(6)}$$

Thus, if R_{14} and R_{15} are 10 kΩ, and C_2 and C_6 are 10 nF, then f_C is about 1600 Hz.

The next two stages have capacitors in parallel with the feedback resistors. The frequency response of these filters is also defined by Equation 6. Using 20 kΩ for the feedback resistor gives a cutoff frequency, f_C, of about 800 Hz.

References

For TI information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the following document.

Document Title	TI Lit. #
1. "TLV2544, TLV2548 2.7-V to 5.5-V, 12-bit, 200-kSPS, 4-/8-channel, Low-power Serial Analog-to-Digital Converters with Autopower-down," Data Sheet	slas198
2. "TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA Family of 600-µA/Ch 2.8-MHz Rail-to-Rail Input/Output High-Drive Operational Amplifiers with Shutdown," Data Sheet	slos232

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Document Title **TI Lit. #**

3. "Understanding Basic Analog-Ideal Op Amps," Application Report slaa068
4. "Single Supply Op Amp Design Techniques," Application Report sloa030
5. "Active Low-Pass Filter Design," Application Report sloa049
6. "Application of Rail-to-Rail Operational Amplifiers," Application Report sloa039
7. Ron Mancini, "Sensor to ADC—Analog Interface Design," *Analog Applications Journal* (May 2000), p. 22 . . . . . .slyt015
8. "Signal Conditioning Wheatstone Resistive Bridge Sensors," Application Report sloa034

Related Web sites

www.sensym.com/to5.htm

www.novasensor.com/catalog/catalog.html

Appendix A. Calculations

The following values and equations were used in this article. Values in **bold** are calculated. All entered values are non-bold.

Given:

$Input_{MIN}$ = 0.0 psi ⇒ $Output_{MIN}$ = 1.25 V

$Input_{MAX}$ = 1.0 psi ⇒ $Output_{MAX}$ = 3.75 V

Sensitivity = 0.004 mV/V/psi

Excitation voltage = 5 V

Full-scale span = 0.02 V

Nominal Gain = 125

R_8 = 3.22 kΩ

R_9 = 1.43 kΩ

$R_1 = R_4 = R_7 = R_6$ = 20 kΩ

$R_5 = R_2$ = 2 kΩ

V_{IN} = 0.02 V

V_{OUT} = 2.5 V

R_3 = 3478 Ω

1% value

R_{3A} = 3304 Ω ⇒ 3320 Ω

Pot. value

R_{3B} = 348 Ω ⇒ 500 Ω

$C_4 = C_6$ = 0.01 µF

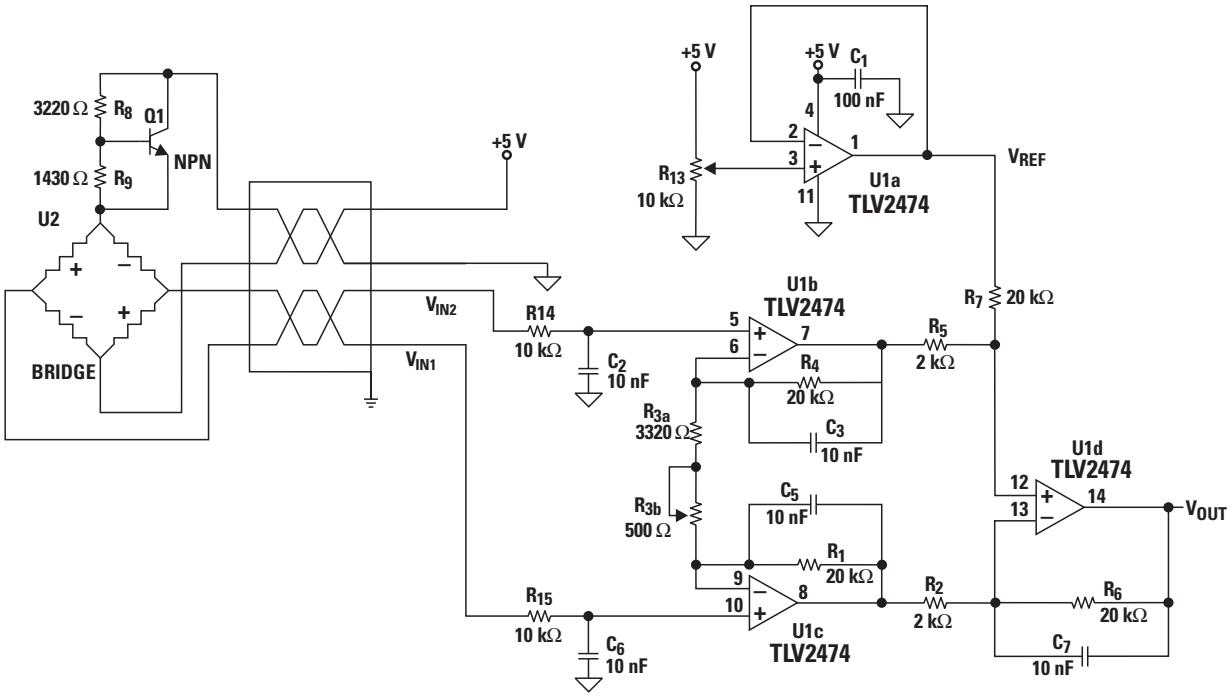
$R_{14} = R_{15}$ = 10 kΩ

F_C = 1592 Hz

$C_3 = C_5 = C_7$ = 0.01 µF

$R_1 = R_4 = R_6$ = 10 kΩ

F_C = 796 Hz



An audio circuit collection, Part 2

By Bruce Carter
Advanced Linear Products, Op Amp Applications

Introduction

This is the second in a series of articles on single-supply audio circuits. The reader is encouraged to review Part 1*, in the November 2000 issue of *Analog Applications Journal*, which concentrated on low-pass and high-pass filters. Part 2 concentrates on audio-notch-filter applications and curve-fitting filters.

Audio notch filters

There are audio applications where a single frequency is undesirable and needs to be rejected. The frequency to be rejected is not part of the original audio and is annoying to the listener. Frequencies on either side of the rejected frequency, however, contain useful audio content. If they are rejected as well, there will be an equally annoying "hole" in the audio. Notch filters are used to reject very narrow frequency bands with minimal attenuation on either side of the notch. Notch filters, compared to low-pass and high-pass filters, are hard to implement. Components that would cause only a slight ripple or "washout" in a low-pass or high-pass filter often have a dramatic effect on the depth of the notch. A slight mistuning of a low-pass or high-pass filter is inaudible, but mistuning a notch filter may cause it to miss the interfering frequency altogether. Following are some hints about how to implement a notch with a reasonable degree of confidence.

*The original Part 1 release of this series had op amp polarity symbols reversed in several figures. Please download the corrected version at: www.ti.com/sc/docs/apps/msp/journal/nov2000/nov_08.pdf

60-Hz hum filter

One of the most common problems with audio is the presence of a 60-Hz hum. Since 60 Hz is the frequency used for ac-power distribution, it is one of the most prevalent interference sources.

Usually, a 60-Hz hum is the result of poor grounding practices. It is better to attack the problem at the source than to filter the audio. Nevertheless, there may be situations where the grounding of a particular system may not be accessible. In that case, an add-on filter may be appropriate.

The 60-Hz hum filter shown in Figure 1 is based on twin-T configuration. This topology is very effective but can be temperamental. The circuit response is very dependent on the actual values of R1, R2, R3, C1, C2, and C3. All of these tuning components should be 1%, but that may not be enough. They should all be taken from the same lot, because parts manufactured at the same time tend to have the same characteristics.

If components are matched properly, performance can be very good. Mismatched components will seriously degrade the response. In the twin-T configuration, R3 is half the value of R1 and R2. The best way of making the resistance value for R3 is to use two of the resistors used for R1 and R2 in parallel. Similarly, taking two capacitors of the same value as C1 and C2 in parallel forms C3. This increases the component count of the circuit by two (one additional resistor and capacitor) but greatly increases the

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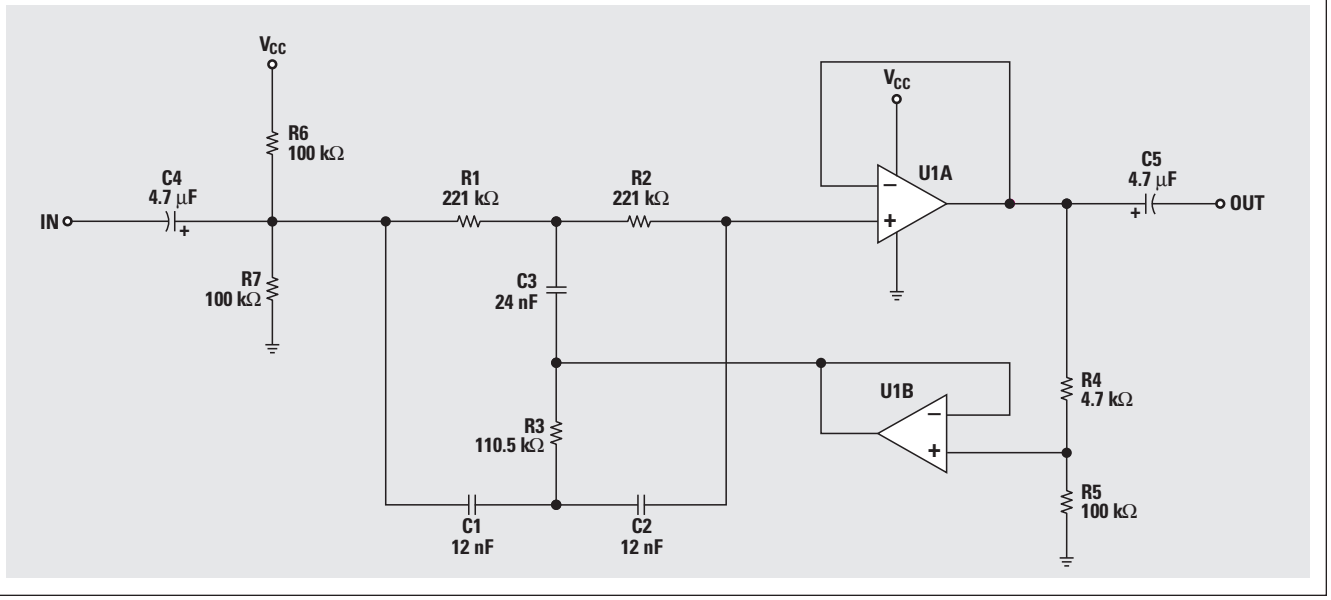
Figure 1. Configuration of a 60-Hz notch filter



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matching, because the designer can take easy steps to insure that the parts are from the same batch (off the same reel, out of the same box, etc.).

Note in Figure 1 that no half-supply reference is required. R6 and R7 generate half supply after the input capacitor. The theoretical response of this filter is shown in Figure 2. The ideal values produce a notch as shown. If, however, the RC combination is 1% off, the notch will be shifted left or right by 0.6 Hz, and rejection of the 60-Hz frequency could be less than 20 dB.

A way around that problem is to put a small potentiometer in series with R3, which should be reduced one or two standard E-96 values. Figure 3 shows circuit response with R3 varied from 107 kΩ to 113 kΩ.

Varying R3 over even this small range produces a tremendous variation in the depth of the notch as well as the Q of the circuit. In every case, though, more than 20 dB is achievable, and most of the time as much as 30 or 40 dB. If a deeper null is needed, R1 and R2 need to be adjustable as well. They can be adjusted in a dual potentiometer to reduce the number of potentiometers in the circuit to 2. If the capacitors are matched (which is possible if they are from a single batch), 60-dB rejection is possible.

The circuit can be modified to reject hum from the 50-Hz line frequency of ac power in Europe and other parts of the world, as follows:

- Change R1 and R2 to 42.4 kΩ.
- Change R3 to 21.2 kΩ (two 42.4-kΩ resistors in parallel).
- Change C1 and C2 to 75 nF.
- Change C3 to 150 nF (two 75-nF capacitors in parallel).

The previous comments regarding the 60-Hz notch filter apply to the 50-Hz version as well. Theoretical response of the 50-Hz notch filter is shown in Figure 4. Standard E-24 capacitor values and standard E-96 resistor values do not produce a combination that is as close to perfect as in the 60-Hz case, so trimming may be even more necessary for a 50-Hz notch filter.

Figure 2. Response of 60-Hz notch filter

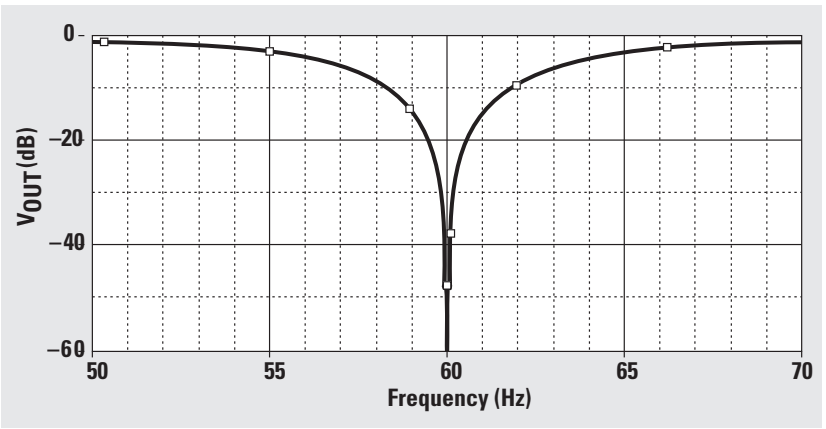


Figure 3. Varying notch depth

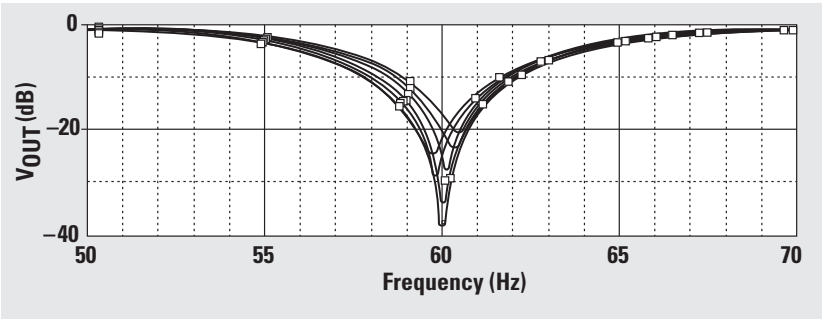
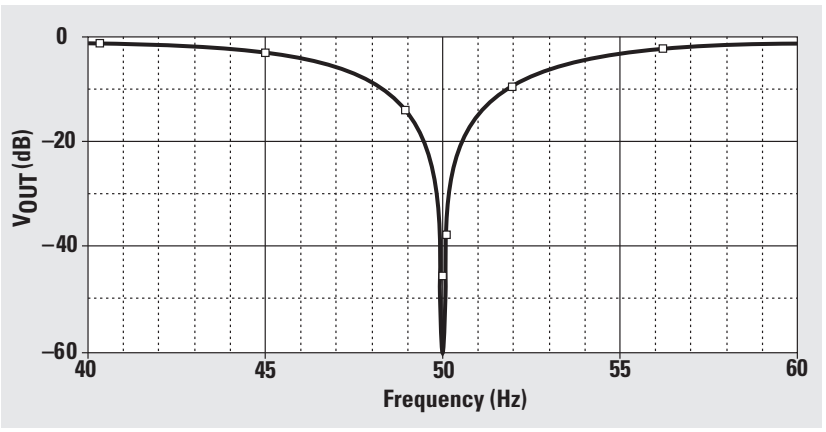


Figure 4. Response of a 50-Hz notch filter

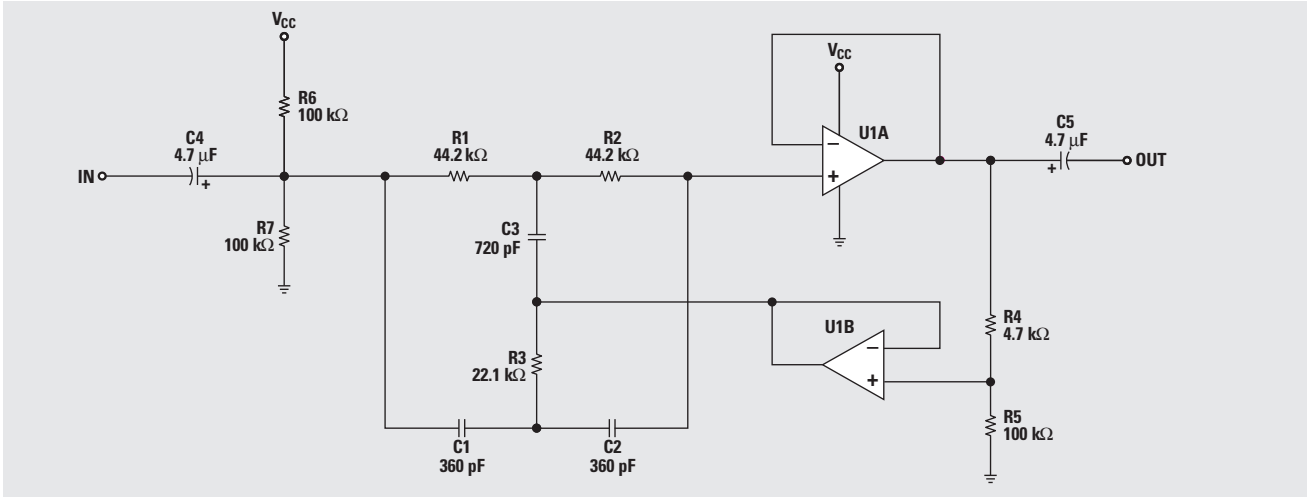


Medium-wave whistle filter

In North America, medium-wave (AM) stations are separated by 10-kHz channels from 540 to 1700 kHz. AM frequency response is unlimited compared to FM, which is severely rolled off above 15 kHz. Unfortunately, there will be interference from the adjacent channels, especially at night.

The audio modulation from adjacent channels is usually not a problem on strong local stations, but the carrier is. It shows up in the audio as a 10-kHz tone. This tone can be quite loud—especially at night, even on local stations. For those who can hear it, the pitch is extremely annoying. Making the problem even worse, there are channels above and below those used by most stations, and they are not exactly at 10 kHz. The FCC allows a tolerance of ±20 Hz from the assigned frequency, and that will make the two

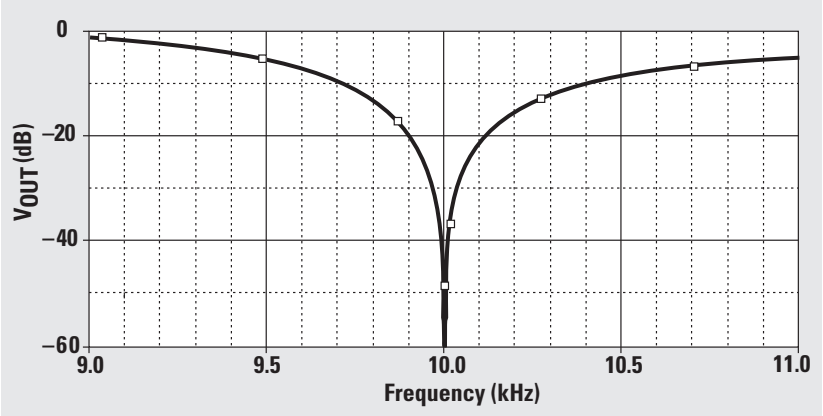
Figure 5. 10-kHz notch filter



adjacent channels modulate each other and create beat-frequencies, adding to the annoying aspect of the tone.

To eliminate the 10-kHz tone, a notch filter is needed that eliminates a narrow band around 10 kHz, while leaving other frequencies untouched. Many years ago, high-priced AM receivers used a high-Q LC filter, but tuning was so critical that it was of limited use. The op amp approach shown in Figure 5 is extremely stable and never requires additional adjustments once the initial center frequency is set. The twin-T notch filter topology is used again, due to its ability to provide large attenuations with only two op amps. All of the comments about the 60-Hz notch filter apply to the 10-kHz notch filter. Even with simple tuning, however, the improvement should be dramatic. The response of this filter is shown in Figure 6.

Figure 6. Response of 10-kHz notch filter



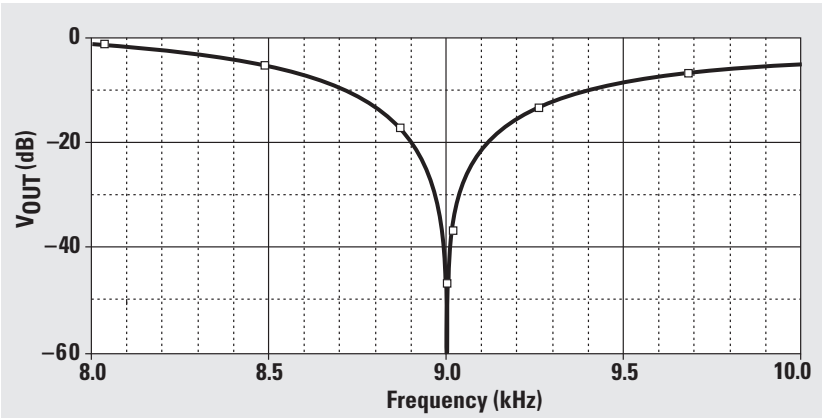
In Europe and much of the rest of the world, the medium-wave transmission uses channels from 531 to 1611 kHz, separated by 9 kHz. This will cause a 9-kHz (instead of 10-kHz) tone in the received audio.

To reject the 9-kHz tone resulting from 9-kHz channel spacing:

- Change R1 and R2 to 45.3 kΩ
- Change R3 to two 45.3-kΩ resistors in parallel (22.65 kΩ).
- Change C1 and C2 to 390 pF.
- Change C3 to two 390-pF capacitors in parallel (780 pF).

The response of a well-tuned 9-kHz notch filter is shown in Figure 7.

Figure 7. Response of 9-kHz notch filter



Much of the world relies on short-wave radio stations for news and entertainment. Short-wave radio is transmitted on

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several bands, with stations separated by only 5 kHz. To reject the 5-kHz tone resulting from 5-kHz channel spacing:

- Change R1 and R2 to 42.4 kΩ
- Change R3 to two 42.4-kΩ resistors in parallel (21.2 kΩ).
- Change C1 and C2 to 750 pF.
- Change C3 to two 750-pF capacitors in parallel (1500 pF).

The response of a well-tuned 5-kHz notch filter is shown in Figure 8.

This notch filter topology can be retuned to reject almost any audio frequency that poses a problem. Areas of the world served by both 10-kHz-spaced and 9-kHz-spaced medium-wave stations may experience objectionable tones at any frequency from 1 kHz to 10 kHz and above.

Curve-fitting filters

Analog designers are often asked to design low-pass and high-pass filter stages for maximum rejection of frequencies that are out of band. This is not always the case, however. Sometimes the designer is asked to design a circuit that will conform to a specified frequency response curve. This can be a challenging task, particularly if all the designer knows is that a single-pole filter rolls off 20 dB per decade; and a double-pole filter, 40 dB per decade. How does the designer implement a different roll-off?

It is not possible to get more out of a filter than it is designed to produce. A single pole will give no more than 20 dB per decade—and cannot be increased or decreased. More roll-off demands a double-pole filter with 40 dB per decade. Obtaining different roll-off characteristics is done by allowing filters at closely spaced frequencies to overlap.

One popular curve-fitting application is the RIAA equalization (see Figure 9), which compensates for equalization applied to vinyl record albums during manufacture. Designers of many newer pieces of audio gear have omitted the RIAA equalization circuit completely, assuming that the majority of users will not desire the function. In spite of the enormous popularity of audio CDs, there are still dedicated audiophiles who have a large library of record albums—titles that are not available on CDs or are out of print.

RIAA has the following response:

- 17 dB from 20 to 50 Hz,
- 0 dB from 500 to 2120 Hz, and
- –13.7 dB at 10 kHz.

Figure 8. Response of 5-kHz notch filter

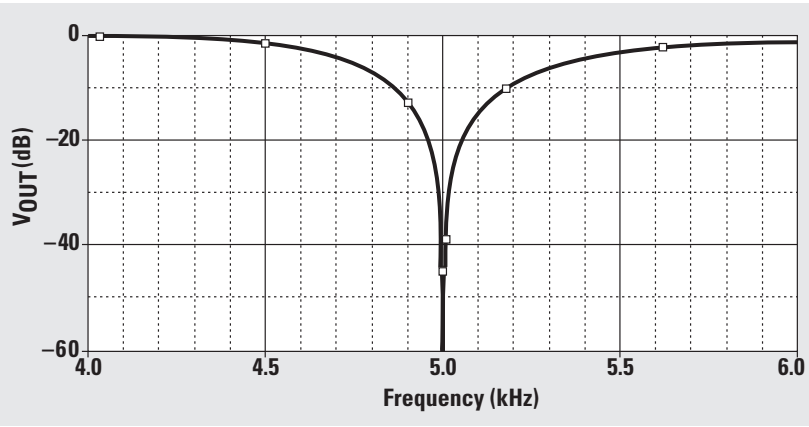


Figure 9. The RIAA equalization curve

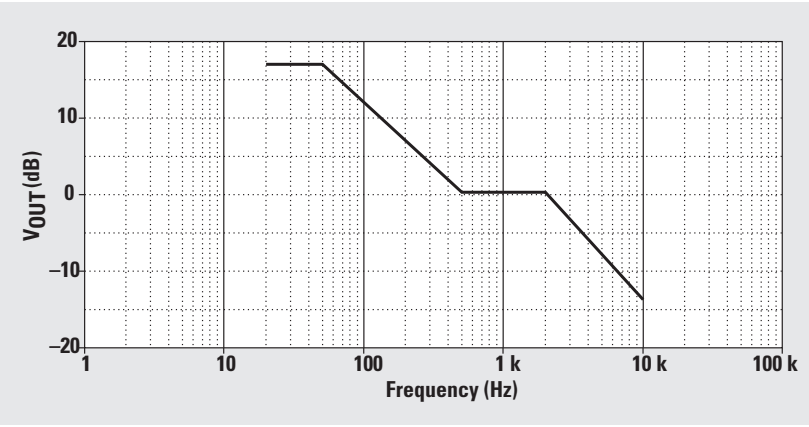


Figure 10. RIAA equalization circuit

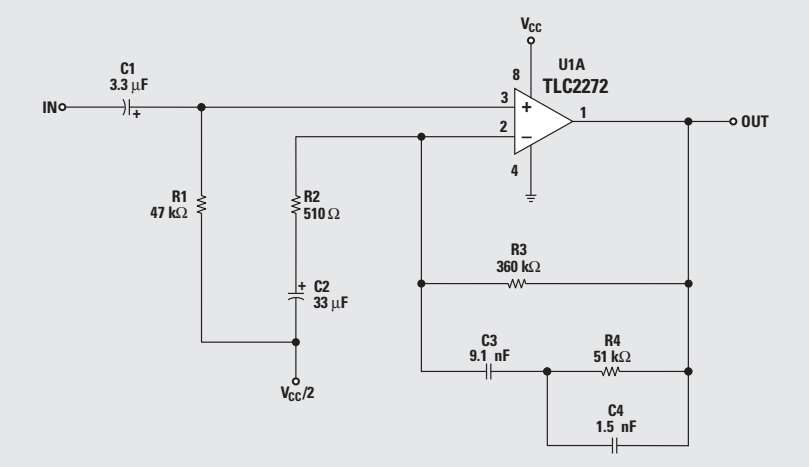
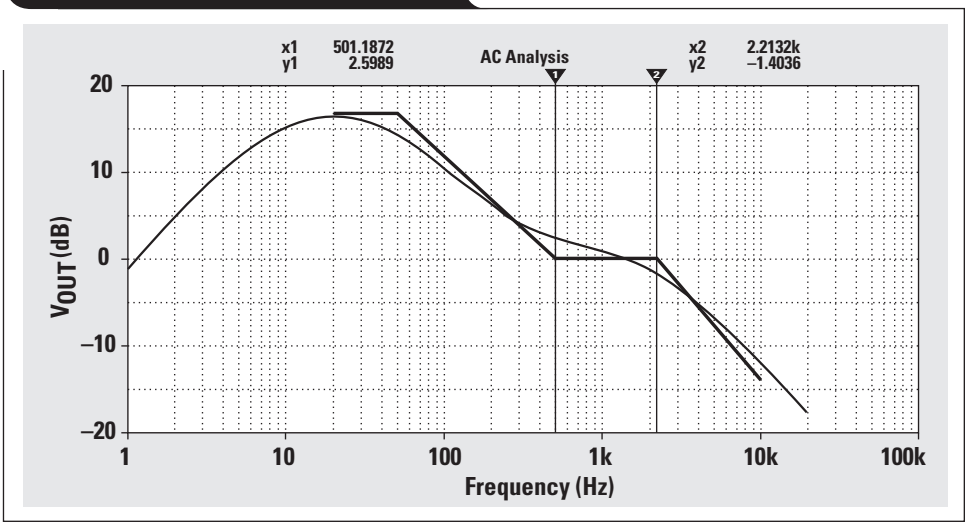


Figure 11. RIAA equalizer resonse



RIAA equalization curves often include another breakpoint at 10 Hz to limit low-frequency "rumble" effects that could resonate with the turntable's tone arm. The standard input impedance in the circuits shown in Figure 10 is 47 kΩ. This impedance makes a convenient place to inject dc offset into single-supply circuits, so it is isolated from the phonograph cartridge by an input capacitance. The phonograph cartridge output is assumed to be 12 mV.

Application circuits were evaluated from many sources in print and on the Web. Many of these did not work at all, did not easily translate to single-supply operation, or deviated markedly from the RIAA specification.

The circuit topology presented in Figure 10 was one of the most common, appearing in several sources. This circuit was tweaked manually to produce the closest possible conformance to the RIAA curve. A small additional gain resistor was sometimes added between the junction of R3 and C3 and the inverting input. It did not seem to be necessary, and this implementation contains the smallest number of passive components. There is even a Web page that contains a Java-based calculator dedicated to this topology (see www.vwlowen.demon.co.uk/java/riaa.htm).

The implementation of the circuit in Figure 10 yields the curve shown in Figure 11. Several things are troublesome with this topology:

- No matter how much the circuit is optimized, the section from 500 Hz to 2120 Hz is not simulated well. The first-order breakpoints that are possible with the single op amp create only a slight ripple on the characteristic curve in Figure 11. These breakpoints require a second-order filter. This is very near the region where human hearing is the most sensitive and errors will be the most audible. The musical content immediately below 1 kHz will be too loud, and that immediately above 1 kHz will be too soft. Aesthetically, this will make the sound "muddy," lacking brilliance and tonal clarity.
- C2 is a large capacitance value that happens to be in the highest-gain network in the circuit. Power-on transients will cause large, unexpected voltage swings—possibly overloading the input to the next stage. They could also create loud, possibly destructive transients in loudspeakers. Further, the difficulty of getting precision values of electrolytic capacitors will lead to wide variations in response—both of the amplitude and the low-frequency roll-off breakpoint.
- Fine-tuning this circuit is difficult; virtually all components interact.

The procedure for tuning is:

1. Set the low-frequency gain (LFG) with R2 and R3:

$$\mathrm{LFG} = \frac{\mathrm{R3}}{100 \times \mathrm{R2}} = 16.97\ \mathrm{dB}$$

2. Set the mid-frequency gain (MFG) with R4:

$$\mathrm{MFG} = \frac{\mathrm{R4}}{100 \times \mathrm{R2}} = 0\ \mathrm{dB}$$

3. Set the low-frequency roll-off (LFR) with C2:

$$\mathrm{LFR} = \frac{1}{2\pi \times \mathrm{R2} \times \mathrm{C2}} = 9.46\ \mathrm{Hz}$$

4. Set the low-frequency breakpoint (LFB) with C3:

$$\mathrm{LFB} = \frac{1}{2\pi \times \mathrm{R3} \times \mathrm{C3}} = 48.6\ \mathrm{Hz}$$

5. The mid-frequency breakpoint (MFB) is already determined by the values of R4 and C3:

$$\mathrm{MFB} = \frac{1}{2\pi \times \mathrm{R4} \times \mathrm{C3}} = 342\ \mathrm{Hz}$$

6. Set the high-frequency breakpoint (HFB) with C4:

$$\mathrm{HFB} = \frac{1}{2\pi \times \mathrm{R4} \times \mathrm{C4}} = 2080\ \mathrm{Hz}$$

These steps must be followed in order. The initial selection of R2 determines the other components. It is unfortunate that there is no control over the mid-frequency breakpoint, which probably accounts for the error in the response of the curve (Figure 11). The mid-frequency breakpoint is constrained to 342 Hz when it should be 500 Hz.

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Fine-tuning can be improved by splitting the implementation into two op amps (see Figure 12):

- Set the low-frequency roll-off with R1 and C1:

$$\text{LFR} = \frac{1}{2\pi \times \text{R1} \times \text{C1}} = 10.3 \text{ Hz}$$

- Set the low-frequency gain with R3 and R2:

$$\text{LFG} = \frac{\text{R3}}{\text{R2}} = 16.9 \text{ dB}$$

- Set the low-frequency breakpoint with C2:

$$\text{LFB} = \frac{1}{2\pi \times \text{R3} \times \text{C2}} = 48.2 \text{ Hz}$$

- Set the high-frequency breakpoint with R4 and C3:

$$\text{HFB} = \frac{1}{2\pi \times \text{R4} \times \text{C3}} = 723 \text{ Hz}$$

The response of this circuit is shown in Figure 13.

The circuit will be the starting point for simulation of the RIAA curve. The response from 500 to 2120 Hz should be flat at 0 dB. This first-order circuit is 1.8 dB too high at 500 Hz, and 2.4 dB too low at 2120 Hz. Selecting the HFB at 723 is a trick that shifts the response at 1 kHz down to 0 dB. This is a fairly drastic change, though. The first step in improving the RIAA characteristic is to change the 2120-Hz portion to second-order. A unity-gain Sallen-Key stage is selected, as shown in Figure 14.

R4, R5, C3, and C4 control the 2120-Hz breakpoint. The response of the circuit changes to that shown in Figure 15. The 2120-Hz response has improved from 2.4-dB to 0.8-dB deviation from the curve. Unfortunately, there is less interaction with the 50-Hz low-pass filter; and the 500-Hz response is now 2 dB, instead of 1.8 dB, above ideal. Clearly, another second-order filter is required. Accomplishing this requires a change in first-order-stage topology and an increase in complexity to four op amps, as shown in Figure 16.

Figure 12. Dual op amp implementation of equalizer

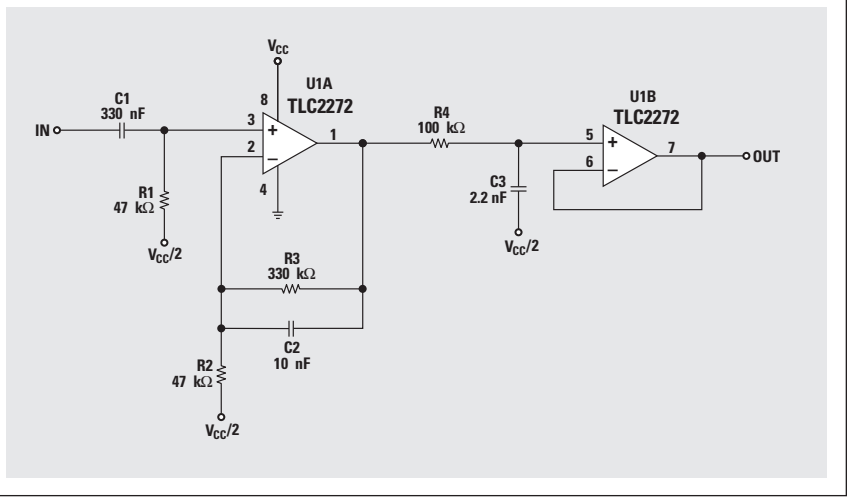


Figure 13. Response of split op amp circuit

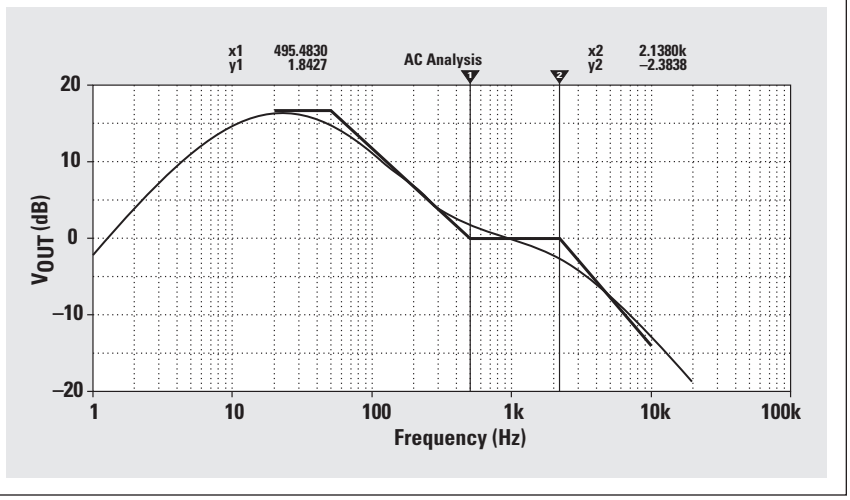
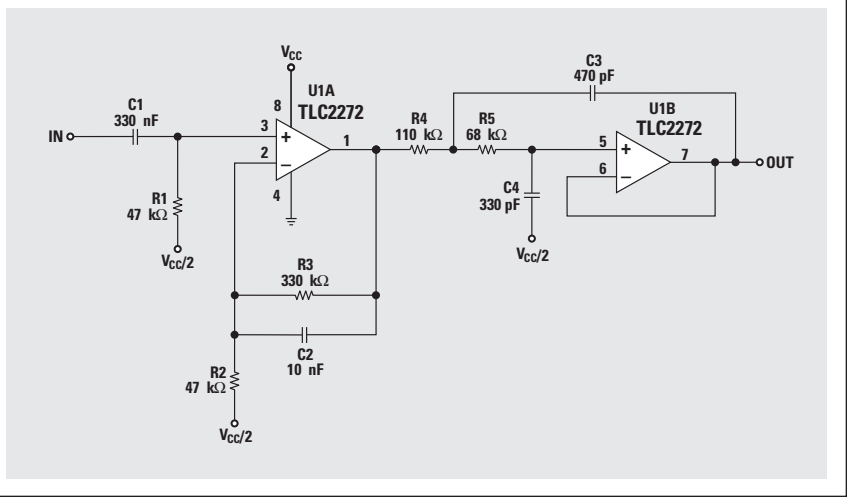


Figure 14. Unity-gain Sallen-Key equalizer



This circuit topology is very flexible. Most of the RIAA breakpoints are independently adjustable, as follows:

- R1 and C1 set the LFR as before.
- U1A, R2, and R3 control the overall gain of the circuit.
- R4 and R5 control the LFG.
- R5 and C2 control the 50-Hz LFB.
- C3, C4, C5, R6, R7, and U1C form a 500-Hz high-pass filter that reverses the effect of the 50-Hz low-pass filter and flattens the response through 1 kHz until the 2120-Hz low-pass filter begins to affect the response.
- R8, R9, R10, C6, C7, and U1D form the 2120-Hz low-pass filter as before, but the input resistor has been split into a summing resistor.

The overall response of the filter is shown in Figure 17.

The 500-Hz response is above the ideal curve by 0.8 dB, and the 2120-Hz response is below the ideal curve by –1.3 dB. This circuit is about the best that can be created without many more op amps and complex design techniques. It should produce very aesthetically pleasing sound reproduction.

References

1. "Audio Circuits Using the NE5532/34," Philips Semiconductor (October 1984).
2. *Audio Radio Handbook*, National Semiconductor (1980).
3. "Op Amp Circuit Collection," National Semiconductor AN-031 (1978).

Related Web sites

www-s.ti.com/sc/techlit/slyt023
www.ti.com/sc/amplifiers
www.ti.com/sc/device/tlc2274
www.vwlowen.demon.co.uk/java/riaa.htm

Figure 15. Response of the Sallen-Key stage

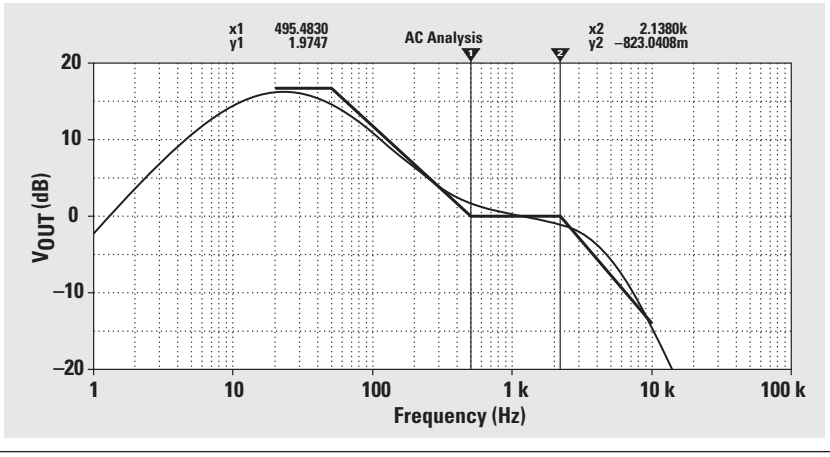


Figure 16. Filter with four op amps

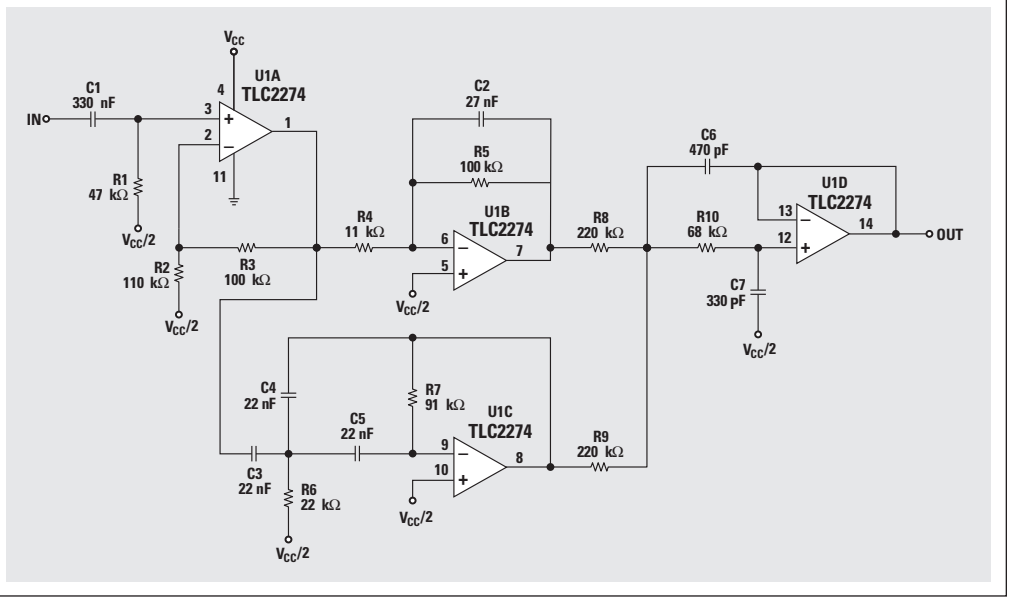
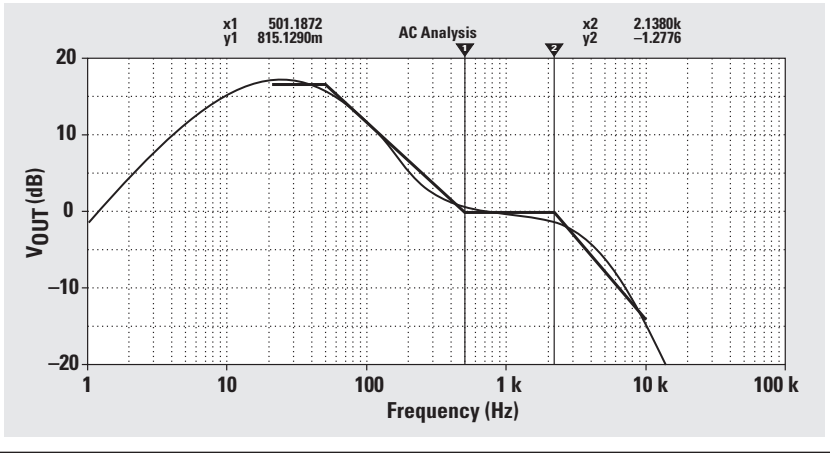


Figure 17. Response of filter with four op amps



Frequency response errors in voltage feedback op amps

By Ron Mancini
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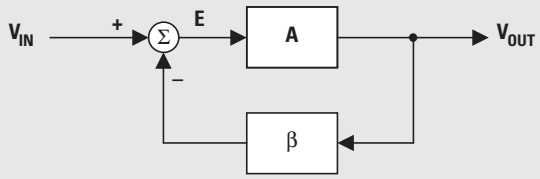
Introduction

An article entitled "Matching operational amplifier bandwidth with applications" appeared in the February 2000 issue of *Analog Applications Journal*. It attempted to analyze errors incurred when op amps are operated on the decreasing portion of the bandwidth curve, but a small mistake confused the explanation. This article focuses on the error analysis, so each equation is analyzed in detail. Further, the error analysis is completed for the inverting and non-inverting op amp configurations; thus the error function is analyzed as a function of circuit configuration as well as frequency.

Figure 1. Basic feedback loop



Feedback theory

The basic feedback circuit is shown in Figure 1, where E is the error voltage, β is the feedback factor, and A is the forward gain. Equations 1 and 2 govern the circuit performance.

$$V_{OUT} = EA \quad (1)$$

$$E = V_{IN} - \beta V_{OUT} \quad (2)$$

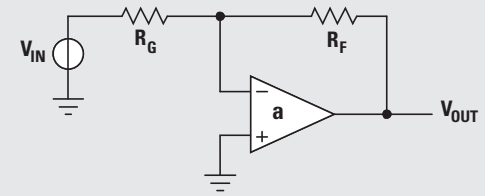
The accuracy equation (Equation 3) and closed-loop gain equation (Equation 4) are obtained by combining Equations 1 and 2.

$$\frac{E}{V_{IN}} = \frac{1}{1 + A\beta} \quad (3)$$

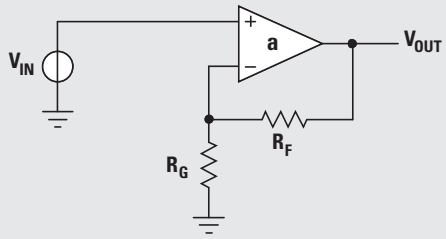
$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad (4)$$

The quantity Aβ appears in both equations and is called loop gain because it has a special significance in feedback circuits. The loop gain determines the stability of a feedback circuit as shown in Equation 4 (instability or oscillation occurs when $A\beta = -1$), and it determines accuracy as shown in Equation 3. Accuracy and stability are inversely related—i.e., stability decreases as accuracy increases, and vice versa. The loop gain is calculated with the voltage inputs grounded (current inputs open), so the input signal and its insertion point (plus or minus input) have no effect on the loop gain. This means that the loop gain for a non-inverting, inverting, or differential op amp circuit is the same. Three op amp circuits are shown in Figure 2, and the loop gain for all three circuits is given in Equation 5.

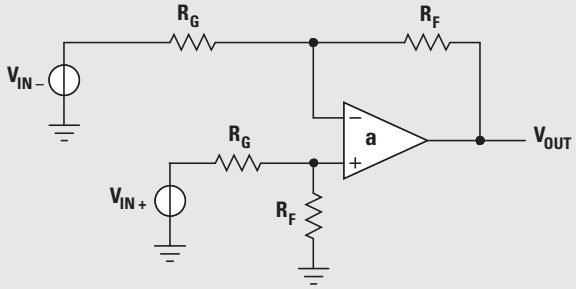
Figure 2. Op amp circuits



(a) Inverting Op Amp



(b) Non-inverting Op Amp



(c) Differential Op Amp

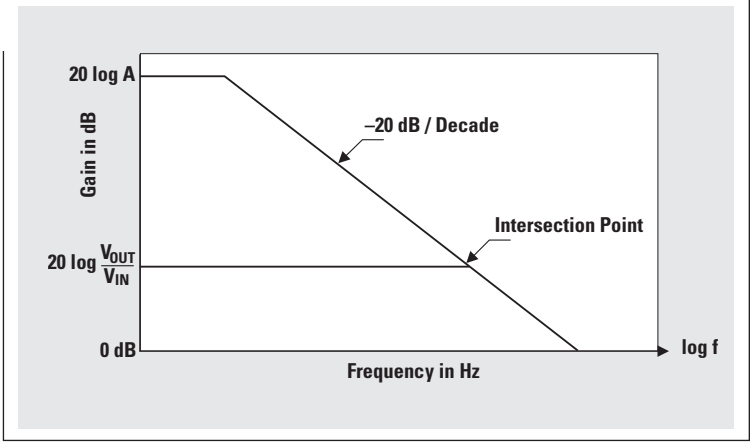
$$A\beta = \frac{aR_G}{R_F + R_G} \quad (5)$$

The parameter "a" is the open-loop gain of the op amp and is often confused with the forward gain "A" in the basic feedback circuit (see Figure 1). The op amp's open-loop gain, a, decreases with frequency and is included in the forward gain, A; hence the error increases with frequency, as indicated by Equation 3. A more in-depth analysis of stability and feedback is found in References 1 and 2.

Equation 6 is the log of Equation 4 and is plotted in Figure 3.

$$20\log\left(\frac{V_{OUT}}{V_{IN}}\right) = 20\log(A) - 20\log(1 + A\beta) \quad (6)$$

Figure 3. Plot of op amp equation



The plot of Equation 6 assumes that one pole is contained in the forward gain; thus the forward gain rolls off with a slope of –20 dB/decade. If more poles are included in the forward gain, the curve rolls off faster. The closed-loop gain is constant until it intersects the forward-gain curve, then it follows the forward-gain curve down at a –1 slope (–20 dB/decade). The closed-loop gain is down –3 dB at the apparent intersection of the curves shown in Figure 3, but we never work close to the intersection because the error is too big at the intersection frequency. The difference between curves in Figure 3 is 20 log(1+Aβ) as defined in Equation 6. The β portion of the loop gain does not vary with a frequency change because it is resistive (at least in this example), but the op amp gain contains a pole making it responsible for the gain roll-off. Setting the input signal equal to 1 V normalizes the error voltage at E = 1/ (1+Aβ); and, under these conditions, the loop gain determines the error caused by the decreasing amplifier gain.

The open-loop gain plot of the TLV247x op amp is shown in Figure 4. This is a plot of the op amp's typical open-loop gain characteristics. In an attempt to relate this curve to a data-sheet specification, we will calculate the dc intercept of the differential voltage gain (DVG). The typical DVG curve given in the data sheet does not show the low-frequency data; thus we must reconstruct the curve at its dc intercept. From Figure 4 we observe that the DVG at 100 Hz is approximately 87 dB; the slope in the linear portion of the curve is –20 dB/decade (–6 dB/octave); and, if we back up one decade to 10 Hz, the DVG is 87 + 20 = 107 dB. If we now back up an octave to 5 Hz, the DVG is 107 + 6 = 113 dB. The large signal differential voltage amplification (AVD) is specified on the data sheet as 116 dB typical at dc. The two specifications match up fairly well because DVG = 113 dB at 5 Hz, so we accept the data-sheet typical value of op amp open-loop gain equal to 116 dB. The AVD guaranteed minimum specification is 90 dB; hence the typical curve is reduced by 116 dB – 90 dB = 26 dB to turn Figure 4 into a guaranteed curve—i.e., 107 – 26 = 81 dB at f = 10 Hz. The data for the new curve is given in Table 1.

Table 1. Guaranteed minimum bandwidth of TLV247x

FREQUENCY (Hz)	GAIN (dB)
10	81
100	61
1000	41
10,000	21
100,000	01

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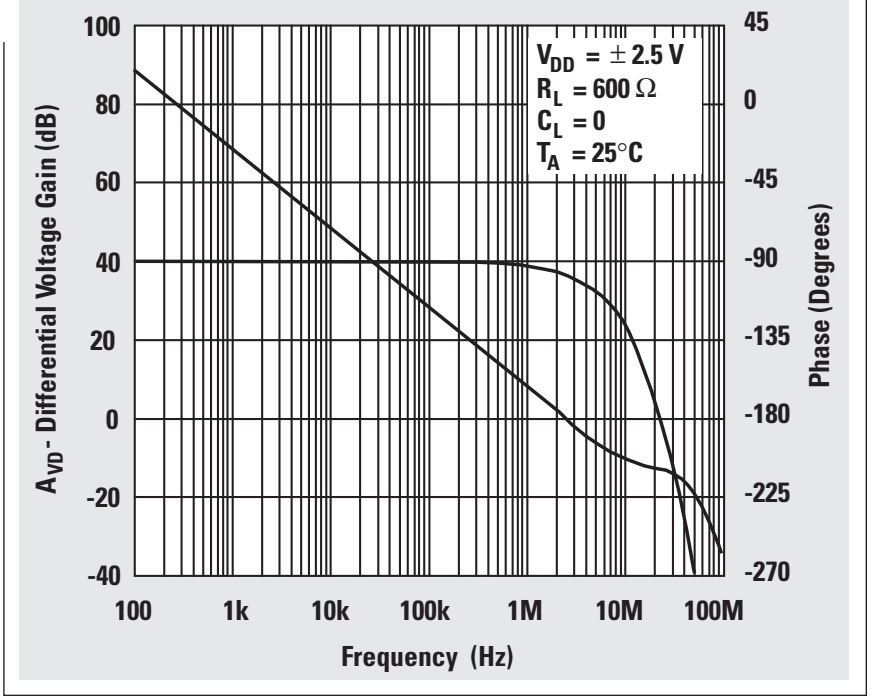
Figure 4. Open-loop gain plot of the TLV247x



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Non-inverting op amp

The non-inverting closed-loop gain is

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta} = \frac{a}{1+\frac{aR_G}{R_F+R_G}}. \quad (7)$$

When the op amp is used in the non-inverting circuit configuration, the forward gain, A, equals the op amp open-loop gain, a. In Equation 8, 20 log(1+Aβ) is calculated for the following conditions: the closed-loop gain is 2 (6 dB), the input signal is 10 Hz, and 20 log(a) = 81 dB. The error is calculated in Equation 9; notice that 1 is negligible compared to a very high aβ, and 20 log(1+Aβ) = 20 log(1+aβ).

$$20\log(1+a\beta) = 20\log(a) - 20\log\left(\frac{V_{OUT}}{V_{IN}}\right) = 81\text{ dB} - 6\text{ dB} = 75\text{ dB} \quad (8)$$

$$E = \frac{1}{1+a\beta} = \frac{1}{10^{\frac{dB}{20}}} = \frac{1}{10^{\frac{75}{20}}} = \frac{1}{5623.4} = 0.1778\text{ mV} \quad (9)$$

If the closed-loop gain is changed to 10 (20 dB) for an input signal of 10 Hz, then 20 log(1+Aβ) = 61 dB, and the error is 0.89 mV. Notice that the error, E, increases as the closed-loop gain increases because the loop gain decreases when the closed-loop gain increases. When the closed-loop gain is kept constant at 20 dB and the input signal frequency is increased to 1000 Hz, the error increases to 89.1 mV. Notice that the error increases as the signal frequency increases because the op amp gain decreases with increasing frequency. If oscilloscope probes are placed across the inputs of an op amp, the differential voltage observed is the error voltage, and one can observe the error voltage increase as the signal frequency is increased.

Inverting op amp

The inverting closed-loop gain is

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta} = \frac{\frac{-aR_F}{R_F+R_G}}{1+\frac{aR_G}{R_F+R_G}}. \quad (10)$$

The inverting op amp circuit's forward gain does not equal the op amp open-loop gain; rather, it is modified by a combination of the gain setting resistors. When the closed-loop gain is 2 (6 dB), $R_F = 2R_G$. The circuit's forward gain, A, is

$$|A| = \left|\frac{aR_F}{R_F+R_G}\right| = \left|\frac{a2R_G}{2R_G+R_G}\right| = \frac{2a}{3}. \quad (11)$$

The op amp open-loop gain at f = 10 Hz is

$$a = 10^{\frac{81}{20}} = 10^{4.05} = 11{,}220.2. \quad (12)$$

The op amp open-loop gain is reduced by the two-thirds factor to obtain the forward gain:

$$A = \frac{2a}{3} = \frac{2(11{,}220.2)}{3} = 7480.1. \quad (13)$$

Then the forward gain is converted back to dB:

$$A = 20\log(7480.1) = 77.48\text{ dB}. \quad (14)$$

Equation 6 is repeated in Equation 15, where 20 log(1+Aβ) is calculated for a closed-loop gain of 2 (6 dB) and an input signal of 10 Hz.

$$20\log(1+A\beta) = 77.48\text{ dB} - 6\text{ dB} = 71.48\text{ dB}. \quad (15)$$

The error is given by

$$E = \frac{1}{1+A\beta} = \frac{1}{10^{\frac{dB}{20}}} = \frac{1}{10^{\frac{71.48}{20}}} = \frac{1}{3749.7} = 0.266\text{ mV}. \quad (16)$$

Because the forward gain is decreased by the closed-loop gain, the error for the inverting op amp—at the same closed-loop gain and input signal frequency—is higher than it is for the non-inverting op amp. The error is calculated for a closed-loop gain of 10 (20 dB and $R_F = 10R_G$); and an input signal of 10 Hz is calculated in the following equations.

$$|A| = \left|\frac{aR_F}{R_F+R_G}\right| = \left|\frac{a10R_G}{10R_G+R_G}\right| = \frac{10a}{11} \quad (17)$$

$$A = \frac{10a}{11} = \frac{10(11{,}220.2)}{11} = 10020 \quad (18)$$

$$A = 20\ \log(10020) = 80.02\ \text{dB} \quad (19)$$

$$20\log(1+A\beta) = 80.02\text{ dB} - 20\text{ dB} = 60.02\text{ dB} \quad (20)$$

$$E = \frac{1}{1+A\beta} = \frac{1}{10^{\frac{dB}{20}}} = \frac{1}{10^{\frac{60.02}{20}}} = \frac{1}{1002.3} = 0.9977\text{ mV} \quad (21)$$

Again, the error increases as the closed-loop gain increases, and the error will increase when the input signal frequency increases.

Measurements

Error voltages are hard to measure at low frequencies because they are very small voltages, thus error measurements are taken at higher frequencies. When two error measurements are separated by a frequency decade they should have a voltage difference of 20 dB, and this voltage difference acts as a check on the measurement technique. Instrumentation is kept at a minimum in these measurements so they can be easily repeated.

Configure the subject op amp as an inverting amplifier as shown in Figure 2a, with a gain of one ($R_F = R_G$). Set the input voltage to 1 V, and measure the voltage from the inverting input to ground. The measured error voltages are E = 2.83 mV at f_{IN} = 10 kHz and E = 28.3 mV at f_{IN} = 100 kHz. The error voltages differ by a factor of 10; thus the slope of the forward-gain curve is –20 dB/decade. Obtaining the correct slope indicates that the error measurements are probably correct. Equation 22 calculates the quantity (1+Aβ) at the 100-kHz input frequency.

$$(1+A\beta) = \frac{1}{E} = \frac{1}{0.0283} = 35.33 \quad (22)$$

Equation 23 takes the log of Equation 22.

$$20 \log(35.33) = 31 \text{ dB} \quad \textbf{(23)}$$

For very large values of A, $V_{OUT}/V_{IN} = 1/\beta$; thus $20 \log(V_{OUT}/V_{IN}) = 20 \log(1) = 0$. Equation 6 reduces to Equation 24 when $\beta = 1$ and A is very large.

$$20 \log(A) = 20 \log(1 + A\beta) = 31 \text{ dB} \quad \textbf{(24)}$$

Equation 25 relates the forward gain to the op amp gain.

$$A = \frac{aR_F}{R_F + R_G} = \frac{aR_F}{R_F + R_F} = \frac{a}{2} \quad \textbf{(25)}$$

$$a = 2A = 2(31 \text{ dB}) = 6 \text{ dB} + 31 \text{ dB} = 37 \text{ dB} \quad \textbf{(26)}$$

Three values for op amp open-loop gain (f_{IN} = 100 kHz) have been taken from a data-sheet curve, calculated, and measured; and these values are given in Table 2.

Table 2. Comparison of op amp open-loop gains

HOW OBTAINED	a (dB)
Data sheet curve	27
Worst-case calculation	01
Measurement and calculation	37

The measured data supports the data-sheet typical curves much better than does the calculated worst case data. The measured error voltages of several op amps ranged from 32 mV to 26 mV, so this batch of op amps has much higher than nominal gain (10 dB higher). Since this will not always be the case, it is prudent to design with the worst-case specifications developed in Table 1.

Conclusions

The first conclusion is that the error increases at higher input-signal frequencies. This is because the gain bandwidth is constant in voltage-feedback op amps.

The second conclusion is that the non-inverting circuit configuration has less error than the inverting circuit configuration, and the error difference is greater at low closed-loop gains.

The third conclusion is that the error in a differential amplifier circuit constructed with a single op amp is different for the inverting and non-inverting inputs. This difference causes some of the common-mode input voltage to feed through to the output as a differential error voltage. The inverting and non-inverting input impedances are different in a single op amp differential amplifier; and this, coupled with the single op amp error amplification, precludes use of the single op amp differential amplifier in demanding applications. Multiple op amp differential amplifiers or instrumentation amplifiers are used in the demanding applications.

There is phase shift associated with the amplifier gain, a, and these calculations have neglected that phase shift for clarity's sake. The error introduced by neglecting the feedback phase shift is small and usually negligible except near the intersection point (Figure 3), but the error at that point is so large that very few people operate an op amp there.

References

For TI information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the following document.

Document Title **TI Lit. #**

1. "Feedback Amplifier Analysis Tools," Application Report sloa017
2. "Stability Analysis of Voltage-Feedback Op Amps Including Compensation Techniques," Application Report sloa020
3. "Current Feedback Amplifier Analysis and Compensation," Application Report . . .sloa021

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Synthesis and characterization of nickel manganite from different carboxylate precursors for thermistor sensors

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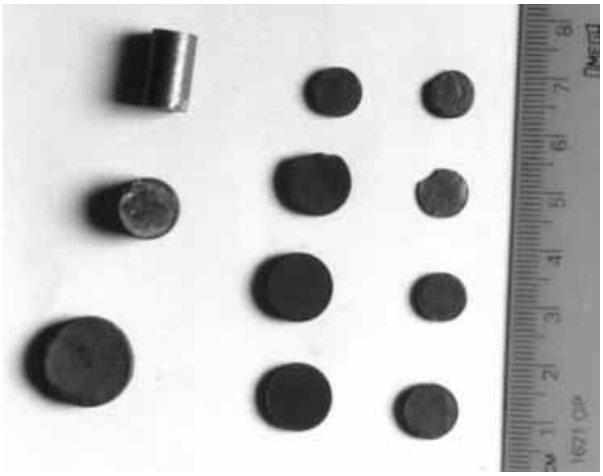
Introduction

The thermistor sensor is a widely used temperature transducer synthesized with a ceramic-like semiconductor material. Its basic temperature-sensing mechanism is the population of charge carriers in the conduction band. Initially the thermistor was designed for use during World War II, but since then it has continuously evolved for applications such as thermometers, temperature controllers, automatic gain control, and time-delay circuits. Its number of applications is increasing rapidly, encompassing office automation equipment, air conditioners, and other domestic appliances. Recently the thermistor has come into the limelight due to its use in portable phones, car phones, and transceivers. Expanding applications in delicate communications equipment and the rapid influx of such equipment into the consumer market has forced thermistor manufacturers to consider improving the specifications. In this article the authors investigate various thermistor anomalies from a materials point of view. Figure 1 shows thermistor samples we manufactured in various sizes. The small samples are suitable for applications where speed of measurement is crucial.

The thermistor sensor offers various advantages: high sensitivity; availability in a large range of resistance values (useful from a power dissipation point of view); ability to operate over a wide temperature range in a solid, liquid, or gaseous environment; adaptable size and shape for a wide variety of mechanical environments; ability to withstand electrical and mechanical stress; and low cost. At the same time, this sensor has several limitations: lack of interchangeability; poor linearity and precision; limited range; instability at high temperatures; hysteresis; and low resolution. With the advent of microprocessors and microcontrollers, most of these drawbacks are no longer a problem except for lack of interchangeability. The authors investigate remedies for the bottlenecks posed by thermistors in References 16, 17, and 18. On several occasions we observed that the thermistor-based circuit needs tuning when it is changed. The reasons for lack of interchangeability are loose manufacturing standards and manufacturers' ignorance of standard material characterization tools used to check completion of solid-state reactions (formation).

Figure 1. Thermistor samples



Materials used

At present the thermistor materials of interest and use are mixed metal oxides (especially spinels) of manganese, nickel, cobalt, copper, iron, and titanium. The authors of References 1–5 show an interest in transition metal manganite, $Mn_{3-x}M_xO_4$ [$(0 < x < 1)$ and M = nickel, cobalt, etc.]. Nickel manganite, $NiMn_2O_4$, is a popular material for thermistors despite its poor stability at high temperature. The electrical conductivity is due to hopping between Mn^{3+} and Mn^{4+} ions in the octahedral sub-lattice of the spinel structure. In this article the carboxylate precursor method, used for the first time to synthesize $NiMn_2O_4$, is described. The different carboxylates used for precursor formation are fumarate, succinate, oxalate, tartarate, and malonate. The precursors as well as the $NiMn_2O_4$ obtained by thermal decomposition of these precursors have been characterized by X-ray diffraction, infrared analysis, and thermal analysis to study the formation and working.

Preparation

Different nickel manganese carboxylate precursors were prepared by using salts of carboxylic acid and metal chlorides. Following is a description of how the metal chloride solution and the precursors were prepared.

Preparation of metal chloride solution

Around 11.8854 g of $NiCl_2.6H_2O$ (0.5M) was accurately weighed on a Mettler balance and dissolved in distilled water. Similarly, 19.79056 g of $MnCl_2.4H_2O$ (1M) was also accurately weighed and dissolved in acidified water [to prevent formation of $Mn(OH)_2$]. Both salt solutions were

then mixed together to make the volume 100 ml in a standard volumetric flask. This metal chloride solution was then used for the preparation of the nickel manganese carboxylate precursors.

Preparation of nickel manganese fumarate (NMF)

Sodium fumarate was accurately weighed at 32.008 g (2M) and dissolved in distilled water; the total volume was made 100 ml in a standard flask. This solution was then heated to 80°C. The hot metal chloride solution was added drop-by-drop, with constant stirring, to this hot fumarate solution. The precipitate of nickel manganese fumarate that formed was filtered in a Buchner funnel using a Whatmann filter No. 41. It was washed with distilled water until it was free of chloride ions, then dried with diethyl ether and stored in a desiccator.

Preparation of other precursors

The other precursors—nickel manganese succinate (NMS), nickel manganese oxalate (NMO), nickel manganese tartarate (NMT), and nickel manganese malonate (NMM)—were also prepared in the same manner as described for NMF by using sodium succinate, ammonium oxalate, sodium tartarate, and sodium malonate, respectively, along with metal chloride.

Characterization

The nickel manganese carboxylate precursors were characterized by chemical analysis. The $NiMn_2O_4$ obtained by thermal decomposition of the carboxylate precursors was also characterized by X-ray diffraction and IR analysis. The results of all the characterizations are summarized in Tables 1-9.

Chemical analysis

The percentage of nickel and manganese in the precursors was estimated by using the standard methods described in Reference 23. The elemental analysis was carried out on an AAS 201 Chemito GBC902, double-beam atomic absorption spectroscope. The wavelengths used for nickel and manganese estimation were 352.4 nm and 403.1 nm, respectively. The standard solutions prepared for nickel and manganese were in the range of 6 to 25 µg/ml and 7 to 27 µg/ml, respectively.

IR analysis

IR analysis of the precursors and their decomposed products was carried out on Shimadzu FTIR instrument model 8101A. The pellets used for reading spectra were prepared by mixing 1 to 2 mg of the sample with a pinch of KBr. The IR spectra in the range of 400 to 4600 cm^{-1} was recorded at room temperature.

Density measurement

The pycnometric density measurement of the precursors and their decomposed products was determined at room temperature with CCl_4 as the medium by using the formula

ρ_{sample} = (weight of the sample)/(weight of the liquid displaced/density of the liquid).

Thermal analysis

The physical and chemical properties of the precursors were monitored by using thermal analysis techniques like isothermal weight loss studies, thermogravimetry analysis (TGA), and differential thermal analysis (DTA). For calculating the weight loss, precursors were accurately weighed and placed in silica crucibles, then heated in an oven for 20 minutes at various temperature ranges until the precursors exhibited no further weight loss. TGA was done on an STA 1500 instrument in air at a heating rate of 10°C/min. DTA was recorded on an STA 1500 instrument in air at a heating rate of 10°C/min.

X-ray diffraction (XRD) analysis

X-ray diffraction of the sintered and decomposed products was carried out on Philips X-ray Diffractometer model PW 3710 with Cu Kα radiation and nickel as a filter. The studies were carrried out to confirm the completion of solid state reaction, observe the impurity phases, and determine lattice constants, interplanar distances, octahedral and tetrahedral site radii, bond length, X-ray density, etc. The various parameters were calculated using standard values.

Formula fixation

Based on the characterization results previously described, a formula for each precursor was fixed as follows:

NMF: $NiMn_2(C_4H_2O_4)_3.4^1/_2H_2O$
NMS: $NiMn_2(C_4H_4O_4)_3.10H_2O$
NMO: $NiMn_2(C_2O_4)_3.6^1/_2H_2O$
NMT: $NiMn_2(C_4H_4O_6)_3.8H_2O$
NCM: $NiMn_2(C_3H_2O_4)_6.3H_2O$

Pellet formation

Some of the steps in thermistor manufacture are shown in Figure 2. The thermistors were fabricated by preheating, presintering, grinding, and shaping them to the desired geometry and by a final sintering at elevated temperature. The thermally decomposed product of the precursors was preheated in a silica crucible to 400°C to drive off

Continued on next page

Figure 2. Some steps in thermistor manufacture

The light-colored powder at the top is raw precursor. Below that is pre-sintered powder before and after it is finely ground and filtered. The weight loss that results is evident. Compressing the sintered precursor in a hydraulic press produces the finished thermistor.

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moisture. The preheated product was mixed thoroughly by grinding and then was compressed under 5 tons per square inch of pressure in a hydraulic press in a round die. These pellets were then heated to 900°C under a controlled temperature profile using a PID controller. The final products were disc thermistors with diameters of 1 mm (0.04 in.) to 3 mm (0.12 in.), targeting low-cost thermometry applications for domestic use.

Results and conclusion

This article presents our work on the preparation of nickel manganese carboxylates by various precursor methods; viz., nickel manganese fumarate, nickel manganese succinate, nickel manganese oxalate, nickel manganese tartarate, and nickel manganese malonate. Various characterization tools were applied to these precursors to verify the formation. The asymmetric and symmetric stretching of carboxylate ions was seen in the range of 1550 to 1625 cm^{-1} and 1350 to 1400 cm^{-1}, respectively, with $\Delta\nu$ (ν_{asys} - ν_{sys}) separation of ~190 to 240 cm^{-1}, indicating the monodentate linkage of both carboxylates in the dianions. Thus the carboxylates coordinated to the metal as bidentate ligand via both carboxylate groups. Almost all the hydrate nickel manganese carboxylate precursors decomposed below 400°C to form $NiMn_2O_4$. Most of the dehydration took place below 250°C, while the decarboxylation of anhydrous precursors occurred between 250 and 400°C. XRD confirmed the formation of $NiMn_2O_4$. The lattice parameter values of all the samples agreed well with the reported ones. The IR data of $NiMn_2O_4$ showed high-frequency band $\nu1$ between 600 and 620 cm^{-1} and low-frequency band between 450 and 460 cm^{-1}. The I-V characterization of all the samples up to 200°C with four-probe setup revealed their thermistor behavior. The low value of resistivity at room temperature was attributed to the presence of moisture.

Table 1. Infrared data of hydrated nickel manganese carboxylates

CARBOXYLATES	INFRARED DATA				cm^{-1}	
	$\nu(H_2O)$	ν_{asym}(O-C-O)	ν_{sym}(O-C-O)	δ(O-C-O)	ν(M-O) + ν(C-C)	ν(CH=CH)
NMF	3475	1580	1390	800	590	990
	3400	1560				
NMS	3400	1550	1350	800	660	—
			1400			
NMO	3400	1625	1360	840	495	—
NMT	3400	1575	1380	800	575	—
NCM	3400	1575	1400	840	565	—
					530	

Table 2. Chemical analysis, total weight loss and density of hydrated nickel manganese carboxylates

CARBOXYLATES	CHEMICAL ANALYSIS				TOTAL WEIGHT LOSS (%)		DENSITY (gcm^{-3})
	NICKEL (%)		MANGANESE (%)				
	OBS.	CALC.	OBS.	CALC.	OBS.	CALC.	
NMF	9.4315	9.9176	17.855	18.5663	60.62	60.70	1.7929
NMS	10.8211	8.4217	14.28	15.7657	66.63	66.65	2.0192
NMO	9.8526	10.6768	20.8	19.98	57.46	57.38	2.1585
NMT	6.95	7.7545	15.34	14.5168	69.45	69.72	1.7304
NCM	11.00	11.1003	16.02	20.7804	56.14	56.01	1.7534

Table 3. Isothermal weight loss and TGA/DTA of nickel manganese carboxylates

CARBOXYLATES	TGA (AIR)		DTA PEAKS	ISOTHERMAL WEIGHT LOSS		
	TEMPERATURE RANGE (°C)	WT. LOSS (%)	EXO/ENDO PEAKS (°C)	TEMPERATURE RANGE (°C)	WT. LOSS (%)	REMARKS
NMS	RT–91.22	0.62		RT–100	16.80	Loss of $6\frac{1}{2}$ H_2O
	91.22–176.8	26.002	135.27 (endo)	100–120	6.40	Loss of $2\frac{1}{2}$ H_2O
				120–140	4.66	
	176.8–396.76	28.596	331.7 (exo hump)	140–250	22.24	Loss of 1 H_2O
			387.44 (broad exo)	250–380	11.93	
	396.76–526	11.081–0.376				Decarboxylation to form $NiMn_2O_4$
	526–790		602.04 (exo)			

Table 4. Isothermal weight loss studies of hydrated nickel manganese carboxylates

CARBOXYLATES	TEMPERATURE RANGE (°C)	WEIGHT LOSS (%)	REMARKS
NMF	RT–120	7.61	Loss of 2½ H_2O
	120–140	2.69	Loss of 1 H_2O
	140–250	3.21	Loss of 1 H_2O
	250–280	48.19	Decarboxylation to form $NiMn_2O_4$
NMO	RT–100	14.74	Loss of 4½ H_2O
	100–160	1.64	Loss of ½ H_2O
	160–200	4.92	Loss of 1½ H_2O
	200–280	36.39	Decarboxylation to form $NiMn_2O_4$
NMT	RT–100	10.11	Loss of 4 H_2O
	100–120	2.38	Loss of 1 H_2O
	120–180	4.17	Loss of 2 H_2O
	180–225	2.33	Loss of 1 H_2O
	225–250	3.53	Decarboxylation to form $NiMn_2O_4$
	250–380	46.70	
NMM	RT–120	1.73	Loss of ½ H_2O
	120–170	4.90	Loss of 1½ H_2O
	170–180	2.75	Loss of 1 H_2O
	180–260	32.65	Decarboxylation to form $NiMn_2O_4$
	260–380	3.90	

Table 5. X-ray diffraction data of $NiMn_2O_4$ (NMF)*

SR. NO.	2θ (°)	d_{obs} (A°)	d_{calc} (A°)	HKL
1	30.25	2.9545	2.9611	220
2	35.55	2.5252	2.5252	311
3	43.20	2.0941	2.0938	400
4	53.60	1.7098	1.7096	422
5	57.05	1.6143	1.6132	333
6	62.80	1.4795	1.4805	440

*Lattice parameter a = 8.39805
Structure—cubic

Table 6. X-ray diffraction data of $NiMn_2O_4$ (NMS)*

SR. NO.	2θ (°)	d_{obs} (A°)	d_{calc} (A°)	HKL
1	18.33	4.8481	4.8441	111
2	30.16	2.9676	2.9664	220
3	35.54	2.5298	2.5298	311
4	37.17	2.4226	2.4221	222
5	43.20	2.0976	2.0975	400
6	53.61	1.7122	1.7127	422
7	62.78	1.4825	1.4832	440
8	75.35	1.2634	1.2649	622

*Lattice parameter a = 8.39005
Structure—cubic

Table 7. XRD data of $NiMn_2O_4$ obtained from carboxylates (NMO)*

SR. NO.	2θ (°)	d_{obs} (A°)	d_{calc} (A°)	HKL
1	18.36	4.8289	4.8449	111
2	30.13	2.9705	2.9705	220
3	35.49	2.5333	2.5333	311
4	37.15	2.4238	2.4254	222
5	43.14	2.1002	2.1003	400
6	53.53	1.7146	2.7151	422
7	57.23	1.6124	1.6169	333
8	62.84	1.4813	1.4853	440
9	74.15	1.2809	1.2813	533
10	75.18	1.2658	1.2666	622

*Lattice parameter a = 8.397742
Structure—cubic

Table 8. X-ray diffraction data of $NiMn_2O_4$ (NMT)*

SR. NO.	2θ (°)	d_{obs} (A°)	d_{calc} (A°)	HKL
1	30.15	2.9641	2.9692	220
2	35.45	2.5321	2.5321	311
3	43.25	2.0918	2.0995	400
4	53.70	1.7068	1.7143	422
5	57.10	1.6130	1.6162	333
6	62.7	1.4817	1.4845	440

*Lattice parameter a = 8.38848
Structure—cubic

Table 9. X-ray diffraction data of $NiMn_2O_4$ (NMM)*

SR. NO.	2θ (°)	d_{obs} (A°)	d_{calc} (A°)	HKL
1	35.53	2.5308	2.5308	311
2	37.34	2.4122	2.4230	222
3	43.37	2.0898	2.0984	400
4	57.31	1.6103	1.6154	333
5	63.01	1.4778	1.4838	440

*Lattice parameter a = 8.37677
Structure—cubic

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