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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

Auto-Track™ voltage sequencing simplifies simultaneous power-up and power-down

By Chris Thornton (Email: cthornton@ti.com)
Plug-in Power Solutions

Auto-Track Sequencing is a feature available on select power modules in the Texas Instruments (TI) Plug-in Power Solutions family. The feature is designed to simplify the amount of external circuitry required to configure the modules for simultaneous power-up and power-down supply voltage sequencing.

The ability to sequence the power-up of multiple supply voltages in complex logic and mixed-signal applications has become an important requirement for power-system designers. This is because most VLSI logic devices—including DSPs, ASICs, FPGAs, and microprocessors—now require at least two supply voltages. This usually includes a low voltage to power a high-speed logic core; a standard logic voltage to power the input/output (I/O) interface; and supporting system devices such as memory, data converters, and I/O ports.

The power-up sequencing techniques can be implemented with a number of techniques.[1, 2] The implementation of any one method depends largely on the time and/or voltage restrictions that are allowed between the two supply voltages during both power-up and power-down. The restrictions are imposed on the power-system designer by the respective VLSI device manufacturers. Failure to meet the restrictions can result in undue voltage stress and even "latch up" between the VLSI device's I/O port and a supporting peripheral. This can result in immediate, if not latent, damage to the VLSI device. In the latter case the long-term reliability of the affected device may be compromised.[2]

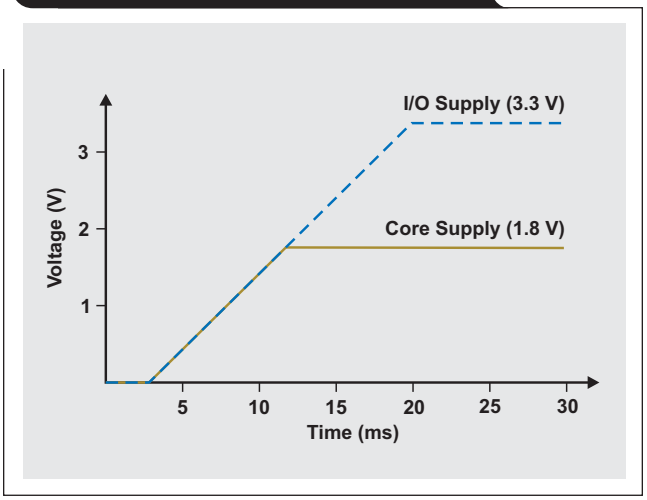
Simultaneous power-up

One of the most widely used power-up sequencing methods is the simultaneous power-up of the circuit supply voltages. See Figure 1. The core and I/O power-supply voltages must begin rising together at the same rate. The two voltages continue to rise until the core supply reaches its nominal regulation voltage. The higher I/O voltage then continues to rise until it too reaches its regulation voltage.

Of the many alternative techniques, the *simultaneous* method is the more accepted for most dual-supply voltage applications. This is because it significantly reduces the voltage difference that can occur between the two voltage rails throughout the power-up sequence. However, it is not a universal answer for every application. As a rule, VLSI device manufacturers do not specify which sequencing method should be used, only the voltage and time restrictions that must be adhered to during power-up.

Although most widely accepted, the simultaneous power-up method is more difficult to implement. It requires that one or more of the power-supply circuits (generating the supply voltages) be precisely controlled during the power-up period. This level of control not only adds components but also requires that the power designer have intimate knowledge of the power-supply regulation circuitry. While this may not be a problem for the designer of a discrete power supply, it adds an unwelcome level of complexity for designers who prefer to use off-the-shelf power-supply modules.

Figure 1. Simultaneous power-up of the core and I/O voltages



Introducing Auto-Track Sequencing

Auto-Track Sequencing is incorporated into many of the wide-output, adjustable power modules in the PTH series of Plug-in Power Solutions. Products with this feature include circuitry that allows their output voltage to follow a control signal when it is below the module's set-point voltage. The feature specifically enables the output voltage to be directly controlled during power-up and power-down transitions. The control signal can be a system-wide master ramp waveform, the output voltage of another power supply circuit, or the module's own internal RC ramp.

How Auto-Track Sequencing works

Auto-Track Sequencing uses a control pin called "Track" to control the output voltage of the module over a range of 0 V up to the nominal set-point voltage. Within this range the voltage at the module's output will follow the voltage applied to the Track pin on a volt-for-volt basis. However, once the voltage at the Track pin is raised above the module's set-point voltage, the module's output remains at its set-point voltage. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V; but if

the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

Since the output from the module simply follows that at the Track pin, it can track virtually any voltage source during the power-up sequence. For the designer's convenience, each Track pin is also provided with its own RC charge circuit that can produce a suitable rising voltage from the input source voltage.

Typical application

The basic implementation of Auto-Track Sequencing allows for simultaneous voltage sequencing of any number of modules that are compliant with this feature. The Track control pins of two or more modules are merely connected together (see Figure 2), which does two things: (1) It forces the Track control of the modules to follow the same collective RC ramp waveform; and (2) it also allows them to be controlled through a single transistor or switch, Q1.

To initiate the power-up sequence, it is recommended that the Track control first be pulled to ground potential. This must be done at or before input power is applied to the modules, and for 20 ms thereafter. This brief period gives the modules time to complete their respective internal power-up sequences so that they are ready to produce an output voltage. A logic-level high signal at the on/off control input turns Q1 on and holds the Track control at ground potential. It should be noted that after the input voltage has stabilized, the output of all modules will remain at 0 V until Q1 is turned off.

After 20 ms, Q1 may be turned off by applying a logic-level, low-drive voltage to the circuit's on/off control. This allows the Track control voltage to rise toward the modules' input voltage automatically. During this period, the output voltage of each respective power module follows the common Track control voltage, rising in unison with other modules to its set-point voltage.

Figure 2. Simplest implementation of Auto-Track voltage sequencing for power-up and power-down

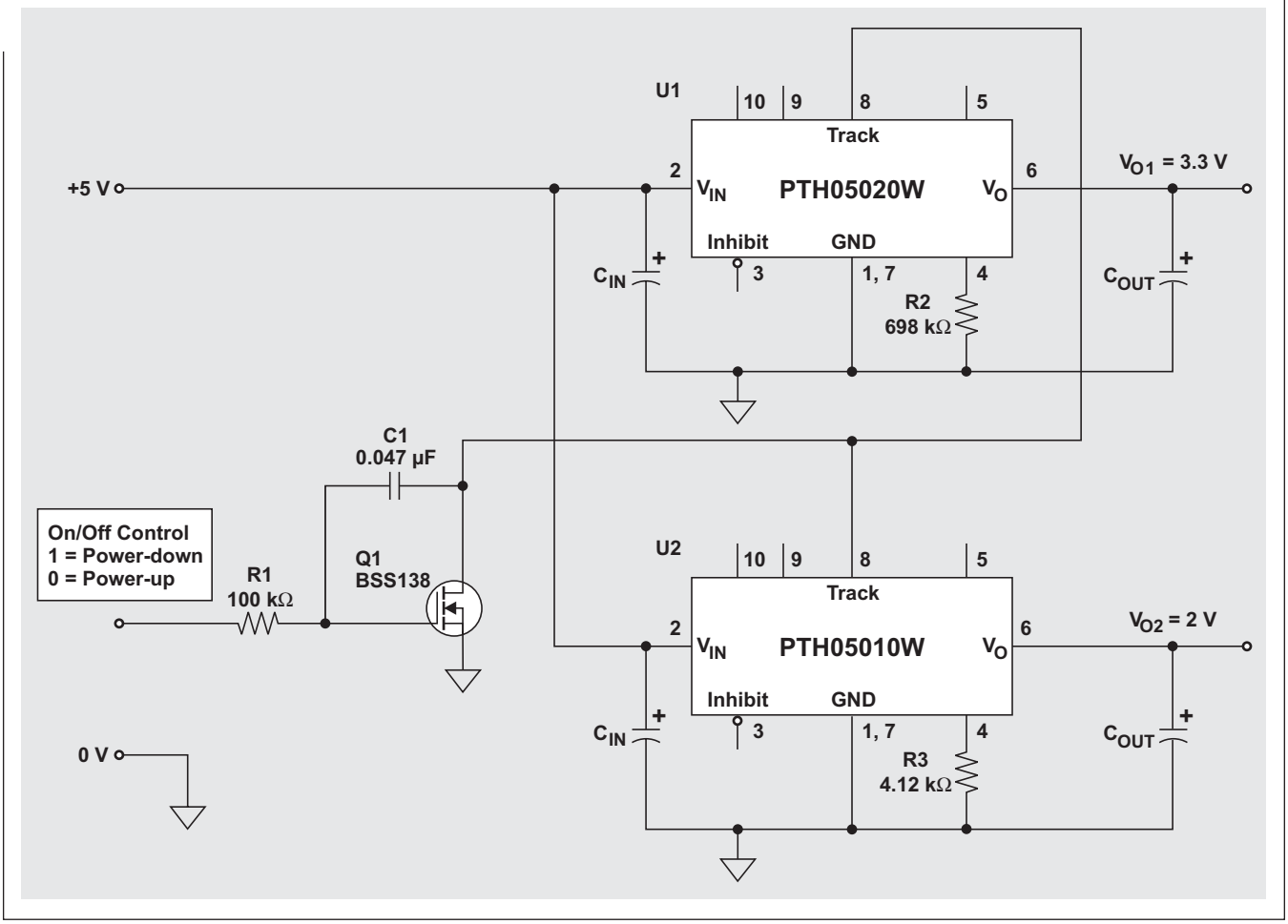


Figure 3 shows the output voltage waveforms from the circuit in Figure 2 after the on/off control voltage to the circuit is set from a high to a low level. The waveforms, V_{O1} and V_{O2}, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (2.0 V), respectively. Figure 3 shows the output voltages, V_{O1} and V_{O2}, rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence, although this is not always a strict requirement. Power-down is the reverse of power-up and is accomplished by lowering the Track control voltage back to 0 V. An important constraint is that the input voltage must be present until the sequence is complete. Q1 must be turned off relatively slowly so that the Track control voltage does not fall faster than Auto-Track Sequencing's slew-rate capability, which is 5 V/ms. The components R1 and C1 in Figure 2 limit the rate at which Q1 can pull down the Track control voltage. The values of 100 kΩ and 0.047 µF correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the on/off control input to the circuit. Figure 4 shows the waveforms of V_{O1} and V_{O2} after the on/off control voltage goes high. Although the Track control voltage begins its downward slope immediately, there is a short time delay before it reaches the voltage of the highest output. As the Track control voltage falls below the nominal set-point voltage of each power module, the respective output decays with all the other modules under Auto-Track Sequencing control.

Simultaneous power-up and power-down from another power module

One of the most powerful attributes of the Auto-Track Sequencing feature is its flexibility. The Track pin of any power module compliant with Auto-Track Sequencing will follow almost any voltage up to a slew rate of 5 V/ms. This includes the output voltage of another power module, even a module that is not compliant with this feature.

Figure 3. Simultaneous power-up of two modules under Auto-Track Sequencing control

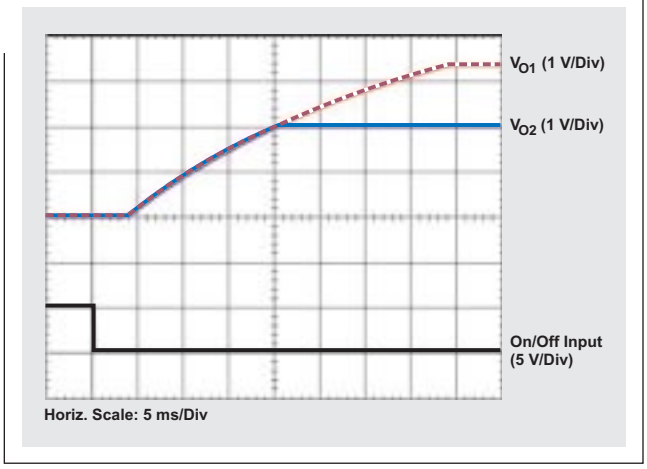


Figure 4. Simultaneous power-down of two modules under Auto-Track Sequencing control

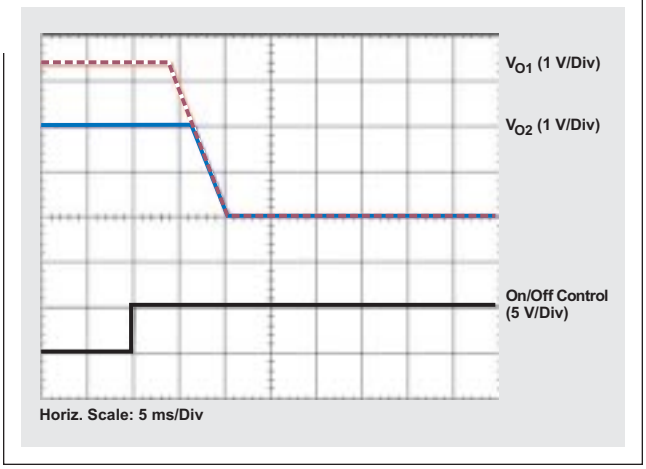


Figure 5. Sequenced power-up and power-down with other modules

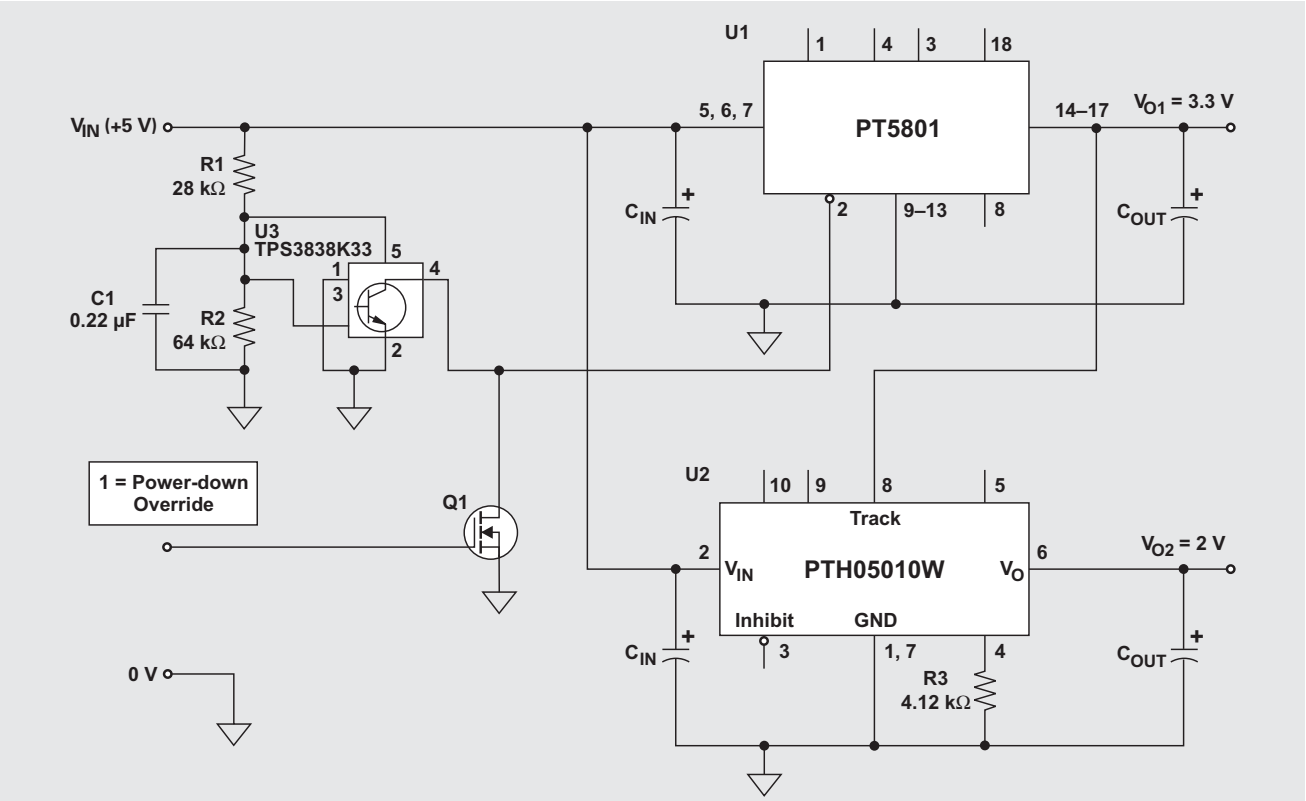
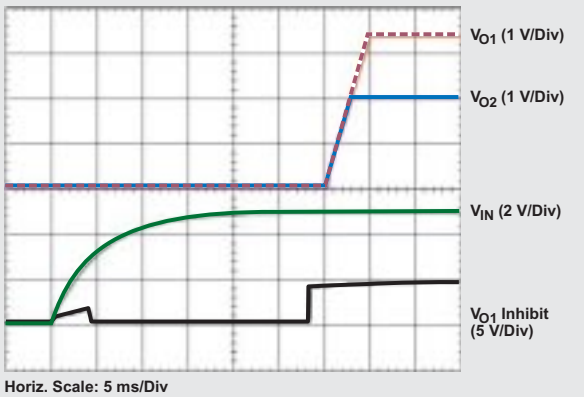


Figure 5 illustrates this arrangement. The Track pins of the lower-voltage modules must be connected directly to the output of the module with the *highest* output voltage, which in this case is PT5801 (U1). In this configuration, U1 must be controlled from its on/off Inhibit control pin.

Figure 6. Simultaneous power-up waveforms from the circuit in Figure 5



To initiate the power-up sequence, the U1 Inhibit control must be held to ground as input power is applied, then held there for another 20 ms. This allows time for the auto-tracking module, U2 (PTH05010W), to complete its internal power-up. In this circuit the TPS3838K33, a nanopower supervisor IC (U3), is used both to detect the input voltage and to provide the required 20-ms time delay.

Figure 6 shows the power-up waveforms for the circuit in Figure 5. The combination of the capacitor C1 and the nanopower supply supervisor U3 delays the release of the ground signal to U1 until about 20 ms after the input source, V_{IN}, has been applied. Soon after its Inhibit control input rises, U1's output voltage rises to its set-point voltage. The rate at which the outputs rise is limited only by U1's internal soft-start circuit. This is about 0.65 V/ms, slow enough for the Auto-Track Sequencing units to follow.

As mentioned, power-down sequencing with Auto-Track Sequencing is subject to the same constraint as power-up. That is, a valid input voltage must be available to all modules controlled by the Track pin throughout the power-down sequence. This constraint makes it necessary for the power system to conduct a coordinated power shutdown for all circumstances, irrespective of whether the shutdown is initiated by a human operator or is the result of a line-voltage failure. In the latter case, there must be sufficient hold-up charge in the power system to allow time for a power-down sequence to be completed before any drop in the input voltage to the circuit occurs. The nanopower

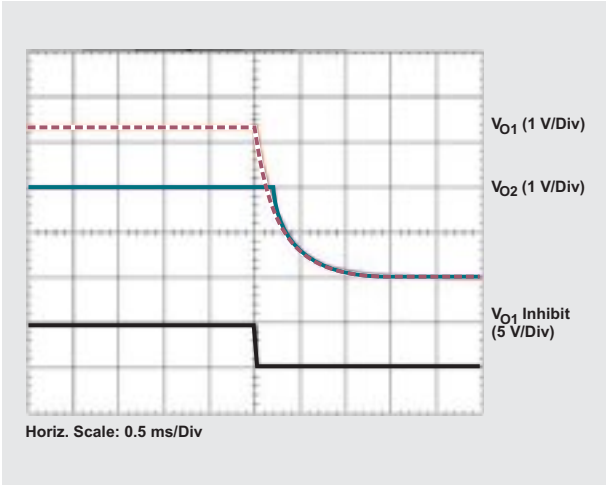
supervisor (U3) will turn off U1 (via the Inhibit pin) only after the input voltage has already begun to decay. Therefore, it cannot be used to initiate power-down; a separate transistor must be used. Q1 in Figure 5 is in parallel with U3 and can turn off U1 prior to any drop in the input voltage. When U1 (PT5801) is turned off, its output is tri-stated, which means it will neither source nor sink current from the load. This allows the output voltage to fall only as fast as the load discharges the output capacitors. Once the output voltage from U1 decays below U2's set-point voltage, it pulls down U2's output via its Track pin.

Figure 7 shows the output waveforms from the circuit in Figure 5 during power-down. To ensure that Auto-Track Sequencing can follow the output of another module, the voltage being followed must not change faster than Auto-Track Sequencing's slew-rate capability of 5 V/ms. During power-down, a decay rate faster than this will result in a delay before the lower-voltage outputs begin to follow the higher voltage, possibly producing an excessive voltage differential. The decay-rate limitation correlates to a minimum of 100 µF of capacitance per ampere of load current at the output of U1. In addition to having the highest output voltage, the module for U1 should be carefully selected to ensure that it does not sink current when turned off via its on/off Inhibit control.

Conclusion

Auto-Track Sequencing is a feature incorporated into select power modules in TI's Plug-in Power Solutions family. The feature makes it possible for the output voltage of these modules to be directly controlled (volt-for-volt) below their respective set-point voltages. This added flexibility allows a number of modules with different output voltages (for example, 3.3 V, 2.5 V, and 1.5 V) to be easily configured for simultaneous power-up and power-down voltage sequencing. Two examples of how Auto-Track Sequencing can be configured were discussed. The first showed how the Track control of a number of modules can be connected so that their output voltages rise in unison to their own internally generated RC ramp voltage. The second showed how the Track control of lower-voltage modules can be connected to directly follow the output of another higher-voltage module during both power-up and power-down transitions.

Figure 7. Simultaneous power-down waveforms from the circuit in Figure 5



References

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Document Title	TI Lit. #
1. Brian Rush, "Power-Supply Sequencing for Low-Voltage Processors," *EDN*, September 1, 2000.	—
2. David Daniels and Tom Fowler, "Dual Output Power Supply Sequencing for High Performance Processors"	slva117

Related Web sites

analog.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with PT5801, PTH05010W, PTH05020W or TPS3838K33

Soft-start circuits for LDO linear regulators

By Jeff Falin (Email: j-falin1@ti.com)
Applications, Portable Power

Many low-dropout (LDO) linear regulators do not have an integrated "soft-start" function that limits the in-rush current to the device being powered. In fact, as the simplified block diagram in Figure 1 shows, most linear regulators consist of only a reference, an error amplifier, and a pass element. Thus, at startup, the error amplifier senses that the output voltage is low and drives the pass element as hard as possible. The pass element pulls a large in-rush current to charge the output capacitance and/or load current abruptly, after a short delay. The delay is caused by three factors: the time required for the input voltage to rise above the undervoltage lockout circuitry, if any; the time required for the chip's internal circuitry, particularly the band-gap reference, to power up; and the time required for the regulator to sense its output voltage and turn on the pass element (i.e., the feedback loop bandwidth). The load resistance and the size of the regulator's output capacitance influence the start-up response. If the regulator starts up into a large capacitive or small resistive load, the in-rush current will be large, approaching the regulator's current limit in some cases. This article discusses two methods of slew-rate limiting a linear regulator's output-voltage rise time and, consequently, limiting its in-rush current at startup. The TPS795xx, high-PSRR, low-noise family of regulators, which were designed for approximately 50-µs start-up times and thus large start-up currents, are used as examples.

The simplest method uses a PMOS FET switch following the regulator output, in series with the regulator's load, as shown in Figure 2. Note that the switch must be placed after the regulator's minimum required output capacitance (i.e., C3) to ensure that the regulator remains stable. After the regulator turns on abruptly, FET Q1 operates as a crude supervisor and pulls R_T low. Capacitor C_T, effectively replacing the gate-to-drain capacitance of the FET, then causes the switch to function like an integrator and provides a more linear transition of the drain voltage.

Figure 1. Simplified block diagram of LDO linear regulator

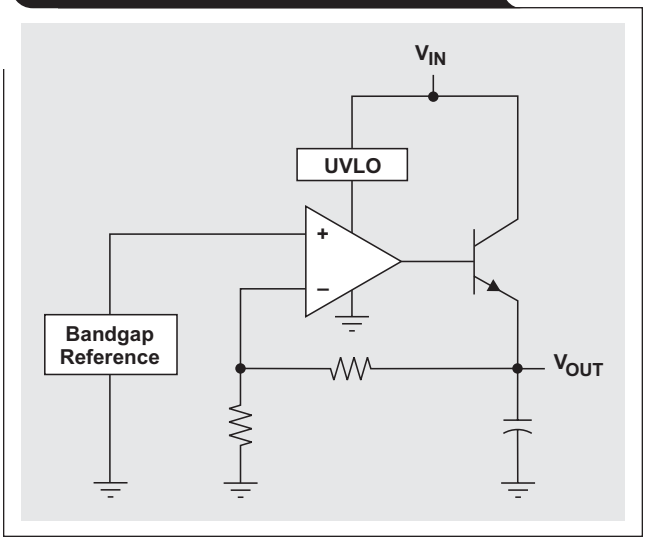
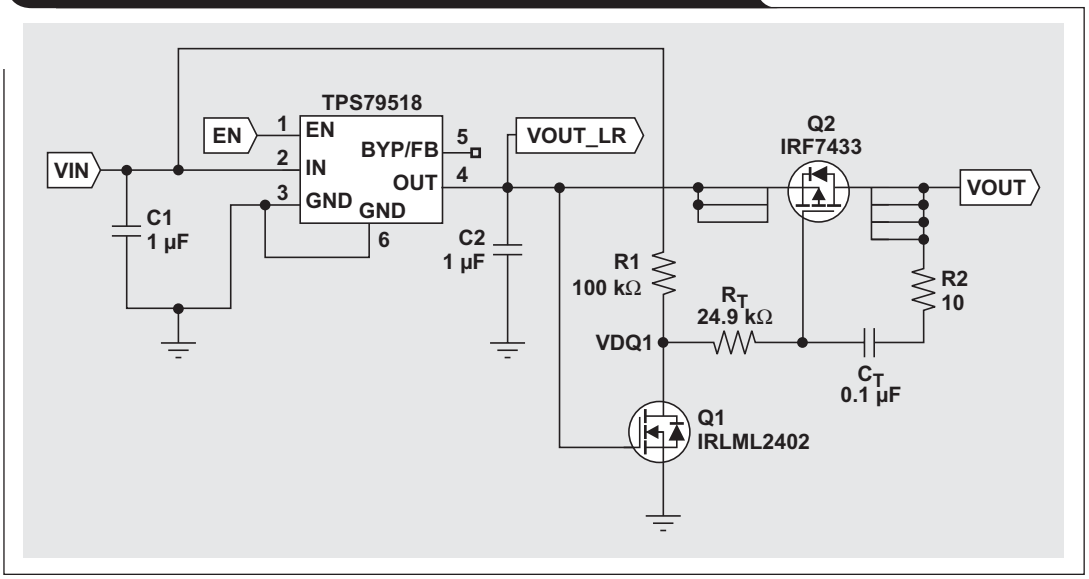


Figure 2. Soft start using a PMOS FET following the output



Careful component selection is critical for proper operation of the circuit. First, Q1 and Q2 must have threshold voltages that are lower than the desired output voltage (i.e., $V_{OUT} > V_{TH1,2}$). Second, Q2's $r_{DS(on)}$ must be small enough so that the drop across it due to the maximum dc load current does not significantly reduce the regulated output voltage. C_T is selected to be much larger than the gate-to-drain capacitance (i.e., $C_T >> C_{GD} = C_{rss}$). R_T is chosen according to the equation

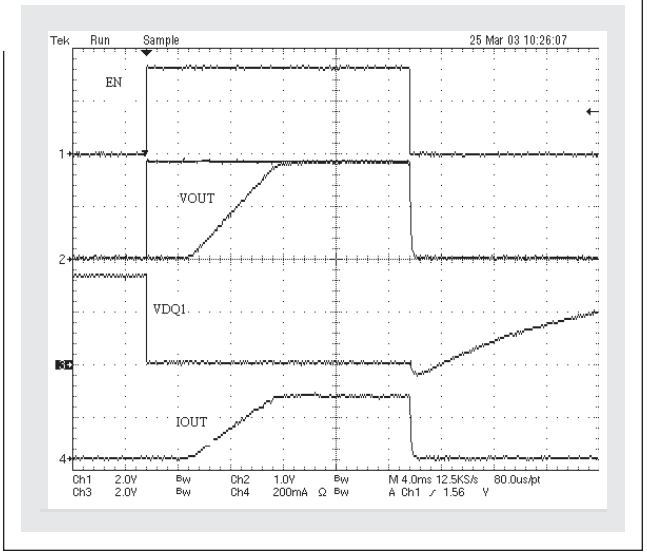
$$R_T = \frac{V_{OUT} - V_{TH}}{C_T \times \frac{V_{OUT}}{t_{Rise}}},$$

where t_{Rise} is the desired rise time (here 5 ms) and V_{TH} is Q2's threshold voltage (here 0.9 V). Resistor R1 is simply a large pull-up resistor. R2 should be selected to be much smaller than R_T.

Figure 3 shows the rise time of the regulator output voltage with and without the additional circuitry for V_{IN} = 3.3 V and I_{OUT} = 300 mA. The measured rise time is 6.5 ms, slightly larger than the designed 5 ms, but within an acceptable margin considering the variation in Q2's threshold voltage, V_{TH}. The 4-ms delay before startup is due to the RC time constant created by the PMOS FET's gate capacitances and R_T. With such a long start-up delay, the variation of threshold voltage of Q1, and thus the exact turn-on time of the switch, can be neglected.

The advantage of this method is its applicability to any regulator or dc/dc converter. The disadvantage is the difficulty in finding FETs either with low enough $r_{DS(on)}$ not to affect regulation under large load currents or with low enough threshold voltages for low output voltages. Another disadvantage is that this circuit does not work properly if V_{IN} is tied to EN. The IRF7433 has a maximum of 46-milliohm $r_{DS(on)}$ at V_{GS} = –1.8 V; so, at 300-mA output current, the output voltage could be 14 mV below the nominal voltage

Figure 3. Results from soft-start circuit using a PMOS FET following the output

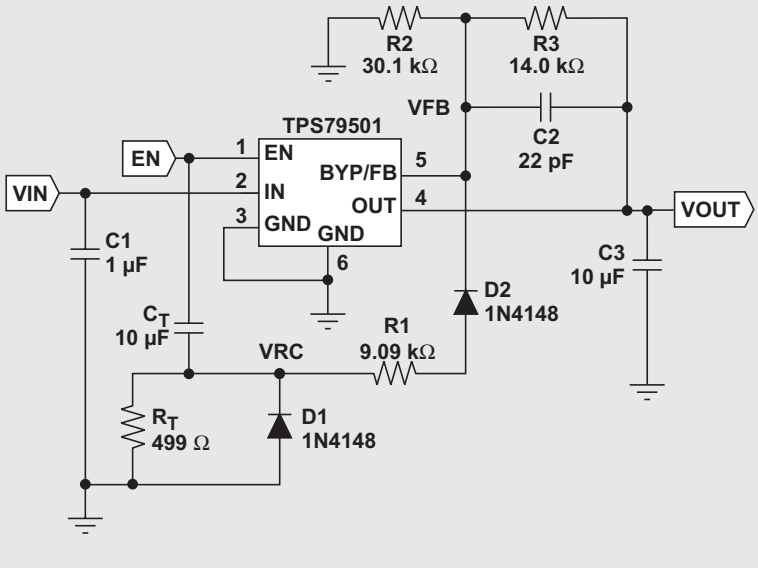


and thus could increase the lower tolerance limit of the regulator solution from –3 to –3.8%. In addition, to prevent large load transients from momentarily turning off the switch and causing the rail voltage to droop, a large output capacitor after the switch is recommended.

The second method uses an RC time constant and diode to shape the voltage that is being fed back from the output to the regulator at startup, as seen in Figure 4.

When the enable signal goes high, node V_{RC} charges to V_{EN}. With proper sizing of R1, the feedback node, V_{FB}, artificially rises above the regulated intended feedback voltage of 1.2 V to V_{FB2}. V_{FB2} is chosen to be at least

Figure 4. Soft-start circuit with RC and diode



200 mV above the intended feedback voltage but less than a diode drop below V_{EN}. Capacitor C_T then discharges through R_T and, as the feedback voltage drops, the pass element slowly turns on and the output voltage slowly rises. Diode D2 keeps R1 and R_T out of the feedback-voltage divider and therefore prevents any degradation in output-voltage tolerance during normal operation. Diode D1 clamps node V_{RC} to a diode drop below ground when EN is taken low.

The following equation is used to determine the appropriate size of R1 to raise node V_{FB} to V_{FB2}:

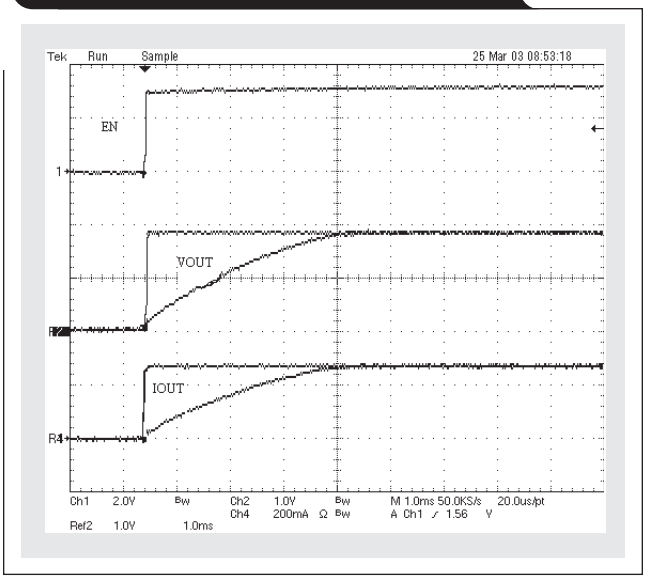
$$R1 = \frac{V_{IN(min)} - 0.6\ V - V_{FB2}}{\frac{V_{FB2}}{R2 \| R3}}$$

In this example, V_{FB2} is 1.2 V + 0.2 V = 1.4 V; and $V_{IN(min)}$ is 3.3 V, so the calculated value of R1 is 9 kΩ. Once R1 is determined, R_T is selected to be much smaller than R1 (roughly a factor of 10 or more) so that it will dominate the RC time constant; and then C_T can be sized to provide the appropriate rise time. In this example, the desired t_{Rise} is 5 ms for R_T = 499 Ω; and C_T = 10 µF is required.

Figure 5 shows the rise time of the regulator with and without the additional circuitry for V_{IN} = 3.3 V and I_{OUT} = 300 mA. The measured rise time is slightly below 4 ms.

The advantages of this method are simplicity, low cost, and isolation from the regulator after startup because of diode D2 and also because the control voltage is not a function of the output voltage. The primary disadvantages are that this circuit requires the use of an adjustable regulator and that it does not work with some regulators. Regulators with extra features, like an integrated SVS or a fast transient-assist circuitry, require the output of the regulator to be biased above ground after it is enabled. Using this soft-start method with such regulators could cause the start-up waveform to have an initial voltage spike before the slow rise to the output voltage.

Figure 5. Results from soft-start circuit using RC and diode



Either method limits the in-rush current, slowing the ramp time of the regulator output. The first method is best suited for higher-voltage rails with looser output-voltage tolerances and fewer transients. The second method provides the best performance, since the additional circuitry is effectively removed after startup and thus does not affect regulation; however, it will not work with all regulators.

Related Web sites

analog.ti.com
www.ti.com/sc/device/TPS79501
www.ti.com/sc/device/TPS79518

UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 1

By Michael O'Loughlin (Email: Michael_Oloughlin@ti.com)
Member, Applications Engineering Staff

Introduction

Power factor corrected (PFC) preregulators are generally used in offline ac/dc power converters with a power level higher than 75 W or to meet line harmonic requirements such as EN61000-3-2. PFC is typically done with a boost converter ac/dc topology due to the continuous input current that can be manipulated through average current-mode control to achieve a near-unity power factor (PF). However, due to the high output voltage of a boost converter, a second dc/dc converter is generally needed to step down the output to a usable voltage. In the past this has been accomplished with two pulse-width modulators (PWMs). One PWM controlled and regulated the PFC power stage, while the second was used to control the step-down converter. The UCC28517 controller reduces the need for two PWMs and combines both of these functions into one control-integrated circuit. The UCC28517 operates the second converter at twice the switching frequency of the PFC stage, which reduces the size of the boost magnetics and the ripple current in the boost capacitor. For more information on this device, please see Reference 7. This article reviews the design of a 100-W ac/dc power stage with power factor correction. A review of the second stage can be found in a future issue of TI's *Analog Applications Journal*.

Variable definitions

ΔI	Change in boost inductor current
$\eta 1$	Output A efficiency
$\eta 2$	Output B efficiency
C_{DIODE}	Boost diode capacitance
Comp	Dynamic range of the multiplier comp pin
C_{OSS}	FET drain-to-source capacitance
f_c	Voltage-loop crossover frequency
f_{line}	Input line frequency
f_p	Single-pole filter frequency
f_R	Ripple frequency
f_S	Minimum switching frequency
f_{SA}	Output A switching frequency
f_{SB}	Output B switching frequency
$G_{ID}(s)$	Power stage gain
G_{CA}	Current amplifier gain
$G_{c(s)}$	Control transfer function
$G_{co(s)}$	Control to output transfer function
g_m	Transconductance amplifier gain
G_{vea}	Voltage amplifier gain
$H_{(s)}$	Voltage divider gain
I_{IAC}	Multiplier input current
I_{MOUT}	Multiplier output
I_{PK}	Peak inductor current, peak diode current, peak switch current
I_{RMS}	RMS device current
I_{SS}	UCC28517 soft-start current of 10 µA
K	Constant typically equal to 1/V
P_{COND}	Device conduction losses
P_{COSS}	Power dissipated by the FET's drain-to-source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by the FET gate
P_{OUTA}	Output A maximum power
P_{OUTB}	Output B maximum power
P_{Q1}	Total FET losses
P_{semi}	Power dissipated by a semiconductor device
Q_{GATE}	FET gate charge
$R_{\theta cs}$	Thermal impedance case-to-sink
$R_{\theta jc}$	Thermal impedance junction-to-case
$R_{\theta sa}$	Thermal impedance sink-to-air
$R_{DS(on)}$	On resistance of the FET
R_{IAC}	Multiplier input resistance
R_{SENSE}	Current sense resistor
$s_{(f)}$	Frequency domain ($2\pi f$)
T_{amb}	Ambient temperature
t_{blank}	Amount of leading-edge blanking time
t_f	FET fall time
t_{holdup}	Boost capacitor hold-up time
T_{jmax}	Maximum semiconductor temperature
t_{on}	Boost inductor energizing on time
t_r	FET rise time
$T_{s(f)}$	Voltage loop frequency response
V_c	Control voltage
V_{CSENSE}	Maximum current sense voltage
V_{drop}	Amount of voltage the boost capacitor has to hold up
$V_{dynamic}$	Current sense voltage range
V_{ea}	Voltage amplifier output
V_f	Forward voltage of a diode
V_{GATE}	Gate-drive voltage
V_{IN}	RMS input voltage
V_{OUTA}	Boost output voltage
V_{OUTB}	Auxiliary output voltage
V_P	Oscillator ramp voltage
V_{pp}	Output peak-to-peak ripple voltage
V_{ripple}	Output B ripple voltage
V_{REF}	UCC28517 internal reference
V_{VFF}	Multiplier feed-forward voltage
Z_{OUT}	Compensation impedance

Table 1. Design specifications

	MAXIMUM	TYPICAL	MINIMUM
V_{IN}	265 V_{rms}		85 V_{rms}
Output A (V_{OUTA})	410 V	390 V	370 V
Output B (V_{OUTB})	12.6 V	12 V	11.4 V
Output A efficiency (η1)		85%	
Output B efficiency (η2)		50%	
P_{OUTA}	100 W		10 W
P_{OUTB}	8 W		4 W
Output ripple A (V_{pp})	12 V		
Output ripple B (V_{ripple})	750 mV		
Output A THD (% THD)	10%		
PF	1		
Output A switching frequency (f_{SA})		100 kHz	
Output B switching frequency (f_{SB})		200 kHz	

The following design example was generated using typical parameters rather than worst-case values. Please refer to Table 1 and Figures 1–3 for design specifications and component placement. All variables are defined in the sidebar on page 13.

PFC boost ac/dc regulator design (OUTA)

Inductor selection

The boost inductor is selected based on the maximum ripple current at the peak of minimum line voltage. The following equations can be used to calculate the required inductor for the boost power stage, assuming that the boost inductor ripple current is 25% of the maximum input current.

$$\Delta I = \frac{\frac{P_{OUTA} \times 0.25 \times \sqrt{2}}{\eta 1}}{V_{IN(min)}}$$

$$D = 1 - \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUTA}}$$

$$L1 = \frac{V_{IN(min)} \times \sqrt{2} \times D}{\Delta I \times f_{SA}}$$

Figure 1. PFC power stage schematic

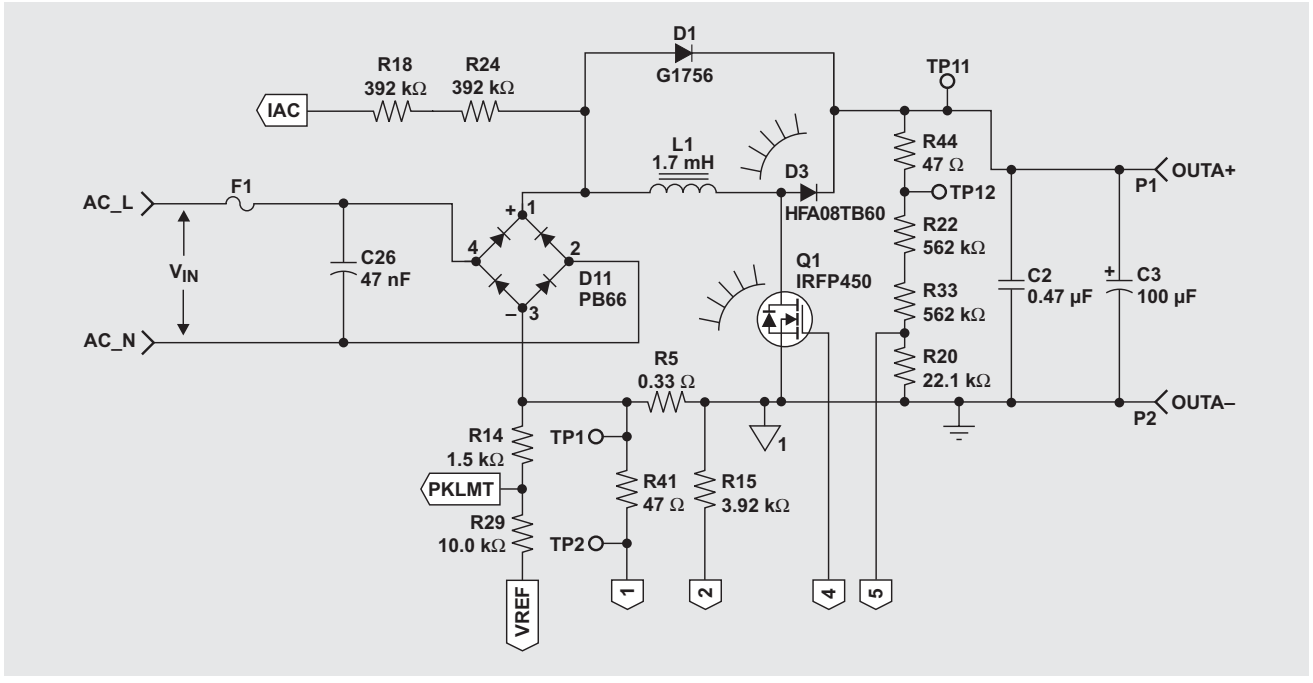


Figure 2. dc/dc power stage schematic

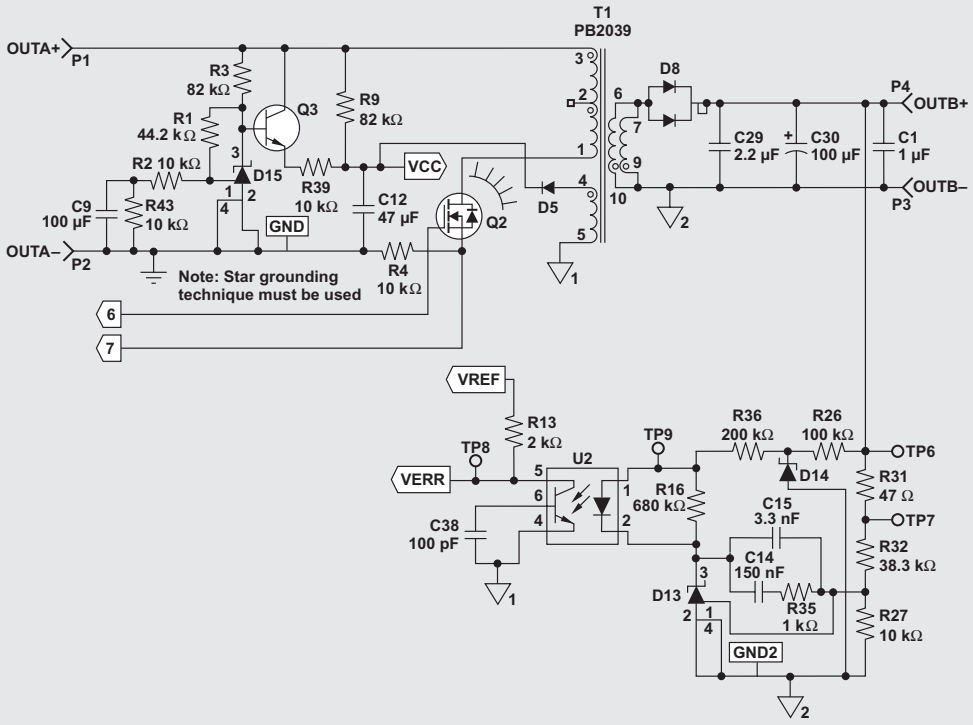
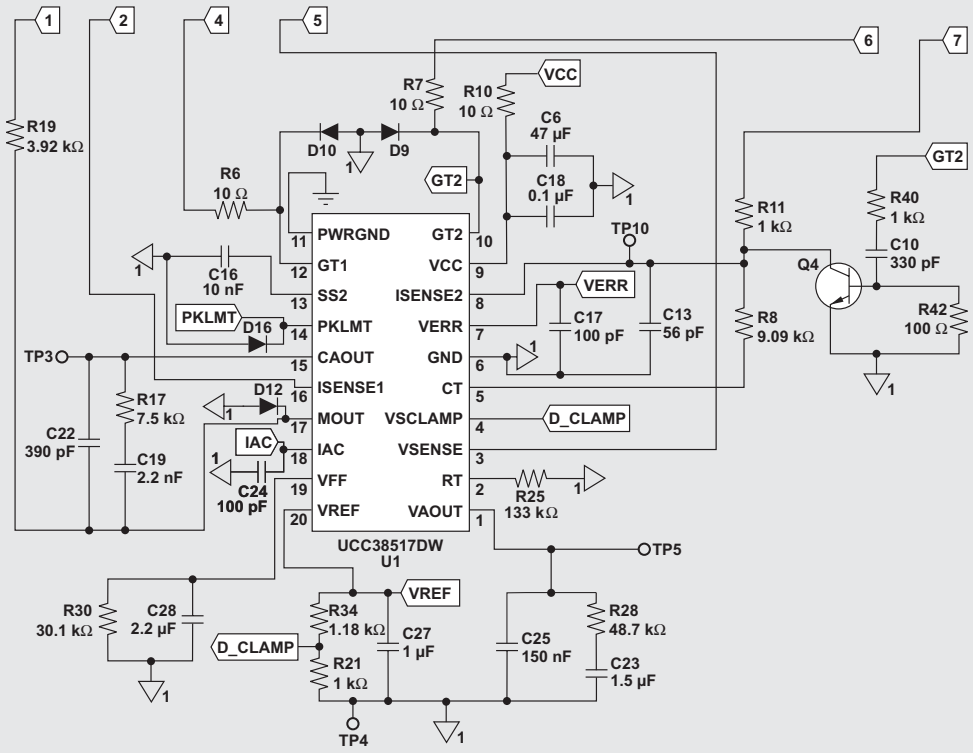


Figure 3. Controller schematic



The calculated inductance for this design was roughly 1.7 mH. To make the design process easier, Cooper Electronics designed the inductor (part number CTX08-14730).

Boost switch (Q1) and boost diode (D3) selection

To select Q1 and D3 properly, a power budget is generally set for these devices to maintain the desired efficiency goal. To meet the power budget for this design, an IRFP450 HEX FET and an HFA08TB60 fast-recovery diode from International Rectifier were chosen.

Equations used to calculate the loss in Q1 were:

$$I_{RMS\_FET} = \frac{P_{OUTA}}{\eta 1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{IN(min)}}{3\pi \times V_{OUTA}}}$$

$$I_{RMS\_L} = \frac{P_{OUTA} \times \sqrt{2}}{\eta 1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}}$$

$$P_{GATE} = Q_{GATE} V_{GATE} \times f_S$$

$$P_{COSS} = \frac{1}{2} C_{OSS} V_{OUTA(min)}^2 \times f_S$$

$$P_{COND\_FET} = R_{DS(on)} \times I_{RMS\_FET}^2$$

$$P_{FET\_TR} = \frac{1}{2} V_{OUTA} \times I_{RMS\_L} \times t_r \times f_S$$

$$P_{Q1} = P_{GATE} + P_{COSS} + P_{COND\_FET} + P_{FET\_TR}$$

$$I_{PK} = \frac{P_{OUTA} \times \sqrt{2}}{\eta 1 \times V_{IN(min)}}$$

$$I_{RMS\_DIODE} = \frac{P_{OUTA}}{\eta 1 \times V_{IN(min)}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times \sqrt{2} \times V_{IN(min)}}}$$

$$P_{COND\_DIODE} = V_f \times I_{RMS\_DIODE}^2$$

$$P_{DIODE\_CAP} = \frac{C_{DIODE}}{2} \times V_{OUTA}^2 \times f_{SA}$$

$$P_{DIODE} = P_{COND\_DIODE} + P_{DIODE\_CAP}$$

Heat sinks

The following equation can be used to calculate the minimum required thermal impedance of the heat sinks ($R_{\theta sa}$) for this design for Q1 and D3.

$$R_{\theta sa} = \frac{T_{jmax} - T_{amb} - P\_semi \times (R_{\theta cs} + R_{\theta jc})}{P\_semi}$$

The heat sink was designed to ensure that the junction temperature would not go above 75% of these devices' rated maximum with convection cooling, assuming a maximum ambient temperature of 60°C. The heat sink required for Q1 was an AVVID, part number 513201 B 0 25 00.

Output hold-up capacitor (C3) selection

The following equations were used to estimate the minimum hold-up capacitor (C3) size and the maximum allowable RMS current through the boost capacitor (I_{RMS_C3}).

$$C3 \geq 2 \times P_{OUTA} \times \frac{t_{holdup}}{V_{OUTA}^2 - (V_{OUTA} - V_{drop})^2}$$

$$I_{RMS\_C3} = \frac{P_{OUTA}}{V_{OUTA}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times V_{IN(min)} \times \sqrt{2}} - 1}$$

The hold-up capacitor was designed for 16.7 ms of hold-up time (t_{holdup}), allowing an output voltage drop (V_{drop}) of 85 V.

Peak-current limit for the boost power stage

Resistor dividers R14 and R29, along with current sense resistor R5, set up the peak-limit comparator of the UCC28517 that is used to protect the boost switch Q1 from excessive currents. This comparator should be set up so that it does not interfere with the boost converter's power limit or with the pulse-by-pulse current limiting of the step-down converters. For this design example, the flyback converter was designed to go into pulse-by-pulse current limiting at roughly 130% of maximum output power, and the power limit of the boost converter was set at 140% of the maximum output power. The peak-current limit for the boost stage was selected to engage at 150% of the maximum output power to ensure circuit stability.

The current sense resistor R5 was selected to operate over a 1-V dynamic range ($V_{dynamic}$) with the following equation.

$$R5 = R_{SENSE} = \frac{V_{dynamic}}{I_{PK} + 0.5 \times \Delta I}$$

The following equation can be used to size resistor R14 properly if R29 is first selected as a standard resistance value.

$$R14 = \frac{\left(\frac{P_{OUTA} \times 1.5 \times \sqrt{2}}{V_{IN(min)} \times \eta 1} + \Delta I\right) \times R5 \times R29}{V_{REF}}$$

Multiplier

The multiplier output of the UCC28517 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high-PF operation. As such, the proper functioning of the multiplier is key to the success of the design. The output of the multiplier, I_{MOUT}, can be expressed as

$$I_{MOUT} = I_{IAC} \frac{V_{ea(max)} - 1}{K \times V_{VFF}^2},$$

where K is a constant typically equal to 1/V.

The I_{IAC} signal is obtained through a high-value resistor (R_{IAC} = R18 + R24) connected between the rectified ac line and the IAC pin of the UCC28517. This resistor is sized to give the maximum I_{IAC} current at the highest expected line voltage. For the UCC28517 the maximum I_{IAC} current is about 500 µA. A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional; but noise can become an issue, especially during low line voltages, assuming a universal line operation of 85 to 265 Vac gives an R_{IAC} value of 750 kΩ. Because of voltage-rating constraints of standard ¼-W resistors, two or more lower-value resistors connected in series are needed to give roughly a 750-kΩ value and to distribute the high voltage across them.

The current through R_{IAC} is mirrored internally to the VFF pin, where it is filtered to produce a voltage feed-forward signal proportional to line voltage that is free of the 120-Hz ripple component. This second harmonic ripple component at the VFF pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial (see Reference 4). Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is

$$\frac{1.5\%}{66\%} \approx 0.022 \text{ (see Reference 5).}$$

A ripple frequency (f_R) of 120 Hz and an attenuation of 0.022 gives us a single-pole filter with

$$f_p = 120 \text{ Hz} \times 0.022 = 2.6 \text{ Hz}.$$

The voltage at the VFF pin not only supplies a voltage feed-forward signal but also activates input current fold-back when the V_{VFF} drops below 1.5 V. Please see Reference 2 for a detailed explanation of how these control ICs provide power limiting. The following equations were used to size resistor R30 and filter capacitor C20.

$$R30 = \frac{1.5 \text{ V}}{\frac{V_{IN(min)} \times 0.9}{(R18 + R24) \times 2}}$$

$$C20 = \frac{1}{2\pi \times 30 \text{ k}\Omega \times 2.6 \text{ Hz}}$$

This results in a single-pole filter, which adequately attenuates the harmonic distortion and provides power limiting.

The multiplier's output resistor R19 is sized to match the maximum current through the sense resistor (R5) to the maximum multiplier current. R15 is sized to balance the offset current in the current amplifier and needs to be set to the same value as R19. The following equations were used to size R15 and R19.

$$I_{MOUT(max)} = \frac{I_{IAC}@V_{IN(min)} \times (V_{ea(max)} - 1\text{ V})}{K \times V_{VFF}^2}$$

$$R19 = R15 = \frac{V_{dynamic}}{I_{MOUT(max)}}$$

Current loop compensation for the boost converter

The following equation defines the gain of the power stage, where V_P is the maximum voltage swing of the UCC28517 oscillator ramp, roughly 5 V.

$$G_{ID}(s) = \frac{V_{OUTA} \times R5}{s \times L1 \times V_P}$$

To have a good dynamic response, the crossover frequency of the current loop was set to 1/10 the switching frequency. This can be achieved by setting the gain of the current amplifier (G_{CA}) to the inverse of the current loop power-stage gain at the crossover frequency. For this design the current amplifier required a gain of 2.581 at 10 kHz. The following equations were used to compensate the current amplifier of the boost power stage.

$$G_{CA} = \frac{1}{G_{ID}(s)} = 2.581$$

$$R17 = G_{CA} \times R19$$

$$C19 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{10}}$$

$$C22 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{2}}$$

Voltage loop compensation for the boost converter

Figure 4 shows the small-signal-control block diagram for this application. The following equations describe small-signal gain as well as the voltage loop frequency response, $T_{s(f)}$.

$$H_{(s)} = \frac{R20}{R20 + R32 + R32}$$

$$G_{c(s)} = g_m \times \frac{s_{(f)} \times R28 \times C23 + 1}{s_{(f)} \times (C23 + C25) \times \left(\frac{s_{(f)} \times C23 \times C25}{C23 + 25} + 1 \right)}$$

$$G_{co(s)} = \frac{\Delta V_{OUTA}}{\Delta V_c} = \frac{P_{OUTA}}{V_{ea(max)} \times s \times V_{OUTA} \times C3}$$

$$T_{s(f)} = -H_{(s)} \times G_{c(s)} \times G_{co(s)}$$

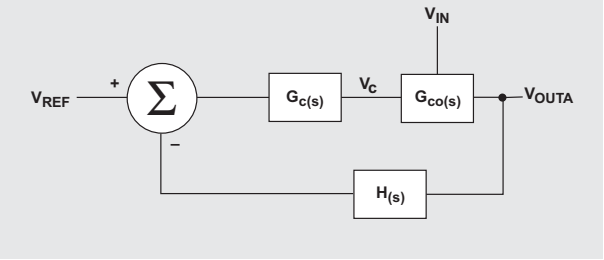
To reduce third-harmonic distortion, the voltage loop typically crosses over at roughly 10 to 12 Hz. For this design, the voltage-loop crossover frequency (f_c) was selected to be roughly 10 Hz. The following equations were used to select the components to compensate the voltage loop, $T_{s(f)}$, to cross over at the desired f_c with 45 degrees of phase margin.

$$R28 = 2\pi \times V_{ea(max)} \times f_c \times C3 \times \frac{V_{OUTA} \times \eta 1}{g_m \times P_{OUTA} \times H_{(s)}}$$

$$C23 = \frac{1}{2\pi \times R28 \times f_c}$$

C25 was selected to attenuate the 120-Hz output ripple voltage (V_{pp}) to 1.5% (% THD) of the voltage amplifier's dynamic output range.

Figure 4. dc/dc converter control loop



$$V_{pp} = \frac{P_{OUTA}}{\pi \times 120\,Hz \times C3 \times V_{OUTA}}$$

$$G_{vea} = \frac{\%\,THD \times V_{ea(max)}}{V_{pp} \times 100}$$

$$Z_{OUT} = \frac{G_{vea}}{H_{(s)} \times g_m}$$

$$C25 = \frac{1}{2\pi \times Z_{OUT}}$$

After the design was complete, the frequency response of the voltage loop, $T_{s(f)}$, was measured with a network analyzer; and the results are shown in Figure 5. It can be observed that f_c was roughly 8 Hz with a phase margin of roughly 50 degrees.

Figure 5. Frequency response of power stage A

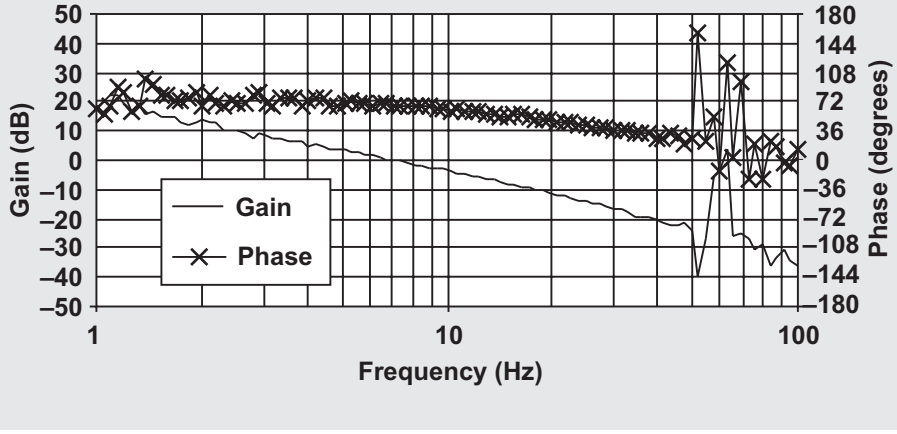


Figure 6. Output A THD vs. output power

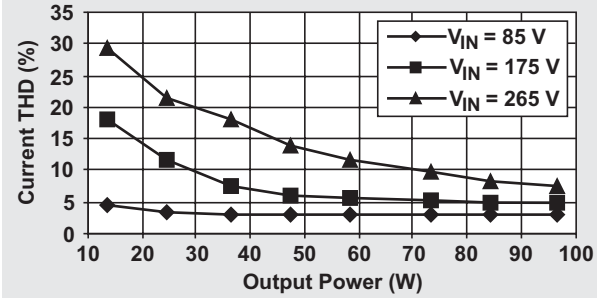


Figure 7. Output A efficiency vs. output power

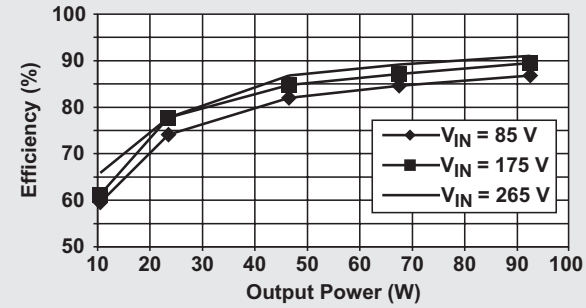


Figure 8. Output A PF vs. output power

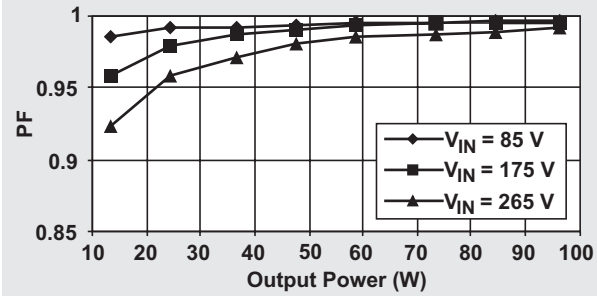
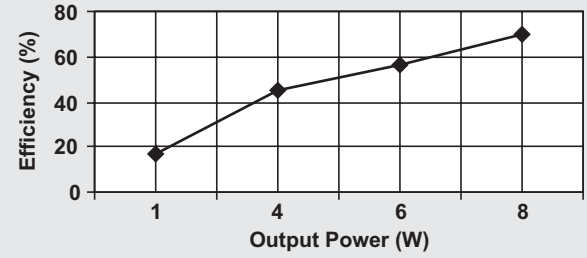


Figure 9. Output B efficiency vs. output efficiency



Summary

This article reviewed the design of a 100-W PFC ac/dc preregulator, which is the first stage in a two-stage power converter. The UCC2851X family of combination PWM controllers is perfect for offline applications that require PFC and auxiliary power supplies to meet different system requirements. The performance of this two-stage power converter is shown in Figures 6–9.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Laszlo Balogh, "Design Review: 140W, Multiple Output High Density DC/DC Converter," p. 6-9	slup117
2. Laszlo Balogh, "Unitrode – UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends," Unitrode Design Note	slua196
3. Lloyd Dixon, "Control Loop Cookbook," p. 5-17	slup113
4. Lloyd Dixon, "Optimizing the Design of a High Power Factor Switching Preregulator," pp. 7-11–7-12	slup093
5. James P. Noon, "A 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions," pp. 1-11–1-14	slup106
6. "Practical Considerations in Current Mode Power Supplies," Unitrode Application Note	slua110
7. "Advanced PFC/PWM Combination Controllers," Data Sheet	slus517
8. "UCC28517 Prototype Reference Design Module," Reference Design	sluu117

Related Web sites

analog.ti.com
www.ti.com/sc/device/TL431
www.ti.com/sc/device/UCC28517

Video switcher using high-speed op amps

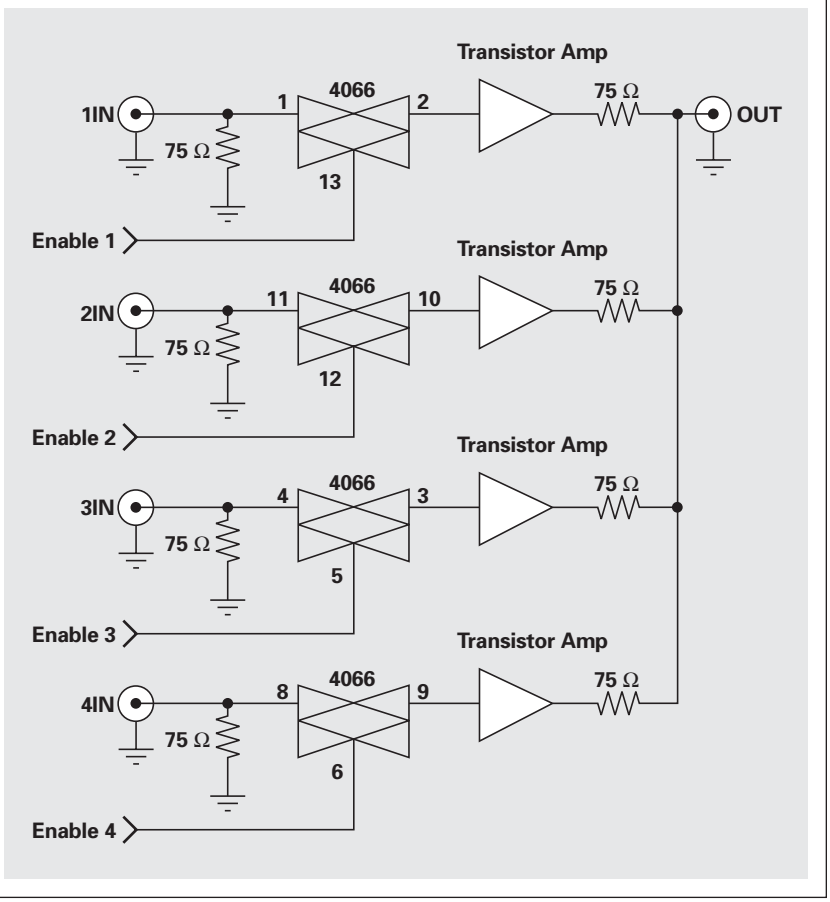
By Bruce Carter (Email: r-carter5@ti.com)
Advanced Linear Products, Op Amp Applications

Introduction

Video switching devices are used to route video from several sources to a single channel.

Low-end consumer products use CMOS analog switches and multiplexers such as the 4066 and 4051, as shown in Figure 1. These devices have a series on resistance that ranges from just over a 100 Ω to 1 kΩ, a resistance that is not constant with video level. Unfortunately, this resistance appears in series with the signal. When combined with the 75-Ω load in the monitor, the analog switch would form a voltage divider, disastrously affecting the luminance. Consumer devices solve this problem by buffering the analog switch outputs with transistor stages. This results in video performance degraded not only by the characteristics of the CMOS switch but by those of the buffer stage as well. There should be a better way—and there is!

Figure 1. Traditional video switching solution



Video op amps with power-down inputs

Let's forget the switching action for a moment and consider just the buffer amplifier function. A transistor stage is problematic because it has several interrelated requirements. It must present high input impedance to the switch—high enough that a 1-kΩ switch resistance is inconsequential, and high enough that variation in resistance of the switch with IRE level does not produce luminance shifts. The stage has to operate with almost zero ripple and phase shift over a 6-MHz bandwidth (which translates to a very wide bandwidth stage). The transistor also has to provide enough drive for a 150-Ω load. These are tough requirements for a single transistor! Many high-end video multiplexer designs, therefore, use a FET for high input impedance and a bipolar transistor for drive.

An op amp has a lot of advantages in this application. High-speed op amps exist that have plenty of bandwidth for video applications. If an op amp with 20 or more times the video bandwidth is used, roll-off and phase shift at 6 MHz are negligible. An op amp has high input impedance, particularly in the noninverting mode. It can be terminated for 75-Ω input by a simple resistor. Two resistors create a gain of 2 in the noninverting configuration, which compensates for a 75-Ω back termination resistor on the op amp output. Overall stage gain is therefore 1.

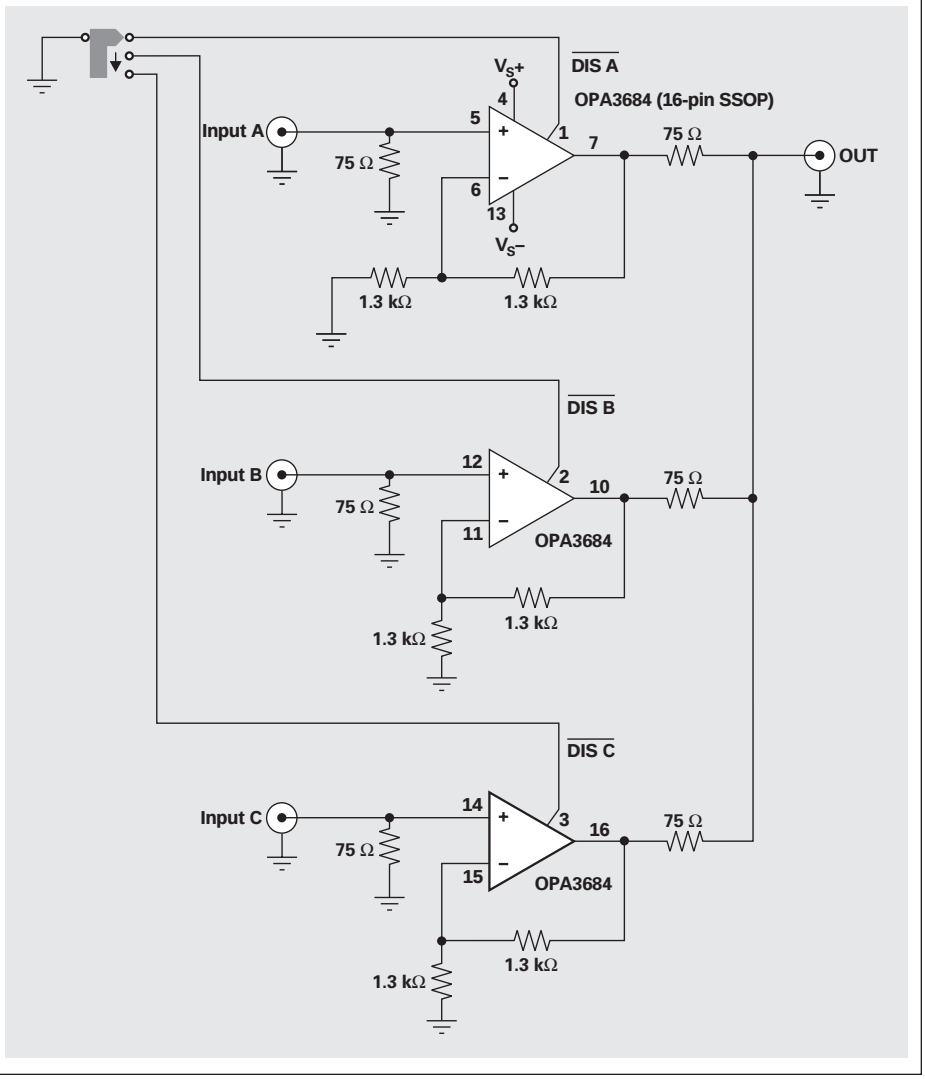
Some new video op amps have a power-down feature that allows the output of the op amp to be disabled, producing a 0-V (0-IRE—"blacker than black") level on its output. It can therefore be connected in parallel with other op amps, because it will contribute no luminance or sync pulses. In power-down mode, its gain-setting resistors appear as a slight load on other op amps. Because the resistors have a relatively high value, they increase the load on other op amps by a negligible amount. The other op amps merely have to have enough excess drive capability

to drive the extra load. This enables the op amp to operate as a video switch, as shown in Figure 2.

Figure 2 shows a 3:1 switcher using the OPA3684. More OPA3684 stages can be connected to add additional inputs. If only two inputs are needed, the THS4226 can be used. The limit on the number of inputs has not been tested; but the only limiting factors appear to be the additional loading on the active op amp output, the physical size of the interface, and the length of connections.

The switcher in Figure 2 shows a three-position, single-pole rotary switch—which, in practical applications, should be a "break before make" type. It can also be an electronic switching system, perhaps with an intelligent infrared interface in a consumer unit.

Figure 2. Video switcher with high-speed op amps



Tests of the video switcher

The following describes testing of a 2:1 video switcher based on the THS4226. The primary areas of concern are:

- *crosstalk*, which is the bleeding of images from inactive channels into the active channel;
- *offset errors*, which will cause a change in luminance (white and black levels);
- *gain errors*, which will expand or contract the visible 7.5- to 100-IRE portion of the video waveform; and
- *phase errors*, which will change the shades of color in the video.

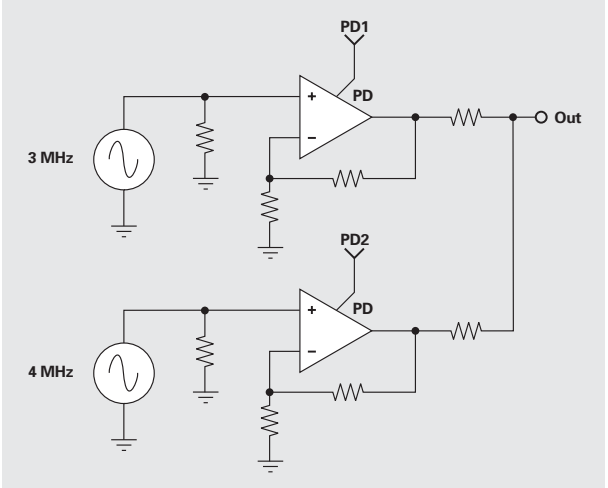
While crosstalk can be measured with conventional test equipment, the rest of the tests were performed by utilizing the Lucasfilm THX test patterns[1] (available on several consumer DVD titles). These test patterns were used on one video input, while a high-quality NTSC program source was used on another input. Although these tests were admittedly subjective, the human eye is very sensitive to shifts in brightness and color when side-by-side comparisons are made.

Crosstalk test

In the test setup in Figure 3, sinusoidal sources are input to the two channels, with 3 MHz input to one channel and 4 MHz to the other. The output is connected to a spectrum analyzer. The level of 3 MHz in the output when it is the inactive channel, and vice versa, determines how much crosstalk there will be in the video.

The level of crosstalk was close to the noise floor of the spectrum analyzer. The best estimate after 1000 samples were taken was that the crosstalk from each inactive channel was about –74 dB, referenced to the active channel.

Figure 3. Crosstalk test



Contrast/picture test

The contrast/picture test shown in Figure 4 is a 100-IRE rectangle centered on a 0-IRE background. For proper operation, the background should appear completely black and the rectangle completely white, with no "bleeding" or "blooming" of the rectangle into the background.

When the contrast/picture test was run through the video multiplexer as the active source, black and white levels were unaffected by the presence of the op amp as a buffer. No bleeding or blooming occurred.

When the contrast/picture test was on the inactive input and program material was on the active input, any crosstalk would have resulted in a visible brightening of the center of the picture. None was observed.

Brightness setup test

The brightness setup test pattern is shown in Figure 5. Although the right-hand side of the test pattern appears interesting, the area of interest is actually the portion on the left-hand side. Printed copies of this article almost certainly will not show anything there. On the left-hand side of the test pattern, there are two faint vertical bars—one lighter and one darker than the background. The black level is defined as 7.5 IRE, to which the background is set. The darker vertical bar is set at 11.5 IRE (slightly higher than the black level), and the lighter one is set at 3.5 IRE (slightly lower than the black level). This test pattern, called the "PLUGE bars," is used to test the black level. Correct setting of the brightness level will allow the darker bar to be visible, but not the lighter one (because it is below the black level). Any shift in the black level due to gain-setting resistors would therefore be evident.

Please note that the purpose of this article is to describe tests performed on the video multiplexer—*not* to provide a test pattern for the adjustment of your monitor. The computer monitor on which this document is displayed is not an NTSC monitor. Colors may not display correctly in PDF format, and the color depth of the display also will affect the colors seen.

The brightness level was set without the video multiplexer being in the circuit. Then the video buffer was inserted into the signal path. No change in brightness level was observed.

The brightness setup test is also an ideal way to test for crosstalk between two video channels. Crosstalk would show up on the black background as a "ghost" image of the program material on the inactive channel. None was observed.

Tint and color setup using SMPTE color bars

The SMPTE color bars shown in Figure 6 have long been used in the television industry to test proper color reproduction. Their primary use here is to test for differential phase changes (and therefore color changes) in the video multiplexer.

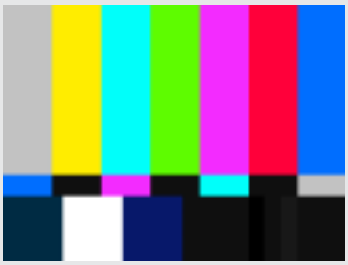
The SMPTE bars were observed with and without the video multiplexer in the signal chain. No color shifts were observed. Although no blue filter was available to monitor the precise tint and color settings, the red color bar did not tend to bloom or get "snowy"—a sure sign that the color portion of the signal was not being significantly affected.

The color bar patterns would also produce color shifts in the other channel if crosstalk was a factor. Any broadcast technician will confirm that human skin is the toughest color to get right—and any change in skin tone due to color crosstalk will be very apparent.

Figure 4. Contrast/picture test pattern

Figure 5. Brightness setup test

Figure 6. SMPTE color bars



Conclusion

Video op amps with power-down inputs are ideal for constructing video multiplexers and switches. They improve performance by replacing problematic analog switches and transistor amplifier buffer stages. They also lower component count, raising reliability.

Reference

1. Lucasfilm THX Consumer Products: www.thx.com/mod/techLib/index.html

Related Web sites

analog.ti.com
www.ti.com/sc/device/THS4226
www.ti.com/sc/device/OPA3684

Expanding the usability of current-feedback amplifiers

By Randy Stephens (Email: r-stephens@ti.com)
Systems Specialist, Member Group Technical Staff

Introduction

Although current-feedback (CFB) amplifiers have been around as long as the widely utilized voltage-feedback (VFB) amplifiers, their acceptance has been sporadic. One of the reasons for this is quite simple—they have a different name and therefore must be difficult and very hard to use. This is simply not true. There are numerous papers[1, 2, 3] comparing the differences between the two amplifier types that show they are more similar to each other than different. In fact, for numerous circuits, a CFB amplifier may actually yield better results due to its inherent slew-rate advantage, lack of a gain-bandwidth product, and reasonably low noise for the performance.

Almost every paper written about CFB amplifiers cautions readers that placing a capacitor directly in the feedback path, without any resistance in series, will cause the CFB amplifier to oscillate. This is true, as the compensation of the amplifier is tied directly to the feedback impedance. Since a capacitor has low impedance at high frequencies, this essentially places a short in the feedback path that inadvertently defeats amplifier compensation, resulting in instability.

Because of this limitation, there are a handful of common circuits that are not recommended for use with a CFB amplifier. These include integrators, some types of filters, and special feedback-compensation techniques. But what if there was a way to make these circuits work? And what if the solution was as simple as adding a single component? This would make it feasible to implement a CFB amplifier for just about every application for which a VFB amplifier could be used, with the benefits of the CFB amplifier.

Compensation

This article does not explain the compensation theory of VFB and CFB amplifiers, as there are many papers written on this topic. The only thing that is important is that there must be resistance, or impedance, in the feedback path at the open-loop intersection point to make the CFB amplifier stable.

Figure 1 shows a traditional VFB amplifier, a THS4012, configured in a noninverting gain of +5 with a simple low-pass gain filter set at approximately 1 MHz by the straightforward $1/(2\pi R_F C_F)$ formula.

If a CFB amplifier like the THS3112 is simply dropped into this circuit, it *will* oscillate and the circuit will become useless. A method of compensating the CFB amplifier in this circuit is to insert a resistance, or impedance (Z), in the feedback path as shown in Figure 2.

It can easily be seen that regardless of the impedance of the feedback path represented by R_F and C_F, the impedance Z is in the amplifier's feedback loop dictating the compensation of the amplifier. The interesting thing about this configuration is that the feedback resistance (R_F), which normally dictates the compensation of the amplifier, can now be essentially any resistance desired. The reader should keep in mind that this is still a high-speed amplifier with speeds over 100 MHz; so the feedback resistance should always be kept less than a few kilohms to minimize the effects of parasitic capacitances on the overall circuit. Conversely, minimizing the resistance too much will place too much of a load on the amplifier, typically degrading performance.

One of the drawbacks of adding the impedance Z in this manner is that the summing node at the inverting terminal is now separated from the virtual summing node. This can

Figure 1. VFB test circuit

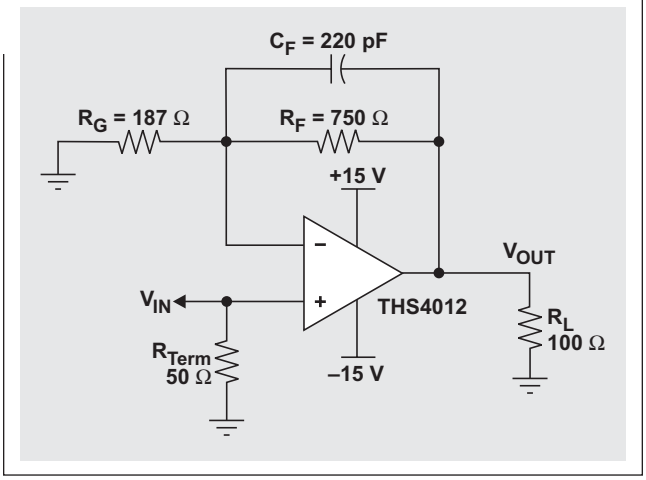
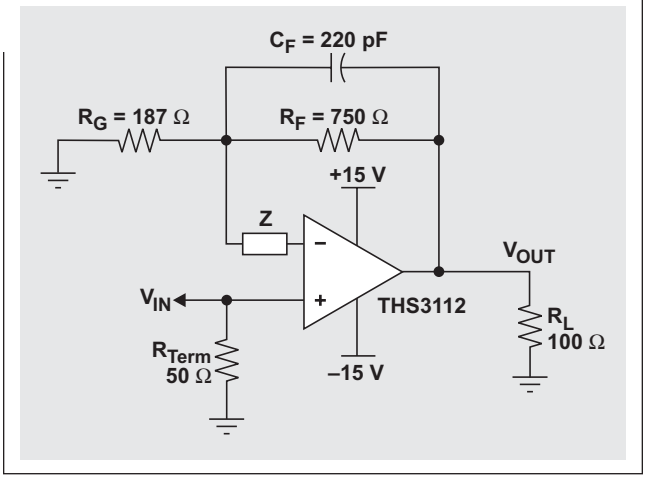


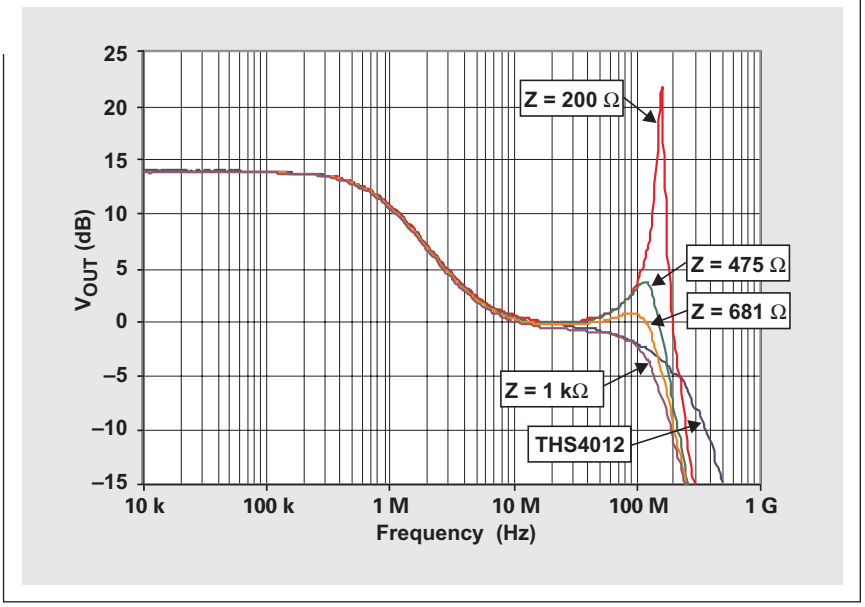
Figure 2. CFB test circuit with simple modification



introduce errors into the system due to the bias current and the dynamic signal current flowing through this impedance; but these effects are reasonably small as long as the impedance is minimized.

Adding impedance Z can affect input offset voltage due to the dc input bias current, which is typically 1 to 10 µA, multiplied by the impedance Z. This resulting voltage gets multiplied by the noise gain of the circuit. Additionally, when a signal appears at the output, the CFB amplifier (as the name implies) relies on an error current flowing through the inverting node through the impedance Z, producing a signal error. However, since the transimpedance of most CFB amplifiers is well over 100 kΩ and sometimes as high as several megohms, this error is also minimized if the impedance is kept low. The drift of this circuit now also relies on the temperature characteristics of impedance Z and should not be used as a precision amplifier; but most CFB amplifiers are not used as precision amplifiers anyway due to their inherent topology limitations. Overall, these issues are minimal and, for most systems, can be effectively ignored in favor of the CFB amplifier's advantages as previously stated.

Figure 3. Frequency responses with resistors (gain = +5)



Testing with different Z values

The easiest way to see if the circuit is stable is to use a network analyzer frequency sweep. Instability can typically be seen as sharp rises in the frequency response at the amplifier's bandwidth limitations. If the peaking is smooth, or there is no peak, then the amplifier should be stable. Figure 3 shows the frequency response of the system with different values of resistors for the variable Z.

The response of the THS4012 is also shown for reference to easily compare the performance of the two systems. It is interesting that no matter what resistance is used for Z, the responses below 20 MHz look identical to each other. This is the ultimate goal of this configuration—no differences in signal performance. For the stability part of the circuit, the area above 20 MHz must be examined.

Examining the circuits in Figures 1 and 2 shows us that the feedback impedance is dictated by the capacitor CF. Above 20 MHz, this impedance is very small—essentially creating a short from the output to the summing node. This configuration is commonly referred to as a unity buffer with the signal gain set to 1. The data sheet for the THS3112[4] recommends that, in a gain of +1 under the circuit conditions utilized, the feedback resistance be 1 kΩ. Thus, it is no surprise to see that when Z = 1 kΩ, the response looks very smooth and well behaved, indicating a very stable system. However, when Z = 681 Ω, the response also looks very reasonable and helps minimize the potential issues stated previously. This shows that there is a reasonably wide range of acceptable values for Z and does not imply that the selection for Z is highly critical. Figure 3 also illustrates a common trait for current-feedback amplifiers—as the feedback impedance is decreased, the peaking will increase. If the impedance is too low, there is a good chance that the circuit will become unstable and oscillate, as illustrated by the response when Z = 200 Ω.

Output noise

One element that may be very important in a system is the output noise. Adding a resistance in the manner discussed only makes the output noise worse. The inverting current noise of the amplifier goes through the resistance at Z and creates a voltage noise. This noise then becomes multiplied by the circuit's gain, which is frequency-dependent.

For a CFB amplifier, the inverting current noise is typically the highest noise component of the amplifier. Although the CFB amplifier voltage noise is inherently very low, typically less than 3 nV/$\sqrt{\text{Hz}}$, the inverting current noise of most CFB amplifiers is generally around 15 to 20 pA/$\sqrt{\text{Hz}}$. The noninverting current noise is only noticeable if the source impedance is high. Using a 50-Ω environment minimizes the noninverting current noise.

The THS3112 was designed to have very low noise. The voltage noise is 2.2 nV/$\sqrt{\text{Hz}}$, the noninverting current noise is 2.9 pA/$\sqrt{\text{Hz}}$, and the critical inverting current noise is a low 10.8 pA/$\sqrt{\text{Hz}}$. However, multiplying the inverting current noise by 1 kΩ and then multiplying by the gain can alone produce a very substantial output noise of about 54 nV/$\sqrt{\text{Hz}}$ in the pass band. To quantify the output noise of the system, the circuits shown in Figures 1 and 2 were tested for output

noise (see Figure 4). For comparison, the THS4012, with a respectable voltage noise of 7.5 nV/$\sqrt{\text{Hz}}$ and both current noises of 1 pA/$\sqrt{\text{Hz}}$, is also shown in Figure 4.

Note that the output noise of the THS4012 is the same as when using the THS3112 with Z = 475 Ω. Again, these responses are just like those of a VFB amplifier in the traditional configuration, showing that the basic functionality is sound—there are no differences between a VFB amplifier and this configuration. Figure 4 shows that although using Z = 1 kΩ produces a very stable amplifier, the output noise is 20 nV/$\sqrt{\text{Hz}}$ higher than that of the THS4012.

Figure 4. Output noise (gain = +5)

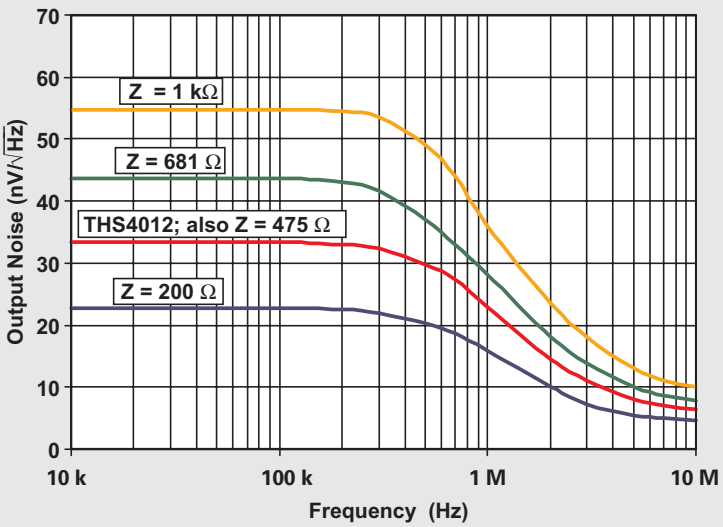
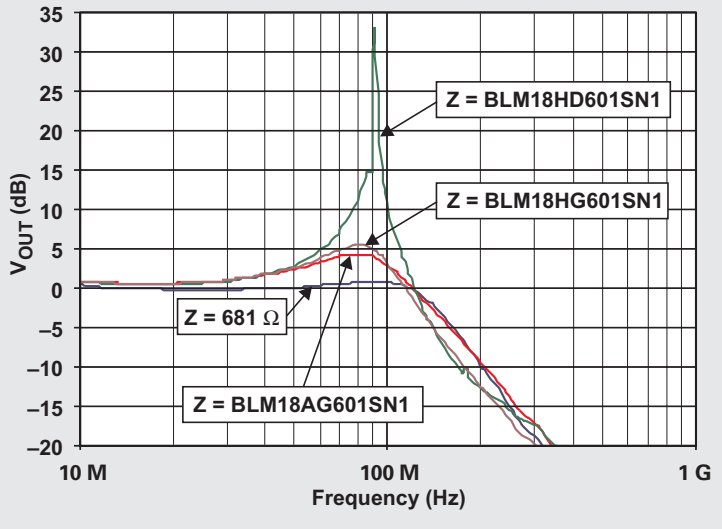


Figure 5. Frequency responses above 10 MHz with ferrite chips (gain = +5)



Keep in mind that the THS3112 has very low overall noise but that many other CFB amplifiers will probably produce much higher noise. The only way to get around this is if the unity-gain stability of the amplifier requires a very small resistor of, say, only 500 Ω or less. But what if there was another way to make the CFB amplifier stable *and* have low noise at the same time?

Fundamentally speaking, the circuit needs high impedance within the feedback path only at the amplifier's bandwidth limit. At frequencies below this point, it really does not matter what the impedance is, and the amplifier will work fine. The issues stated previously are also minimized, resulting in an even better system than one using pure resistors.

The first solution that comes to mind is to use an inductor. Inductors have low impedance at low frequencies and high impedance at high frequencies—exactly what is desired; but their relatively large size and high cost are generally considered prohibitive. An alternative component that minimizes these disadvantages and still functions the same is the ferrite chip.

Testing with ferrite chips used for Z

Ferrite chips have been available for several years, are relatively low-cost, and are available in very small sizes—0402 and larger. Although several manufacturers produce ferrite chips, testing was done with what was available in the test lab—ferrite chips from Murata's BLM series. Examining the impedance characteristics of these ferrites revealed several possible components that could be utilized.

The first factor in determining the proper component was the ferrite's impedance at the amplifier's bandwidth limit. For the THS3112, this implied an impedance of at least 600 Ω at about 150 MHz to meet stability. This can vary, as the first test results showed (see Figure 3).

Additionally, the Q of the ferrite chips varies from grade to grade. Some have a low Q with a fairly smooth rise to the resonance point that then subsides due to inherent properties and parasitics, while other chips have a relatively high Q with a sharp rise and fall in impedance associated with them. Although either style may meet the impedance requirements, testing was required to see if this Q had an effect on the circuit. Again, the best way to show the results was to graph the frequency response of the system, as shown in Figure 5. The responses below 10 MHz were all identical to the original configuration. This figure concentrates on the stability portion of the responses above 10 MHz. For comparison purposes, the 681-Ω, pure-resistance response is shown.

Although all of these ferrite chips have the same impedance at 100 MHz (600 Ω), they produced different results. The HD series high-Q chip shows a very narrow and large peak that will most likely result in instability and oscillations. The AG and HG series low-Q chips both performed about the same, and either one would probably produce acceptable results. The only difference is that the HG series has impedance at higher frequencies and would probably be better suited for use with very high-speed CFB amplifiers such as the OPA685 or the THS3202.

Notice that the pure resistance has a lower response peak than the ferrite chips. Coupled with the fact that the HD series has a high Q and a high peak, this implies that the slope of the impedance at the amplifier's bandwidth is a factor for stability. This makes a lot of sense; as it is well known that for any amplifier, if a zero intersects the amplifier's open-loop response at a rate of closure of 40 dB/decade, large peaking and oscillations will most likely result.[5] For this circuit configuration, if the impedance of Z has a large slope that intersects the transimpedance curve at essentially a rate of closure of 40 dB/decade, peaking and oscillations also will most likely occur. By comparison, a resistor intersects the transimpedance curve at a rate of closure of 20 dB/decade, resulting in a stable response. Even though the low-Q ferrite beads have some slope related to their impedance, the rate of closure is much lower than 40 dB/decade, providing improved stability. Nevertheless, minimizing this intersection rate of closure as much as possible should produce acceptable results.

To further expand on the usefulness of the ferrite chips, more testing was done utilizing the AG series in the circuit, as shown in Figure 6.

This figure shows that, just like the results for the pure resistor, the higher the impedance is, the lower the peaking.

How does this affect the output noise of the system? Figure 7 shows the output noise when the ferrite chips were used, along with the output noise of the THS4012 and some of the original resistor configurations.

As expected, due to the low frequency impedance of the ferrite chips, the noise is extremely low. This noise was the same regardless of which ferrite was used. If noise above 10 MHz was important, the impedance of these ferrite chips would start to increase the output noise to the same extent as resistors. These tests show that there are several advantages of using ferrite chips over resistors.

Figure 6. Responses with AG series ferrite chips (gain = +5)

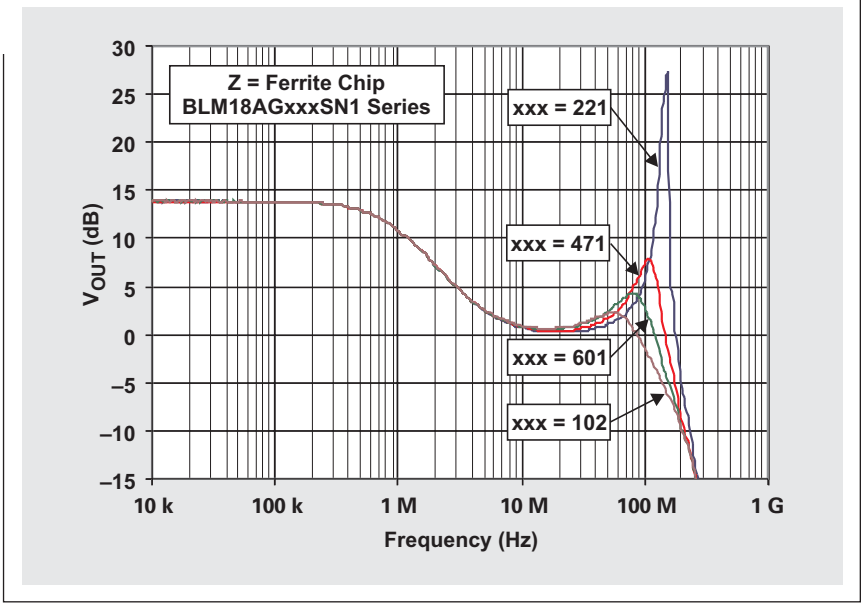
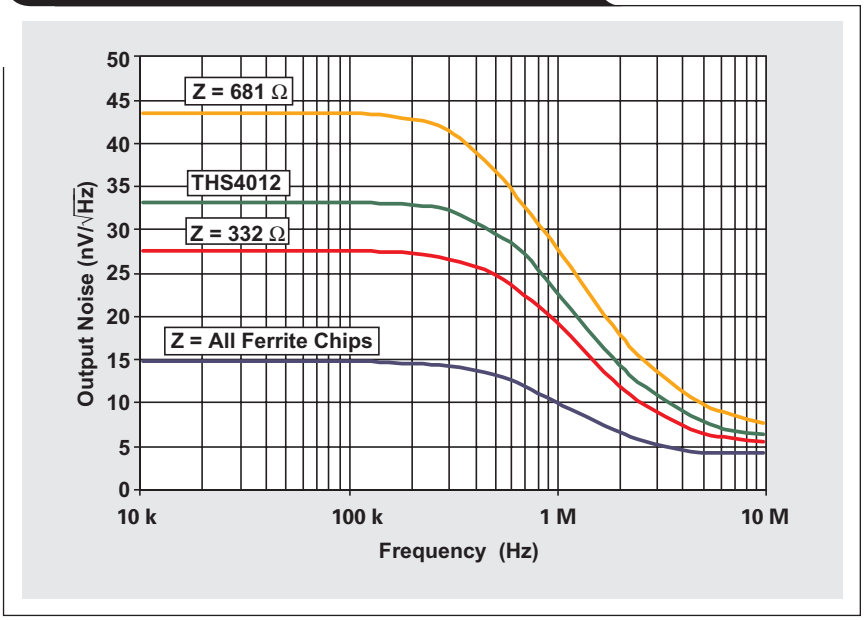


Figure 7. Output noise comparison (gain = +5)



Inverting gain configuration

All of the testing discussed so far was done with the non-inverting gain configuration. This configuration forces the inverting node voltage to move proportionally to the input voltage applied. So how does the system work in the inverting gain configuration where the inverting node is held at a virtual ground? The easy answer is that it works

Figure 8. Inverting gain of 5 VFB configuration

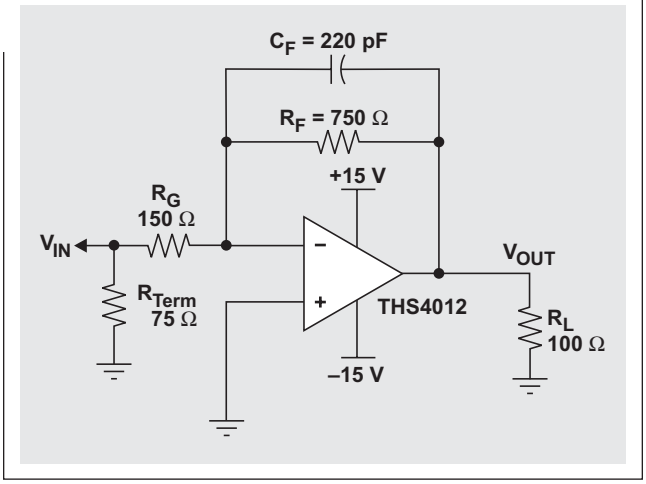
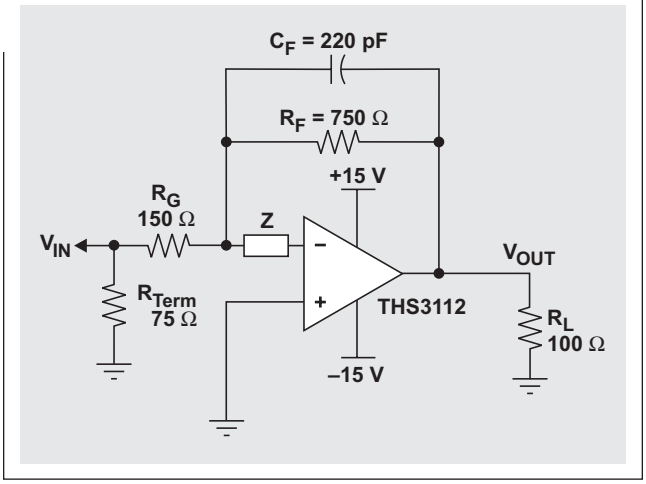


Figure 9. Inverting gain of 5 CFB configuration



exactly the same as before. Figures 8 and 9 show the test circuits for this configuration. The signal gain was kept at a gain of 5.

The same concepts apply for this CFB configuration as for the noninverting configuration. The advantage of this circuit is that the attenuation is not limited to unity gain, or 0 dB, like the noninverting gain circuit. Figure 10 shows the frequency responses of this configuration with varying pure resistor values for Z. The THS4012 response is shown for comparison purposes.

As expected, the responses all look comparable to each other below 10 MHz. Additionally, the resistance values affect the stability and again show that the higher the resistance is, the better the stability. Using a resistance as low as 475 Ω actually shows respectable performance in this configuration. Remember that for oscillations to occur, the gain must be above unity gain, or 0 dB. As long as the peak is below 0 dB, oscillations should not occur. As in the noninverting case, using 200 Ω shows a large narrow peak that will most likely result in stability issues and/or oscillations.

However, notice that above 10 MHz the same general shape occurs for both the CFB and VFB amplifiers. This is caused by the amplifiers' input and output impedances becoming very high above their bandwidth limit. When this occurs, there is a path for the input signal to flow through R_G, through C_F, and then to feed forward to the load. Of course, the amplifiers' own input and output capacitances also affect the amount of feed-through in the circuit; but it is important to remember that this occurs above the amplifiers' usable bandwidths.

Just as for the noninverting configuration, using ferrite chips has several advantages for the inverting configuration.

Figure 10. Frequency responses with resistors (gain = –5)

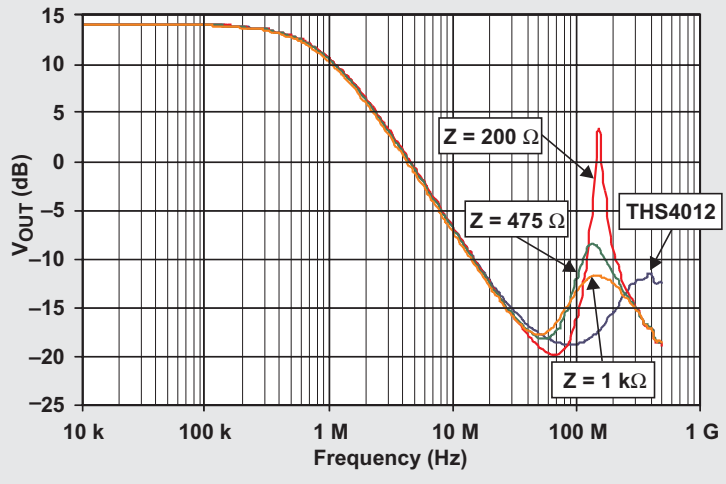


Figure 11 shows the frequency responses of several of these chips. Figure 12 shows the results of using various ferrite chips from the same AG family.

As expected, all of these graphs show the same type of results obtained with the noninverting configuration. Using a low-Q ferrite chip with high impedance will result in a stable system. Although the noise plots for this configuration are not presented here, they will show the same type of results as the noninverting configuration; using ferrite chips will have the lowest output noise of any configuration.

Conclusion

Although this article shows only two configurations with capacitors in the feedback path, it shows the fundamental feasibility of this compensation technique. While resistors do work very well, producing the most stable responses, the drawbacks of the output noise coupled with the dc and ac errors may limit some of the applications.

Using ferrite chips helps alleviate many of these issues, producing the lowest noise of all with no dc errors or in-band ac signal errors; and stability is almost as good as when utilizing resistors. It is important to choose the proper ferrite chip with the amplifier; but this is considered normal procedure for any circuit design and is no more difficult than selecting the right amplifier for the system.

This simple technique helps eliminate one of the major drawbacks of using the CFB amplifier while allowing any system to enjoy many of its benefits. Designers of multiple feedback filters, for example, once limited to the use of VFB amplifiers, can now take advantage of the superior slew rates and lack of gain-bandwidth product characteristics found in the CFB amplifier.

Figure 11. Frequency responses above 10 MHz with ferrite chips (gain = –5)

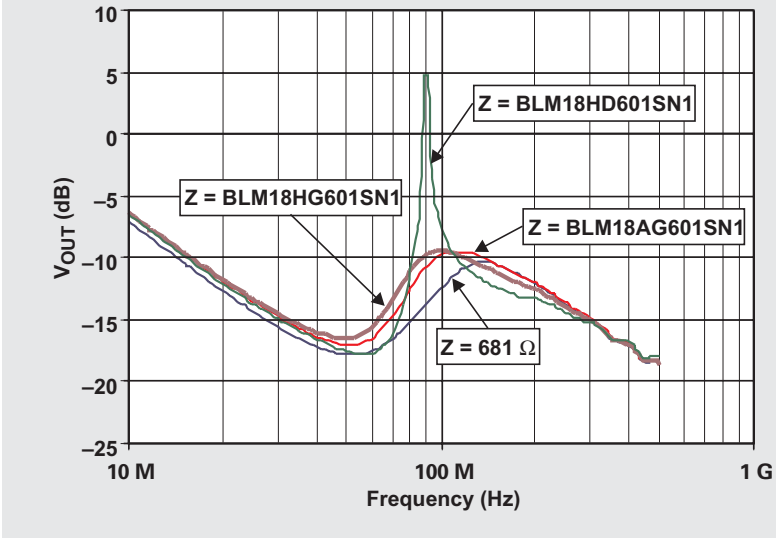
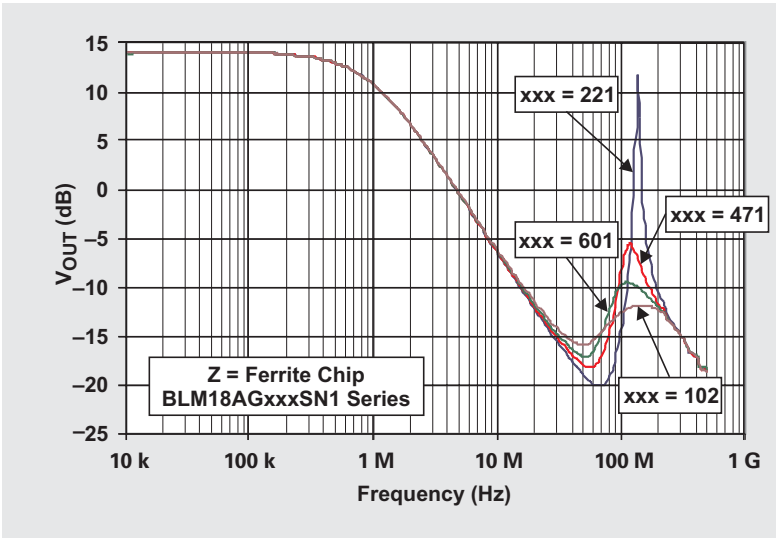


Figure 12. Frequency responses with AG series ferrite chips (gain = –5)



References

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3. "Current Feedback Amplifiers: Review, Stability Analysis, and Applications," Application Bulletin	sboa081
4. "Low-Noise, High-Speed Current Feedback Amplifiers," Data Sheet	slos385
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