UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 1

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Introduction

Power factor corrected (PFC) preregulators are generally used in offline ac/dc power converters with a power level higher than 75 W or to meet line harmonic requirements such as EN61000-3-2. PFC is typically done with a boost converter ac/dc topology due to the continuous input current that can be manipulated through average current-mode control to achieve a near-unity power factor (PF). However, due to the high output voltage of a boost converter, a second dc/dc converter is generally needed to step down the output to a usable voltage. In the past this has been accomplished with two pulse-width modulators (PWMs). One PWM controlled and regulated the PFC power stage, while the second was used to control the step-down converter. The UCC28517 controller reduces the need for two PWMs and combines both of these functions into one control-integrated circuit. The UCC28517 operates the second converter at twice the switching frequency of the PFC stage, which reduces the size of the boost magnetics and the ripple current in the boost capacitor. For more information on this device, please see Reference 7. This article reviews the design of a 100-W ac/dc power stage with power factor correction. A review of the second stage can be found in a future issue of TI's *Analog Applications Journal*.

Variable definitions

ΔI	Change in boost inductor current
$\eta 1$	Output A efficiency
$\eta 2$	Output B efficiency
C_{DIODE}	Boost diode capacitance
Comp	Dynamic range of the multiplier comp pin
C_{OSS}	FET drain-to-source capacitance
f_c	Voltage-loop crossover frequency
f_{line}	Input line frequency
f_p	Single-pole filter frequency
f_R	Ripple frequency
f_S	Minimum switching frequency
f_{SA}	Output A switching frequency
f_{SB}	Output B switching frequency
$G_{ID}(s)$	Power stage gain
G_{CA}	Current amplifier gain
$G_{c(s)}$	Control transfer function
$G_{co(s)}$	Control to output transfer function
g_m	Transconductance amplifier gain
G_{vea}	Voltage amplifier gain
$H_{(s)}$	Voltage divider gain
I_{IAC}	Multiplier input current
I_{MOUT}	Multiplier output
I_{PK}	Peak inductor current, peak diode current, peak switch current
I_{RMS}	RMS device current
I_{SS}	UCC28517 soft-start current of 10 µA
K	Constant typically equal to 1/V
P_{COND}	Device conduction losses
P_{COSS}	Power dissipated by the FET's drain-to-source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by the FET gate
P_{OUTA}	Output A maximum power
P_{OUTB}	Output B maximum power
P_{Q1}	Total FET losses
P_{semi}	Power dissipated by a semiconductor device
Q_{GATE}	FET gate charge
$R_{\theta cs}$	Thermal impedance case-to-sink
$R_{\theta jc}$	Thermal impedance junction-to-case
$R_{\theta sa}$	Thermal impedance sink-to-air
$R_{DS(on)}$	On resistance of the FET
R_{IAC}	Multiplier input resistance
R_{SENSE}	Current sense resistor
$s_{(f)}$	Frequency domain ($2\pi f$)
T_{amb}	Ambient temperature
t_{blank}	Amount of leading-edge blanking time
t_f	FET fall time
t_{holdup}	Boost capacitor hold-up time
T_{jmax}	Maximum semiconductor temperature
t_{on}	Boost inductor energizing on time
t_r	FET rise time
$T_{s(f)}$	Voltage loop frequency response
V_c	Control voltage
V_{CSENSE}	Maximum current sense voltage
V_{drop}	Amount of voltage the boost capacitor has to hold up
$V_{dynamic}$	Current sense voltage range
V_{ea}	Voltage amplifier output
V_f	Forward voltage of a diode
V_{GATE}	Gate-drive voltage
V_{IN}	RMS input voltage
V_{OUTA}	Boost output voltage
V_{OUTB}	Auxiliary output voltage
V_P	Oscillator ramp voltage
V_{pp}	Output peak-to-peak ripple voltage
V_{ripple}	Output B ripple voltage
V_{REF}	UCC28517 internal reference
V_{VFF}	Multiplier feed-forward voltage
Z_{OUT}	Compensation impedance

Table 1. Design specifications

	MAXIMUM	TYPICAL	MINIMUM
V_{IN}	265 V_{rms}		85 V_{rms}
Output A (V_{OUTA})	410 V	390 V	370 V
Output B (V_{OUTB})	12.6 V	12 V	11.4 V
Output A efficiency (η1)		85%	
Output B efficiency (η2)		50%	
P_{OUTA}	100 W		10 W
P_{OUTB}	8 W		4 W
Output ripple A (V_{pp})	12 V		
Output ripple B (V_{ripple})	750 mV		
Output A THD (% THD)	10%		
PF	1		
Output A switching frequency (f_{SA})		100 kHz	
Output B switching frequency (f_{SB})		200 kHz	

The following design example was generated using typical parameters rather than worst-case values. Please refer to Table 1 and Figures 1–3 for design specifications and component placement. All variables are defined in the sidebar on page 13.

PFC boost ac/dc regulator design (OUTA)

Inductor selection

The boost inductor is selected based on the maximum ripple current at the peak of minimum line voltage. The following equations can be used to calculate the required inductor for the boost power stage, assuming that the boost inductor ripple current is 25% of the maximum input current.

$$\Delta I = \frac{\frac{P_{OUTA} \times 0.25 \times \sqrt{2}}{\eta 1}}{V_{IN(min)}}$$

$$D = 1 - \frac{V_{IN(min)} \times \sqrt{2}}{V_{OUTA}}$$

$$L1 = \frac{V_{IN(min)} \times \sqrt{2} \times D}{\Delta I \times f_{SA}}$$

Figure 1. PFC power stage schematic

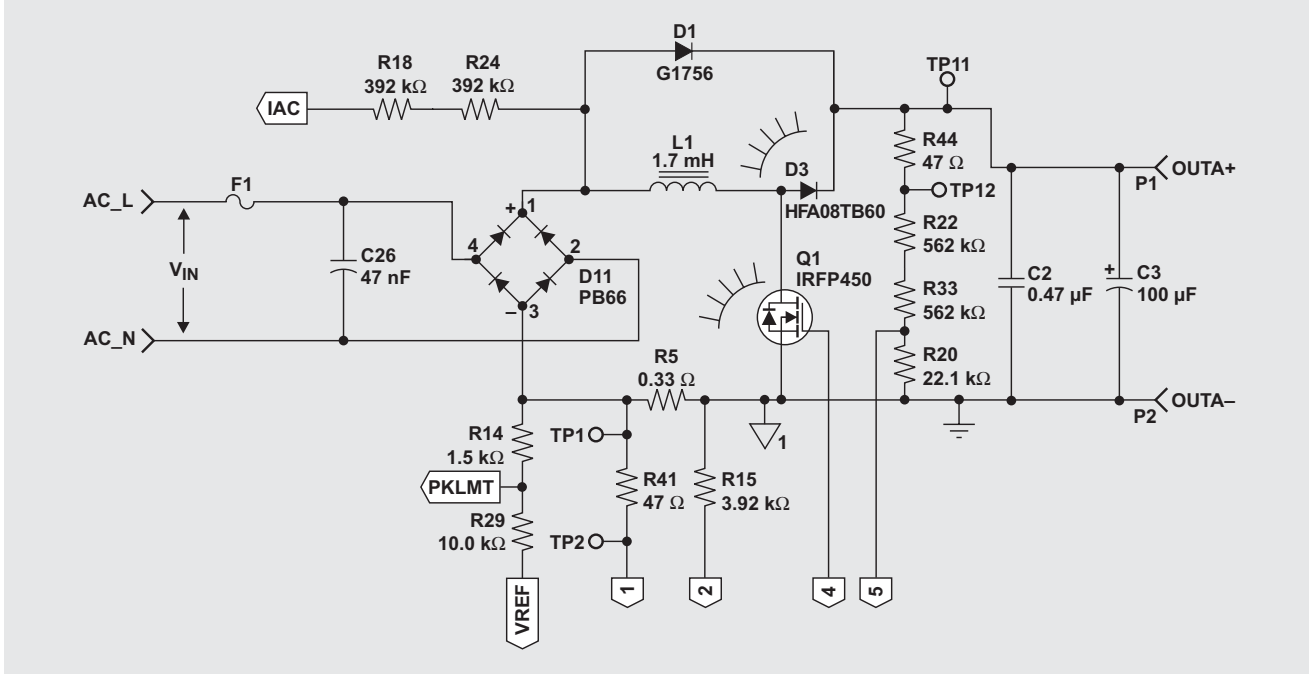


Figure 2. dc/dc power stage schematic

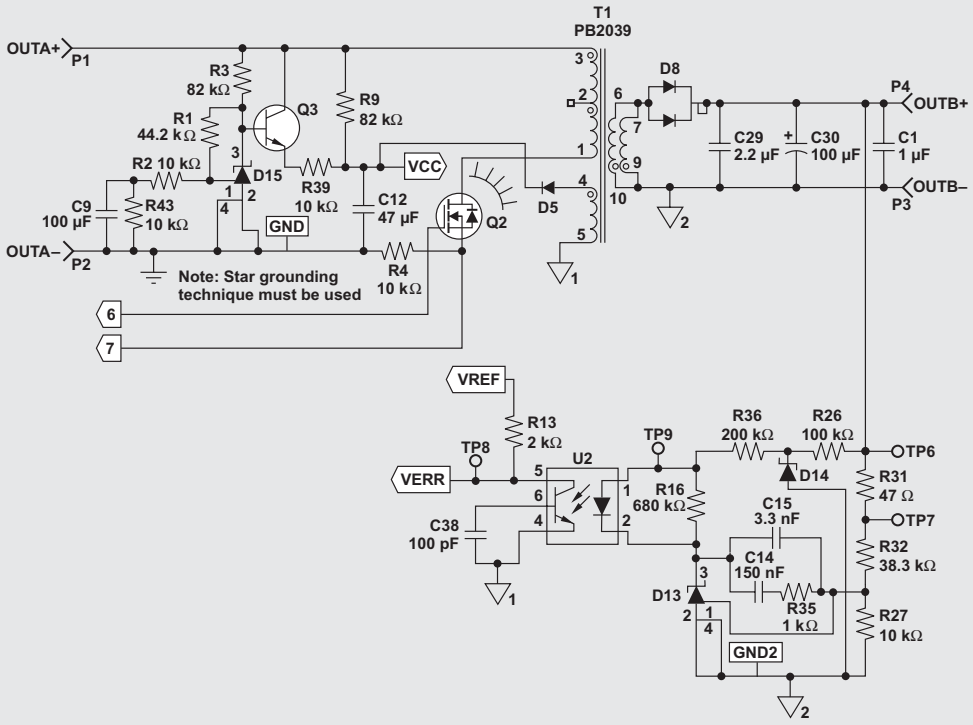
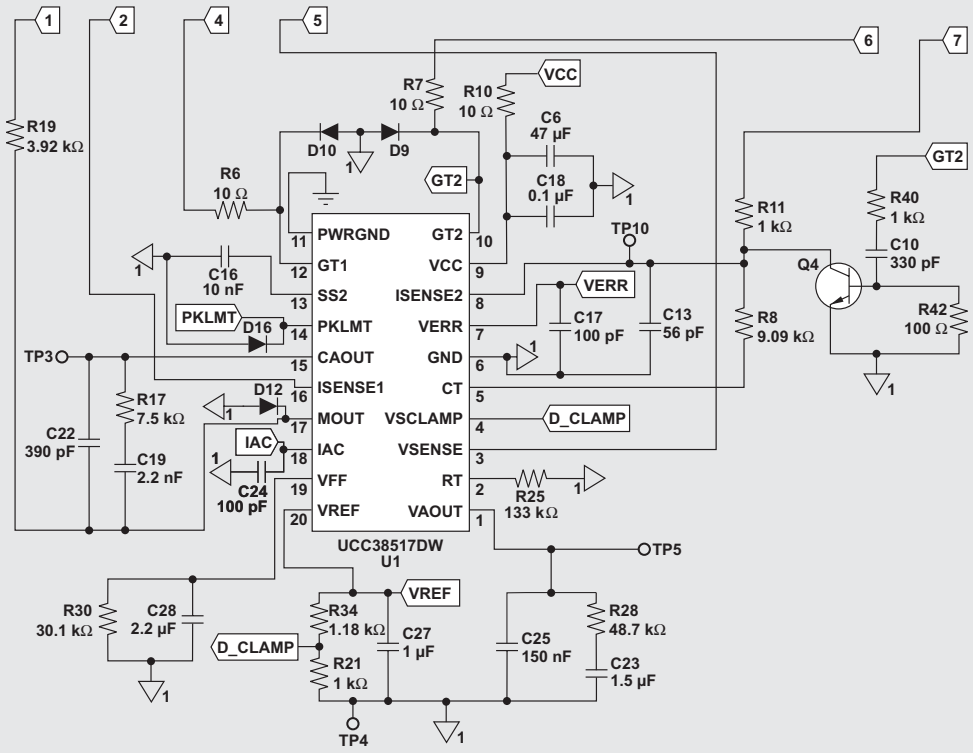


Figure 3. Controller schematic



The calculated inductance for this design was roughly 1.7 mH. To make the design process easier, Cooper Electronics designed the inductor (part number CTX08-14730).

Boost switch (Q1) and boost diode (D3) selection

To select Q1 and D3 properly, a power budget is generally set for these devices to maintain the desired efficiency goal. To meet the power budget for this design, an IRFP450 HEX FET and an HFA08TB60 fast-recovery diode from International Rectifier were chosen.

Equations used to calculate the loss in Q1 were:

$$I_{RMS\_FET} = \frac{P_{OUTA}}{\eta 1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}} \times \sqrt{2 - \frac{16 \times \sqrt{2} \times V_{IN(min)}}{3\pi \times V_{OUTA}}}$$

$$I_{RMS\_L} = \frac{P_{OUTA} \times \sqrt{2}}{\eta 1 \times V_{IN(min)}} \times \frac{V_{OUTA}}{V_{IN(min)}}$$

$$P_{GATE} = Q_{GATE} V_{GATE} \times f_S$$

$$P_{COSS} = \frac{1}{2} C_{OSS} V^2_{OUTA(min)} \times f_S$$

$$P_{COND\_FET} = R_{DS(on)} \times I^2_{RMS\_FET}$$

$$P_{FET\_TR} = \frac{1}{2} V_{OUTA} \times I_{RMS\_L} \times t_r \times f_S$$

$$P_{Q1} = P_{GATE} + P_{COSS} + P_{COND\_FET} + P_{FET\_TR}$$

$$I_{PK} = \frac{P_{OUTA} \times \sqrt{2}}{\eta 1 \times V_{IN(min)}}$$

$$I_{RMS\_DIODE} = \frac{P_{OUTA}}{\eta 1 \times V_{IN(min)}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times \sqrt{2} \times V_{IN(min)}}}$$

$$P_{COND\_DIODE} = V_f \times I^2_{RMS\_DIODE}$$

$$P_{DIODE\_CAP} = \frac{C_{DIODE}}{2} \times V^2_{OUTA} \times f_{SA}$$

$$P_{DIODE} = P_{COND\_DIODE} + P_{DIODE\_CAP}$$

Heat sinks

The following equation can be used to calculate the minimum required thermal impedance of the heat sinks ($R_{\theta sa}$) for this design for Q1 and D3.

$$R_{\theta sa} = \frac{T_{jmax} - T_{amb} - P\_semi \times (R_{\theta cs} + R_{\theta jc})}{P\_semi}$$

The heat sink was designed to ensure that the junction temperature would not go above 75% of these devices' rated maximum with convection cooling, assuming a maximum ambient temperature of 60°C. The heat sink required for Q1 was an AVVID, part number 513201 B 0 25 00.

Output hold-up capacitor (C3) selection

The following equations were used to estimate the minimum hold-up capacitor (C3) size and the maximum allowable RMS current through the boost capacitor (I_{RMS_C3}).

$$C3 \geq 2 \times P_{OUTA} \times \frac{t_{holdup}}{V^2_{OUTA} - (V_{OUTA} - V_{drop})^2}$$

$$I_{RMS\_C3} = \frac{P_{OUTA}}{V_{OUTA}} \times \sqrt{\frac{16 \times V_{OUTA}}{3\pi \times V_{IN(min)} \times \sqrt{2}} - 1}$$

The hold-up capacitor was designed for 16.7 ms of hold-up time (t_{holdup}), allowing an output voltage drop (V_{drop}) of 85 V.

Peak-current limit for the boost power stage

Resistor dividers R14 and R29, along with current sense resistor R5, set up the peak-limit comparator of the UCC28517 that is used to protect the boost switch Q1 from excessive currents. This comparator should be set up so that it does not interfere with the boost converter's power limit or with the pulse-by-pulse current limiting of the step-down converters. For this design example, the flyback converter was designed to go into pulse-by-pulse current limiting at roughly 130% of maximum output power, and the power limit of the boost converter was set at 140% of the maximum output power. The peak-current limit for the boost stage was selected to engage at 150% of the maximum output power to ensure circuit stability.

The current sense resistor R5 was selected to operate over a 1-V dynamic range ($V_{dynamic}$) with the following equation.

$$R5 = R_{SENSE} = \frac{V_{dynamic}}{I_{PK} + 0.5 \times \Delta I}$$

The following equation can be used to size resistor R14 properly if R29 is first selected as a standard resistance value.

$$R14 = \frac{\left(\frac{P_{OUTA} \times 1.5 \times \sqrt{2}}{V_{IN(min)} \times \eta 1} + \Delta I\right) \times R5 \times R29}{V_{REF}}$$

Multiplier

The multiplier output of the UCC28517 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high-PF operation. As such, the proper functioning of the multiplier is key to the success of the design. The output of the multiplier, I_{MOUT}, can be expressed as

$$I_{MOUT} = I_{IAC} \frac{V_{ea(max)} - 1}{K \times V_{VFF}^2},$$

where K is a constant typically equal to 1/V.

The I_{IAC} signal is obtained through a high-value resistor (R_{IAC} = R18 + R24) connected between the rectified ac line and the IAC pin of the UCC28517. This resistor is sized to give the maximum I_{IAC} current at the highest expected line voltage. For the UCC28517 the maximum I_{IAC} current is about 500 µA. A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional; but noise can become an issue, especially during low line voltages, assuming a universal line operation of 85 to 265 Vac gives an R_{IAC} value of 750 kΩ. Because of voltage-rating constraints of standard ¼-W resistors, two or more lower-value resistors connected in series are needed to give roughly a 750-kΩ value and to distribute the high voltage across them.

The current through R_{IAC} is mirrored internally to the VFF pin, where it is filtered to produce a voltage feed-forward signal proportional to line voltage that is free of the 120-Hz ripple component. This second harmonic ripple component at the VFF pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial (see Reference 4). Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input ac line voltage, the amount of attenuation required by this filter is

$$\frac{1.5\%}{66\%} \approx 0.022 \text{ (see Reference 5).}$$

A ripple frequency (f_R) of 120 Hz and an attenuation of 0.022 gives us a single-pole filter with

$$f_p = 120 \text{ Hz} \times 0.022 = 2.6 \text{ Hz}.$$

The voltage at the VFF pin not only supplies a voltage feed-forward signal but also activates input current fold-back when the V_{VFF} drops below 1.5 V. Please see Reference 2 for a detailed explanation of how these control ICs provide power limiting. The following equations were used to size resistor R30 and filter capacitor C20.

$$R30 = \frac{1.5 \text{ V}}{\frac{V_{IN(min)} \times 0.9}{(R18 + R24) \times 2}}$$

$$C20 = \frac{1}{2\pi \times 30 \text{ k}\Omega \times 2.6 \text{ Hz}}$$

This results in a single-pole filter, which adequately attenuates the harmonic distortion and provides power limiting.

The multiplier's output resistor R19 is sized to match the maximum current through the sense resistor (R5) to the maximum multiplier current. R15 is sized to balance the offset current in the current amplifier and needs to be set to the same value as R19. The following equations were used to size R15 and R19.

$$I_{MOUT(max)} = \frac{I_{IAC}@V_{IN(min)} \times (V_{ea(max)} - 1\text{ V})}{K \times V_{VFF}^2}$$

$$R19 = R15 = \frac{V_{dynamic}}{I_{MOUT(max)}}$$

Current loop compensation for the boost converter

The following equation defines the gain of the power stage, where V_P is the maximum voltage swing of the UCC28517 oscillator ramp, roughly 5 V.

$$G_{ID}(s) = \frac{V_{OUTA} \times R5}{s \times L1 \times V_P}$$

To have a good dynamic response, the crossover frequency of the current loop was set to 1/10 the switching frequency. This can be achieved by setting the gain of the current amplifier (G_{CA}) to the inverse of the current loop power-stage gain at the crossover frequency. For this design the current amplifier required a gain of 2.581 at 10 kHz. The following equations were used to compensate the current amplifier of the boost power stage.

$$G_{CA} = \frac{1}{G_{ID}(s)} = 2.581$$

$$R17 = G_{CA} \times R19$$

$$C19 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{10}}$$

$$C22 = \frac{1}{2\pi \times R17 \times \frac{f_{SA}}{2}}$$

Voltage loop compensation for the boost converter

Figure 4 shows the small-signal-control block diagram for this application. The following equations describe small-signal gain as well as the voltage loop frequency response, $T_{s(f)}$.

$$H_{(s)} = \frac{R20}{R20 + R32 + R32}$$

$$G_{c(s)} = g_m \times \frac{s_{(f)} \times R28 \times C23 + 1}{s_{(f)} \times (C23 + C25) \times \left(\frac{s_{(f)} \times C23 \times C25}{C23 + 25} + 1 \right)}$$

$$G_{co(s)} = \frac{\Delta V_{OUTA}}{\Delta V_c} = \frac{P_{OUTA}}{V_{ea(max)} \times s \times V_{OUTA} \times C3}$$

$$T_{s(f)} = -H_{(s)} \times G_{c(s)} \times G_{co(s)}$$

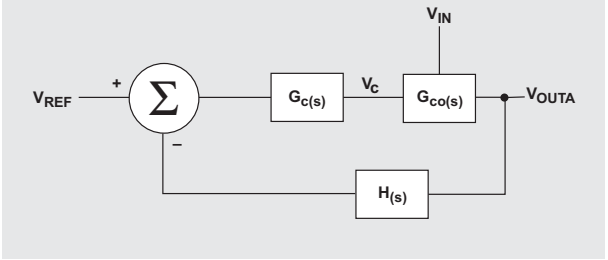
To reduce third-harmonic distortion, the voltage loop typically crosses over at roughly 10 to 12 Hz. For this design, the voltage-loop crossover frequency (f_c) was selected to be roughly 10 Hz. The following equations were used to select the components to compensate the voltage loop, $T_{s(f)}$, to cross over at the desired f_c with 45 degrees of phase margin.

$$R28 = 2\pi \times V_{ea(max)} \times f_c \times C3 \times \frac{V_{OUTA} \times \eta 1}{g_m \times P_{OUTA} \times H_{(s)}}$$

$$C23 = \frac{1}{2\pi \times R28 \times f_c}$$

C25 was selected to attenuate the 120-Hz output ripple voltage (V_{pp}) to 1.5% (% THD) of the voltage amplifier's dynamic output range.

Figure 4. dc/dc converter control loop



$$V_{pp} = \frac{P_{OUTA}}{\pi \times 120\,Hz \times C3 \times V_{OUTA}}$$

$$G_{vea} = \frac{\%\,THD \times V_{ea(max)}}{V_{pp} \times 100}$$

$$Z_{OUT} = \frac{G_{vea}}{H_{(s)} \times g_m}$$

$$C25 = \frac{1}{2\pi \times Z_{OUT}}$$

After the design was complete, the frequency response of the voltage loop, $T_{s(f)}$, was measured with a network analyzer; and the results are shown in Figure 5. It can be observed that f_c was roughly 8 Hz with a phase margin of roughly 50 degrees.

Figure 5. Frequency response of power stage A

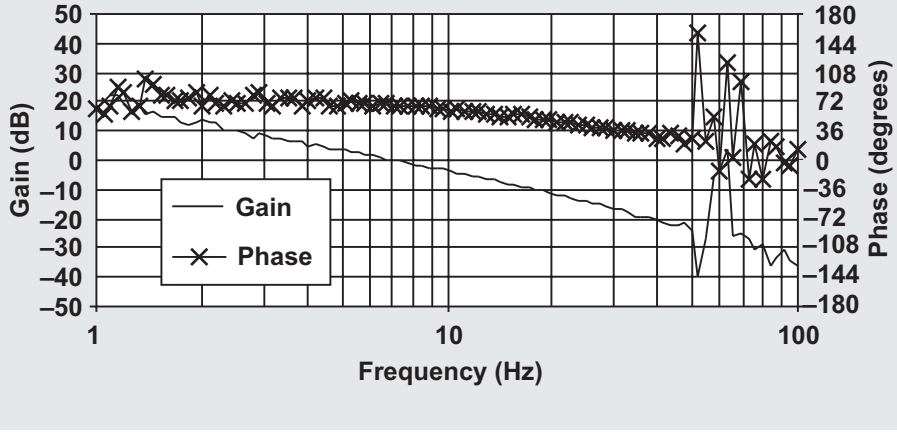


Figure 6. Output A THD vs. output power

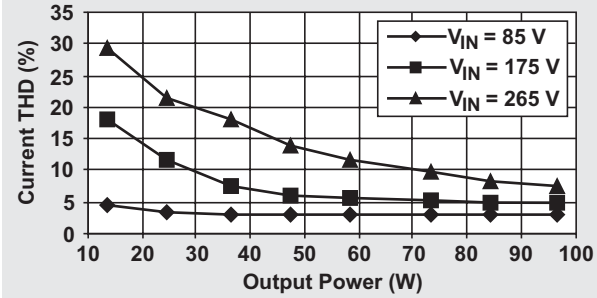


Figure 7. Output A efficiency vs. output power

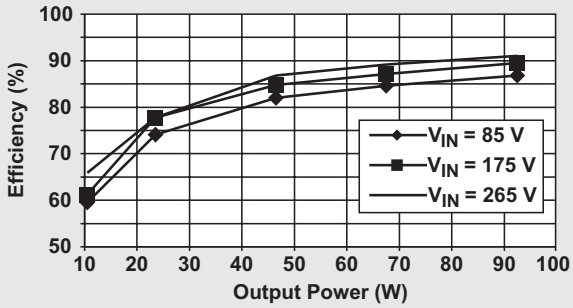


Figure 8. Output A PF vs. output power

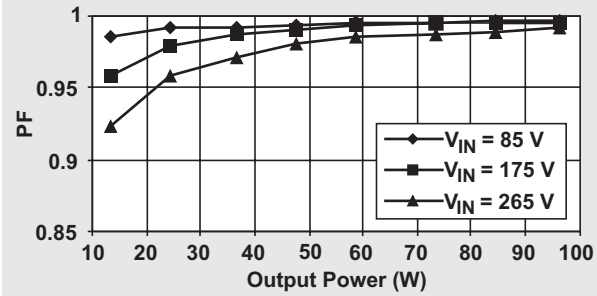
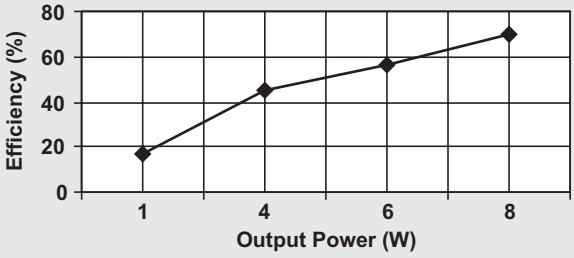


Figure 9. Output B efficiency vs. output efficiency



Summary

This article reviewed the design of a 100-W PFC ac/dc preregulator, which is the first stage in a two-stage power converter. The UCC2851X family of combination PWM controllers is perfect for offline applications that require PFC and auxiliary power supplies to meet different system requirements. The performance of this two-stage power converter is shown in Figures 6–9.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	TI Lit. #
1. Laszlo Balogh, "Design Review: 140W, Multiple Output High Density DC/DC Converter," p. 6-9	slup117
2. Laszlo Balogh, "Unitrode – UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends," Unitrode Design Note	slua196
3. Lloyd Dixon, "Control Loop Cookbook," p. 5-17	slup113
4. Lloyd Dixon, "Optimizing the Design of a High Power Factor Switching Preregulator," pp. 7-11–7-12	slup093
5. James P. Noon, "A 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions," pp. 1-11–1-14	slup106
6. "Practical Considerations in Current Mode Power Supplies," Unitrode Application Note	slua110
7. "Advanced PFC/PWM Combination Controllers," Data Sheet	slus517
8. "UCC28517 EVM User's Guide"	sluu117

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