Stacked-FET switches enable high-efficiency, high-density solutions

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Introduction

High-efficiency, high-density power supplies have been a trend for communications equipment due to increasing power consumption and reduced board space. A stacked-FET switch enables high-efficiency and high-density solutions. Two real design examples are examined to illustrate this point. The first is a 30-A design where the benefits of a stacked-FET switch are evaluated relative to size reduction, efficiency gain and thermal budget savings. A second design implements the stacked-FET switch with an integrated driver to further increase system efficiency in a 60-A supply.

As modern electronics equipment advances in speed and performance, the number of power rails keeps increasing in addition to an increase in power consumption. Conversely, the physical area for power supplies keeps shrinking because precious real estate is given to the core ASIC and processors. As such, a high-efficiency, high-density power supply is a challenge for every power designer.

By combining the latest NexFET™ silicon and innovative packaging technologies, a dual FET (Figure 1) consists of two stacked FETs in a SO8 (5 mm x 6 mm) package. This configuration reduces the device footprint by half and doubles the output density.

Using a stacked-FET switch in point-of-load (PoL) applications has many benefits. this article presents a comparative study for a 1.8-V/30-A application using discrete FETs versus stacked FETs.

Figure 1. Stacked-FET switches in a SO8 package

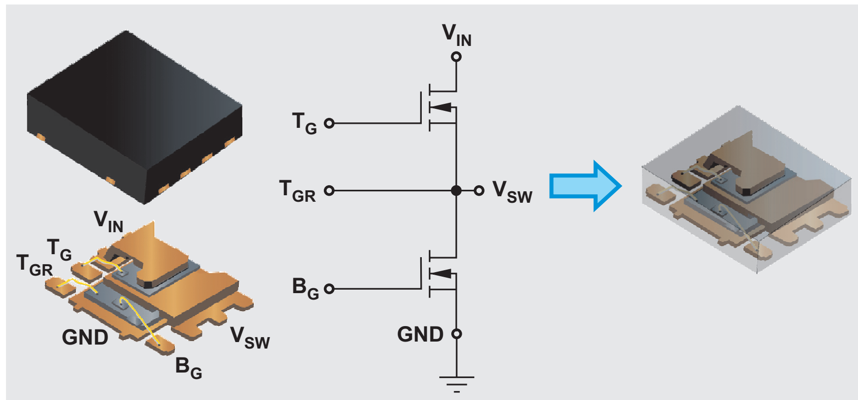
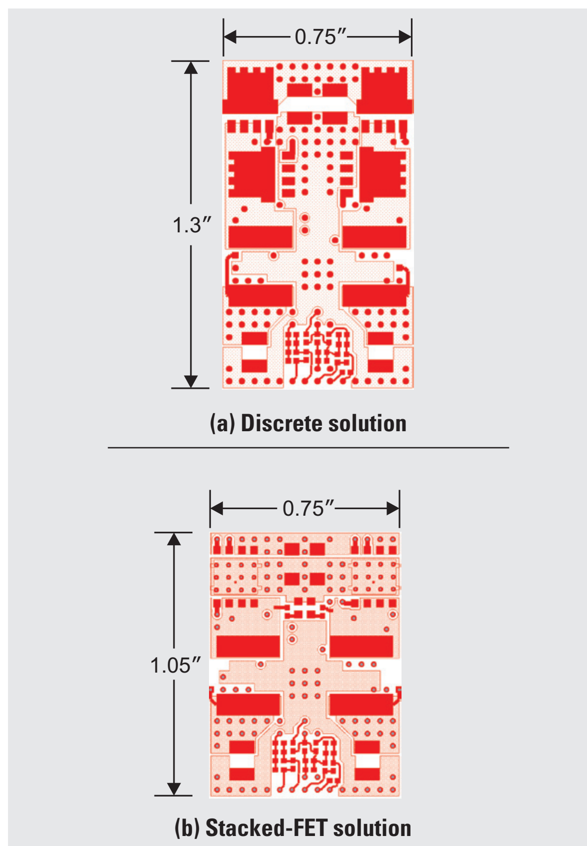


Figure 2. A stacked-FET solution size is 20% smaller than a discrete-FET solution



Reduced footprint

In the 30-A design example, a dual-phase synchronous buck controller was selected with optimum performance over ripple and transient responses. In the discrete solution layout, the FETs occupy nearly half the area. By replacing two discrete FETs with one stacked FET, the solution size shrinks by 20%. Figure 2 shows two layouts: (a) a discrete solution and (b) the stacked-FET solution. The discrete solution measures 0.75 by 1.3 inches, and the stacked-FET solution measures 0.75 by 1.05 inches.

Increased system efficiency

Compared to other state-of-the-art discrete FETs (Figure 3), the stacked-FET efficiency (red curve) is at least 2.2% higher. A stacked-FET switch, such as the CSD87350, has lower on-state resistance ($R_{DS(on)}$) and lower gate charge due to its unique device structure. Moreover, the stacked-FET packaging technique removes the parasitic inductance associated with traditional wire-bonded technology. Thus, it optimizes the switching speed and increases system efficiency. Both designs use the same inductor, input and output capacitors, and were tested under the same test conditions with a 10-V input, 1.8-V output and 300-kHz switching frequency.

Cooler operating temperatures

The power loss of stacked FETs is the sum of both the top and bottom FETs, but its thermal resistance is much less than that of discrete FETs. As illustrated in Figure 4, a stacked-FET switch runs 23° cooler than discrete FETs under the same test conditions (10 V_{IN}, 1.8-V/30-A output, 300 kHz). When the discrete FET reaches 108.7°C, the stacked-FET dies only reach 85.6°C because it is GND referenced.

The large area of the exposed pad connects to the ground plane of the PCB by 12 thermal vias, which utilizes multiple inner ground layers commonly available with a modern multi-layer PCB. For the discrete FET solution, the heat is concentrated in a small area, known as a switching plane, which prohibits multiple vias for signal integrity concerns.

It was demonstrated that stacked-FET technology enables high-efficiency and high-density solutions. One stacked FET replaces two discrete FETs, thus, reducing the overall solution size by 20%. Its increased efficiency and effective thermal conductivity allows it to run 23° cooler versus a discrete FET under same test conditions.

Figure 3. A stacked FET excels over other discrete FETs under the same test conditions

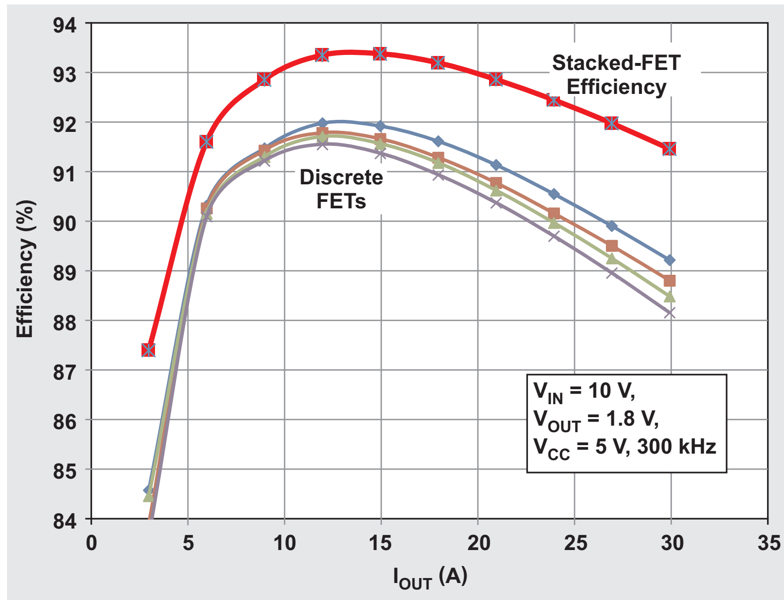
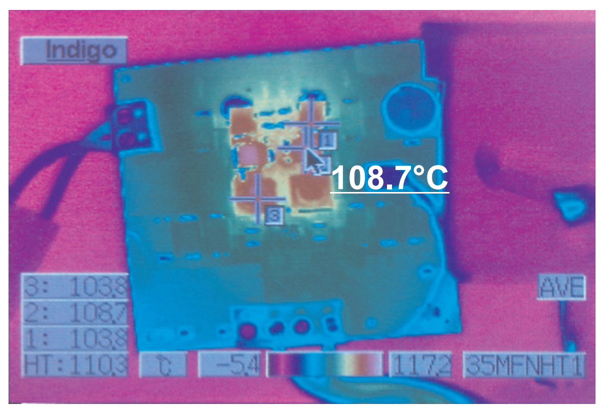
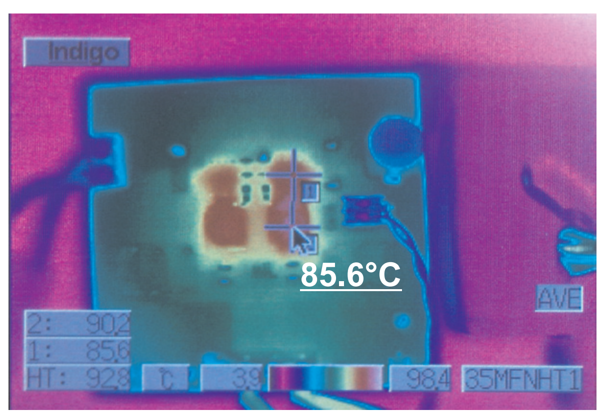


Figure 4. Operating temperatures of discrete and stacked FETs



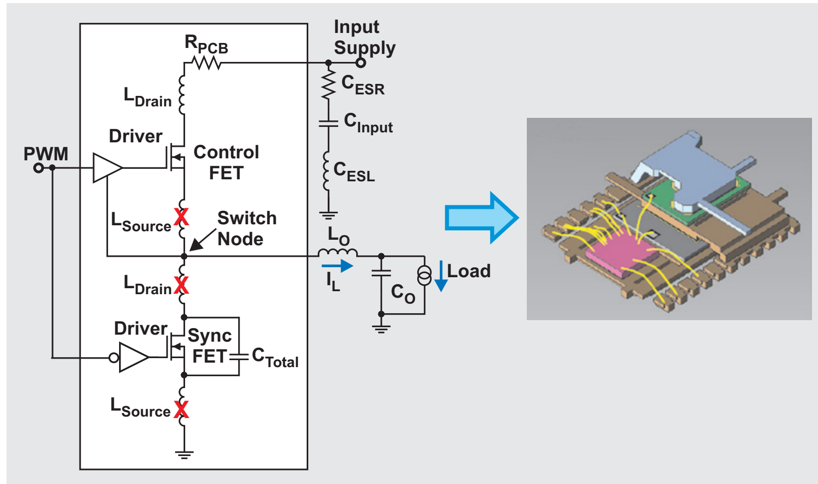
(a) Thermal image of a discrete FET



(b) Thermal image of a stacked FET

To further push the technology boundary, a new device, the CSD95372B in Figure 5, integrates a stacked-FET switch with an integrated driver. The package maintains the same size as a standard FET, which is SO8 (5 mm x 6 mm) package. By shortening the drive-to-FET distance, it fully optimizes the drive capability by minimizing the driver-related parasitic inductances. It has higher switching speeds, lower conduction loss and requires less PCB real estate. Therefore, it achieves even higher system efficiency.

Figure 5. A stacked FET with driver



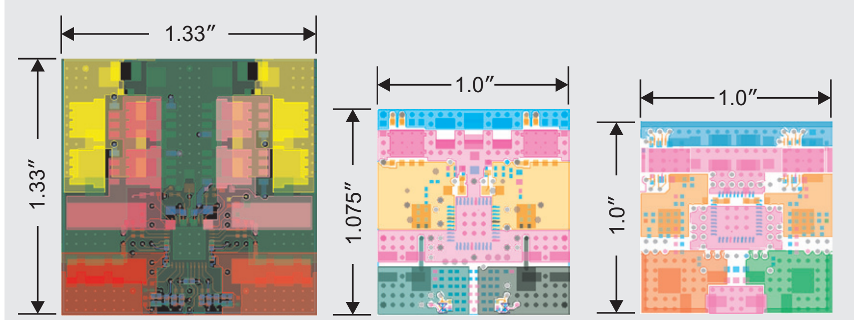
Advantages of stacked FET with integrated driver

A 1-V/60-A design solution was used to demonstrate the advantages of a stacked-FET switch with driver. This design was tested with a 12-V input, 1-V output and a 500-kHz switching frequency. The baseline solution used eight discrete FETs to supply the 60-A load current. As shown in Figure 6(a), the solution size is 1.33 by 1.33 inches.

In Figure 6(b), eight discrete FETs were replaced with two stacked FETs. The solution size now shrinks to 1 by 1.075 inches. This now results in a 40% size reduction from the discrete-FET solution.

In Figure 6(c), two stacked-FET switches with driver also replaced eight discrete FETs. This solution size is 1 by 1 inch, or a 43% size reduction.

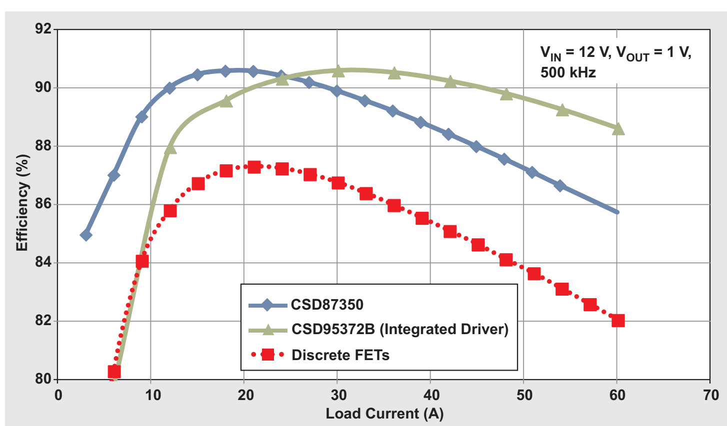
Figure 6. Three solutions for a 1-V/60-A supply



(a) Discrete-FET solution (b) Stacked-FET solution (c) Stacked-FET with driver solution

With the same test conditions applied to each design solution, the stacked-FET with driver solution achieves the highest efficiency of 88.6%. This is 6.6% higher than the discrete-FET efficiency and 2.9% higher at full load (60 A) than the stacked-FET solution without an integrated driver. Figure 7 shows the efficiency of the three different solutions. The green curve represents the stacked-FET with driver solution, the blue curve represents the stacked-FET solution, and the red curve represents a discrete-FET solution.

Figure 7. System efficiency is compared among three designs



Conclusion

The increasing efficiency and density requirements suggests that a high level of package integration is needed. Stacked-FET switches have silicon improvements and innovative packaging technologies that increase system efficiency. Likewise, by replacing a stacked-FET device with one that has an integrated driver, system efficiency further improves due to optimized driver and minimized parasitics.

Related Web sites

www.ti.com/1q15-CSD87350Q5D

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