User's Guide

SNAU215A – August 2017 – Revised December 2017

LMK04832EVM User's Guide

This user's guide describes how to set up and operate the LMK04832 evaluation module (EVM).

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1 Evaluation Board Kit Contents

The evaluation board kit includes what is shown in Table 1.

Table 1. EVM Contents

HSDC004	
Evaluation Board	(1) LMK04832 Evaluation Board with differential VCXO
Communication Interface	(1) USB2ANY

2 Quick Start

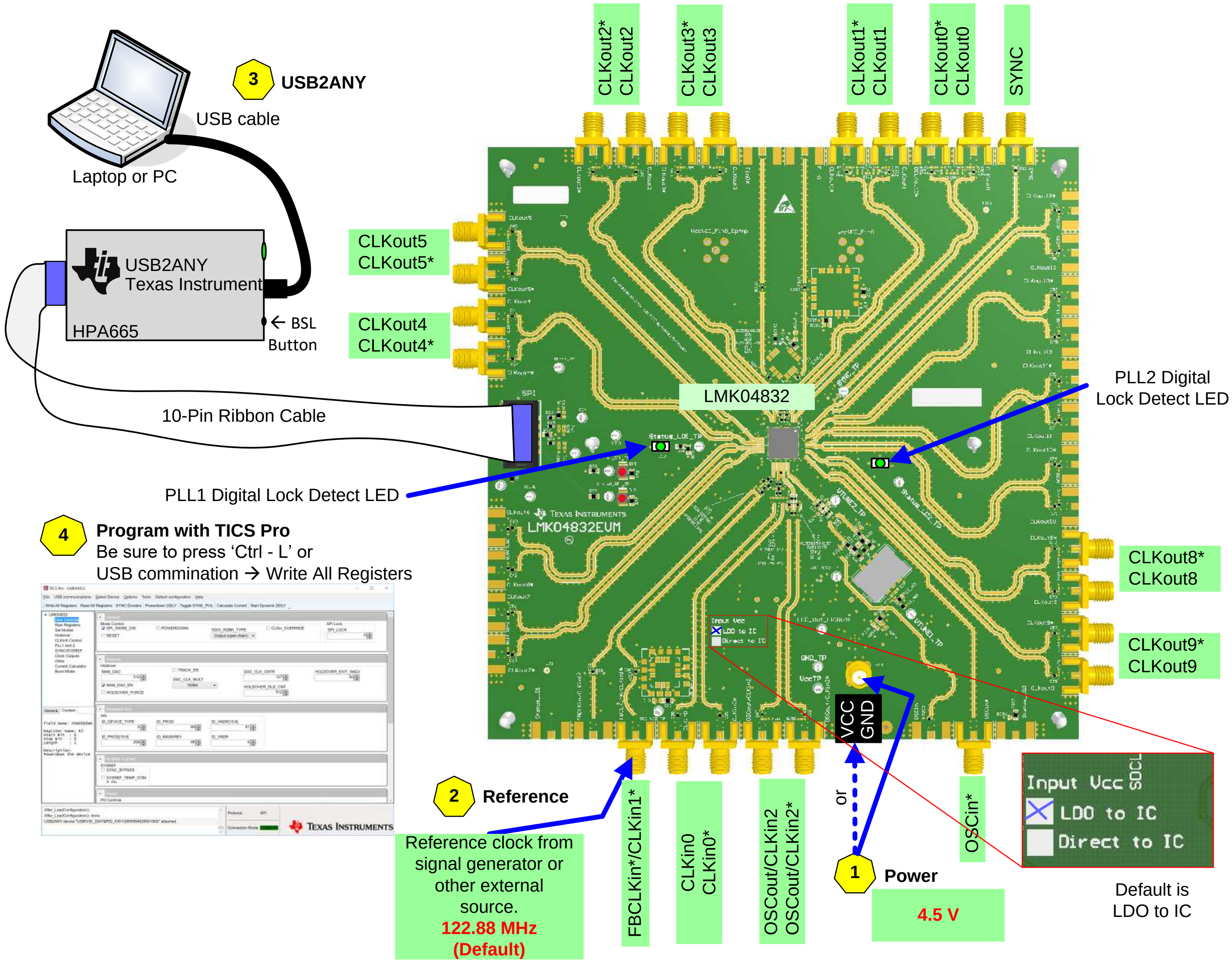

Figure 1. Quick Start Diagram

2.1 Quick Start Description

The LMK04832 EVM allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Connect a voltage of **4.5** volts to the V_{CC} SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO. VCXO operates at 3.3 V using onboard LP5900 LDO.

NOTE: The LP3878-ADJ LDO can source a maximum of 800 mA, any configuration requiring more than 800 mA please bypass the LDO. The **Current Calculator** page Section A.11 can help to determine how much current the configuration requires.

2. Connect a reference clock to the CLKin1* port from a signal generator or other source. Use **122.88 MHz** for default configuration. Exact frequency and input port (CLKin0/CLKin1) depends on programming.
3. Connect USB2ANY to PC and EVM.
4. Program the device with TICS Pro. TICS Pro is available for download at: http://www.ti.com/tool/ticspro-sw.
   a. Select PLMK04832 from the *Select Device* Menu. Click *Select Device → Clock Generator/Jitter Cleaner (Dual Loop)*.
   b. Select **USB2ANY mode** from the Communication Setup window. To access this, select *USB communications → Interface*. Confirm PC to USB communications by clicking *Identify* to see blinking green LED on USB2ANY.
   c. Select a default mode from the *Default configuration* Menu. For the quick start use, *CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz*.
   d. **Ctrl+L** must be pressed at least once to load all registers. Alternatively click menu *USB communications → Write All Registers* or the *Write All Registers* button on toolbar or **Raw Registers** page Section A.3.
5. Measurements may be made at an active CLKout port through the SMA connector.

2.1.1 Clock Outputs Page Description

Clock outputs are grouped in pairs. This description applies for all clock outputs on the Clock Outputs page Section A.9.

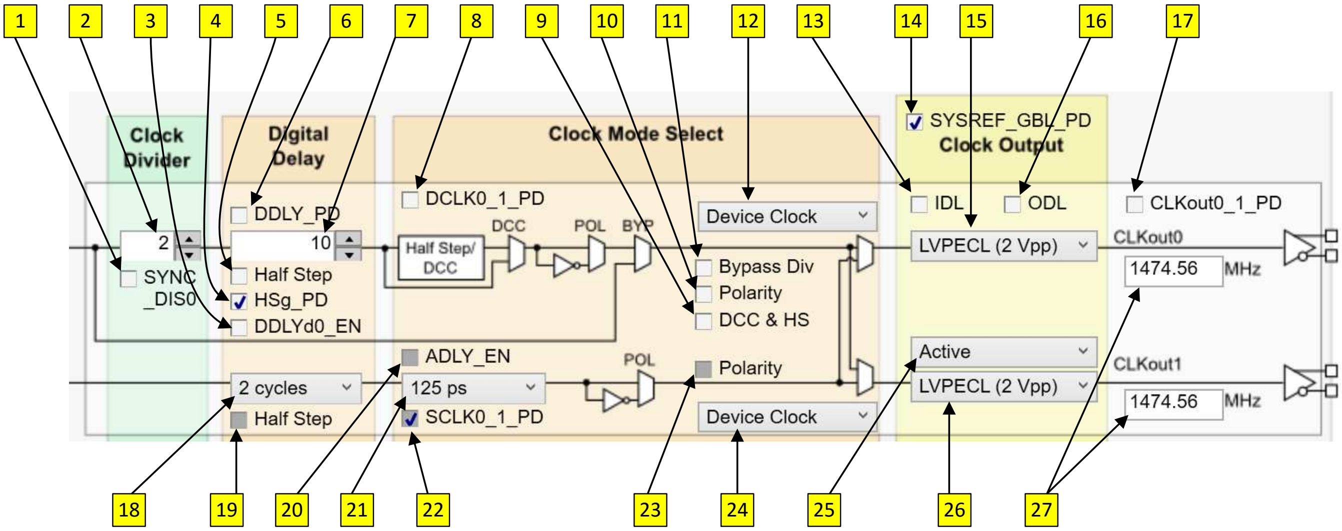

Figure 2. Clock Outputs Page Description Diagram

1. SYNC_DISX: Prevent the divider from being reset by SYNC/SYSREF path.
2. DCLKX_Y_DIV: Divide value for the device clock. If set to 1 then #9 on list must = 1.
3. DDLYdX_EN: Enable dynamic digital delay for this divider.
4. DCLKX_Y_HSg_PD: If clear, glitchless half-step adjustments are enabled.
5. DCLKX_Y_HS: Set half step for this divider. DCLKX_Y_DCC (DCC & HS) must = 1.
6. DCLKX_Y_DDLY_PD: If clear, the digital delay value is assured when a SYNC occurs.
7. DCLKX_Y_DDLY: The digital delay value to be used when a SYNC occurs.
8. DCLKX_Y_PD: Power down the device clock divider and path.
9. DCLKX_Y_DCC: Enable duty cycle correct and half-step for this device clock divider.
10. DCLKX_Y_POL: If set, polarity of device clock is inverted.
11. DCLKX_Y_BYP: If set, the device clock divider is bypassed for CLKoutX and #15 must be CML.
12. CLKoutX_SRC_MUX: Select device clock or SYSREF clock path for CLKoutX.
13. CLKoutX_Y_IDL: Increase input drive level to improve noise floor at cost of power.
14. SYSREF_GBL_PD: Set the conditional for SCLKX_Y_DIS_MODE registers.
15. CLKoutX_FMT: Set the clock output format for CLKoutX.
16. CLKoutX_Y_ODL: Increase output drive level to improve noise floor at cost of power. No effect for CLKoutX in bypass mode.
17. CLKoutX_Y_PD: Power down the entire CLKoutX_Y clock pair.
18. SCLKX_Y_DDLY: The SYSREF clock digital delay setting.
19. SCLKX_Y_HS: Set half step for the SYSREF output.
20. SCLKX_Y_ADLY_EN: Enable analog delay for the SYSREF clock path.
21. SCLKX_Y_ADLY: If enabled, set the analog delay for the SYSREF clock path.
22. SCLKX_Y_PD: Power down the SYSREF clock path.
23. SCLKX_Y_POL: If set, polarity of SYSREF output clock is inverted.
24. CLKoutY_SRC_MUX: Select device clock or SYSREF clock path for CLKoutY.
25. SCLKX_Y_DIS_MODE: Set the output state of output clock drivers for the SYSREF clock. For values of 1 and 2 works in conjunction with control on this list #14, SYSREF_GBL_PD.

26. CLKoutY_FMT: Set the clock output format for CLKoutY.
27. Clock output frequency for CLKoutX and CLKoutY.

NOTE: Setting a register equal to 0 OR un-checking a register's checkbox performs the same action. Similarly, setting a register equal to 1 *is the same as* checking that register's checkbox.

2.1.2 TICS Pro Tips

Mousing over different controls will display some help prompt with the register address, the data bit location and length, and a brief register description in the lower left *Context* help pane.

3 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO) for the phase noise of a dirty reference clock. The first PLL is typically configured with a narrow loop bandwidth to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK04832 evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 1 kHz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. Table 2 and Table 3 contain the parameters for PLL1 and PLL2 for each oscillator option.

TI's PLLatinum Sim tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/pllatinumsim-sw.

3.1 PLL1 Loop Filter

Table 2. PLL1 Loop Filter Parameters for Crystek 122.88-MHz VCXO(1)

122.88-MHz VCXO PLL			
Phase Margin	50°	**Kφ (Charge Pump)**	450 µA
Loop Bandwidth	14 Hz	**Phase Detector Freq**	1.024 MHz
		VCO Gain	2.5 kHz/V
Reference Clock Frequency	122.88 MHz	**Output Frequency**	122.88 MHz (To PLL 2)
Loop Filter Components	LF1_C1 (C42) = 100 nF	LF1_C2p (C43) = 680 nF	LF1_R2 (R5) = 39 kΩ

(1) Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

3.2 PLL2 Loop Filter

Table 3. Integrated VCO PLL(1)

	LMK04832		
	VCO0	VCO1	
C1	0.0047		nF
LF2a_C2 (C2)	3.9		nF
C3 (internal)	0.03		nF
C4 (internal)	0.01		nF
LF2a_R2 (R2)	0.82		kΩ
R3 (internal)	0.2		kΩ
R4 (internal)	0.2		kΩ

(1) PLL Loop Bandwidth is a function of Kφ, Kvco, N as well as loop components. Changing Kφ and N will change the loop bandwidth.

Table 3. Integrated VCO PLL[1] (continued)

	LMK04832		
	VCO0	VCO1	
Charge Pump Current, Kφ	3.2		mA
Phase Detector Frequency	122.88		MHz
Frequency	2457.6	2949.12	MHz
Kvco	13.0	25.0	MHz/V
N	22	24	
Phase Margin	82	83	degrees
Loop Bandwidth	382	440	kHz

4 Default TICS Pro Modes for the LMK04832

TICS Pro saves the state of the selected LMK04832 device when exiting the software. To ensure a common starting point, the following modes listed in Table 4 may be restored by clicking *Default configuration* and selecting the appropriate device configuration.

Table 4. Default TICS Pro Modes for the LMK04832

DEFAULT TICS PRO MODE	DEVICE MODE	CLKin FREQUENCY	OSCin FREQUENCY
CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz

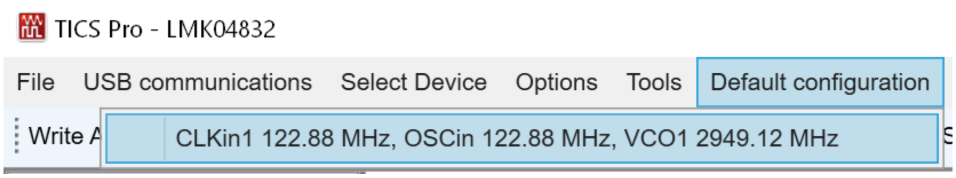

Figure 3. Selecting a Default Mode for the LMK04832 Device

5 Using TICS Pro to Program the LMK04832

This section will demonstrate how to use TICS Pro. For more information on using TICS Pro, refer to Appendix A. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

Before proceeding, be sure to follow the instructions in Section 2 to ensure proper hardware connections.

5.1 Start TICS Pro Application

Click *Start* → *Programs* → *Texas Instruments* → *TICS Pro*

The TICS Pro program is installed by default to the Texas Instruments application group.

5.2 Select Device

Click *Select Device* → *Clock Conditioners* → *Dual Loop* → *LMK04832*

Once started, TICS Pro will load the last used device. A recent history of used devices can be quickly accessed under the *File* Menu. To load a new device, click *Select Device* from the menu bar, then select the subgroup and finally, the device to load.

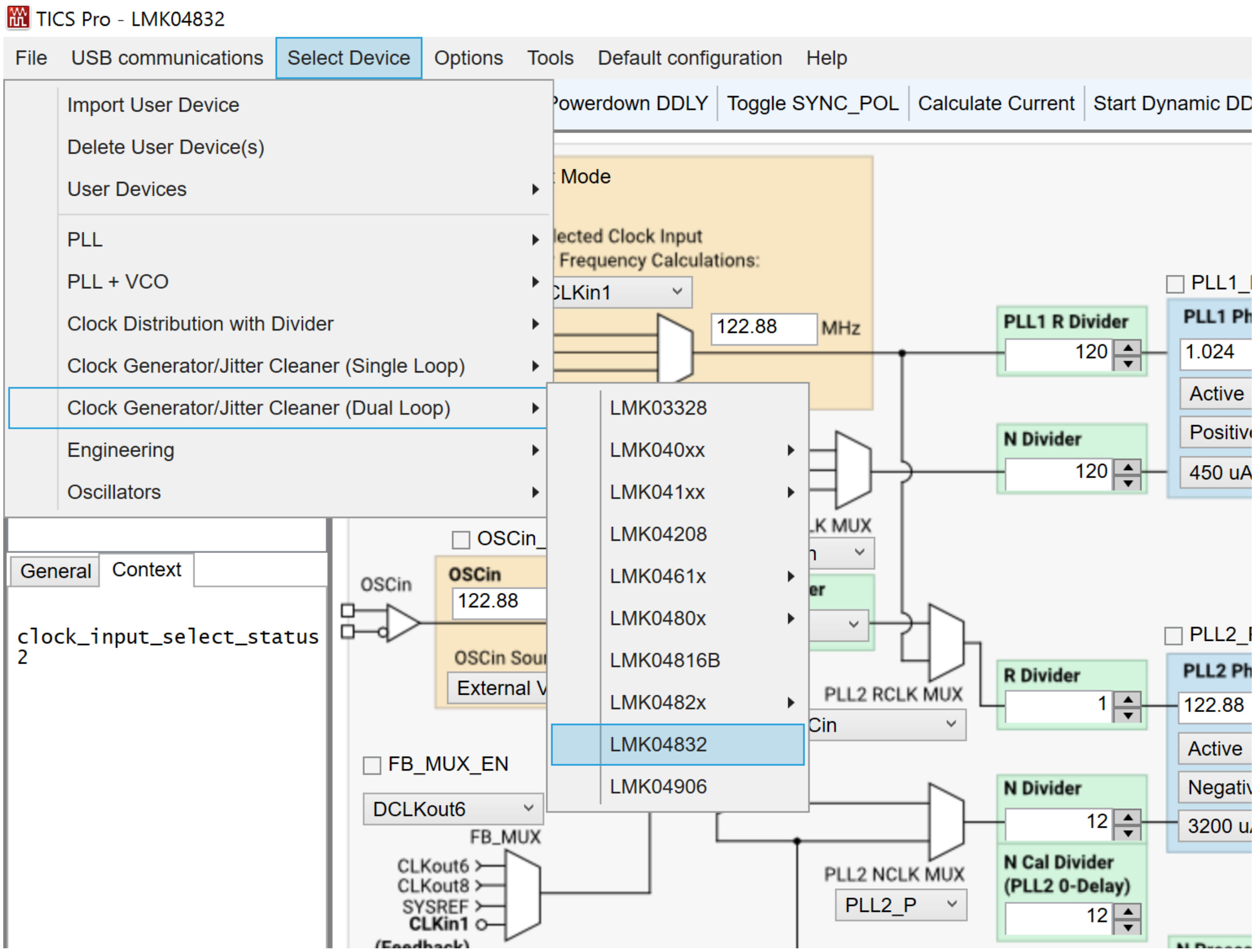

Figure 4. Selecting the LMK04832

5.3 Program the Device

To program press *Ctrl+L*.

Alternatively, click *USB communications* → *Write All Registers* from the menu to program the device to the current state of the register map to the device. *Ctrl+L* is the accelerator key assigned to the *Write All Registers* option and is very convenient.

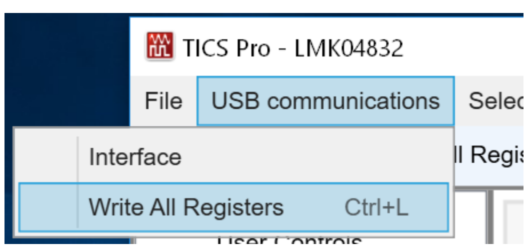

Figure 5. Loading the Device

Once the device has been initially loaded, TICS Pro will automatically program changed registers, so it is not necessary to reload the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the *Options* → *AutoUpdate*

Because a default mode will be restored in the next step, this step is not necessary, but it is included to emphasize the importance of pressing *Ctrl+L* to load the device at least once after starting TICS Pro, restoring a mode, or restoring a saved setup using the File menu.

See TICS Pro instructions located at http://www.ti.com/tool/ticspro-sw/.

5.4 Restoring a Default Mode

Click *Default configuration → CLKin1 122.88 MHz, OSCin 122.88 MHz, VCO1 2949.12 MHz*; then

Press *Ctrl+L*.

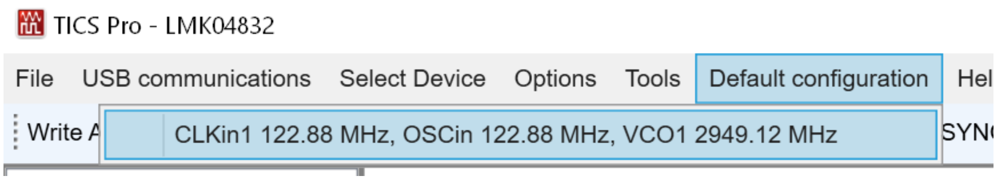

Figure 6. Setting the Default Mode for LMK04832

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when TICS Pro is closed, it remembers the last settings used for a particular device. Again, remember to press *Ctrl+L* as the first step after loading a default mode.

5.5 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded LED D10 and D11 must illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes PLL1_LD_MUX = *PLL1_DLD*, PLL2_LD_MUX = *PLL2_DLD*, and PLLX_LD_TYPE = Output (Push-Pull).

5.6 Enable Clock Outputs

The LMK04832 offers programmable clock output buffer formats, the evaluation board is shipped with pre-configured output terminations. Refer to Table 5 to see a list of the outputs what the output format the hardware is configured for out of the factory.

To measure Phase noise at one of the clock outputs, for example CLKout0:

1. Click on the **Clock Outputs** page, Section A.9
2. Uncheck *CLKoutX_Y_PD* in the Clock Output box to enable the channel,
3. Set the following as needed:
   a. For Device Clock:
      - DCLKX_Y_PD = 0 in Clock Mode Select box.
      - Set Bypass Div (DCLKX_Y_BYP) or Clock Divider (DCLK0_1_DIV) as desired for device clock frequency.
        – If bypass mode is set, CLKoutX must be set to a CML output format. Bypass mode is not available on CLKoutY.
        – If Clock Divider = 1, then DCLKX_Y_DCC must be set for clock output.
      - Phase of the device clock can be adjusted with:
        – Static Digital delay (DCLKX_Y_DDLY) after a SYNC. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up.
        – Dynamic Digital delay (DDLYdX_EN), then programming DDLYd_STEP_CNT. Digital Delay (DCLKX_Y_DDLY_PD) must be powered up. Press Send button at top right of Clock Outputs window to program the DDLYd_STEP_CNT field multiple times.
        – Half Step bit (DCLKX_Y_HS) if DCC & HS (DCLKX_Y_DCC) is set.
        – The Polarity bit (DCLKX_Y_POL)
      - Select the Device Clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 0 (Device Clock) as desired.

b. While the phase noise of a SYSREF Clock is typically not of concern, to configure an output for SYSREF:
   - SCLKX_Y_PD = 0 in Clock Mode Select box.
   - Phase of the SYSREF clock can be adjusted.
     – Local digital delay can be set with SCLKX_Y_DDLY.
     – Local analog delay can be set by enabling with ADLY_EN = 1 (SCLKX_Y_ADLY_EN) and then setting SCLKX_Y_ADLY to the desired time delay.
     – Global digital delay can be set with SYSREF_DDLY, but this delay change will take effect only after a SYNC.
   - Globally SYSREF output must be enabled. The necessary bits depend upon the type of SYSREF to be enabled. For a simple continuous SYSREF (not recommended in final application due to extra power consumption and crosstalk), set SYSREF_PD = 0, SYSREF_MUX = 0x03 (Continuous), and SYNC_DISSYSREF = 1.
   - Select the SYSREF clock for CLKoutX or CLKoutY with CLKout#_SRC_MUX = 1 (SYSREF) as desired.

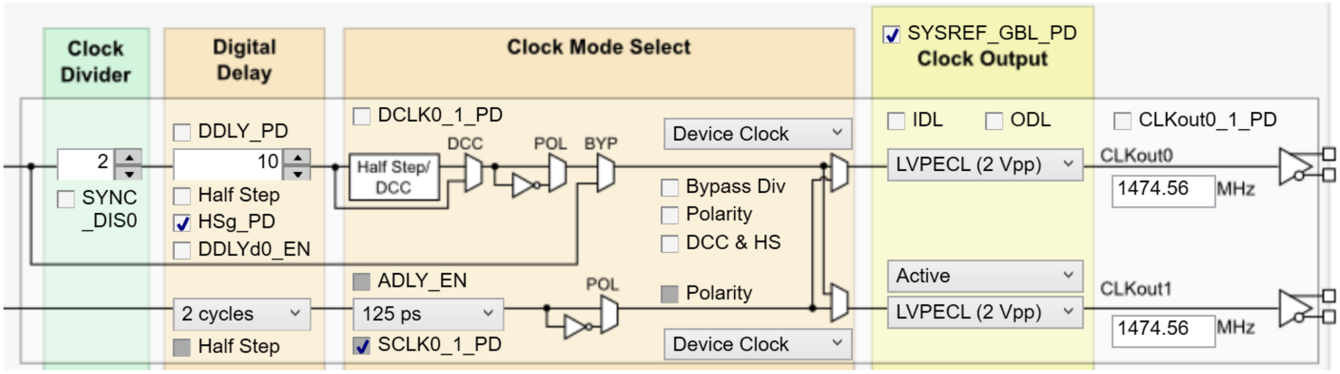

Figure 7. Setting Digital Delay, Clock Divider, Analog Delay, and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-Ω input as follows.
   a. For LVDS:
      i. A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   b. For LVPECL:
      I. A balun can be used, or
      II. One side of the LVPECL signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
   c. For HSDS:
      I. A balun (like ADT2-1T or high-quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   d. For CML:
      I. A balun can be used, or
      II. One side of the CML signal can be terminated with a 50-Ω load and the other side can be run single-ended to the instrument.
   e. For LVCMOS:
      I. Connect the LVCMOS signal to measurement equipment as desired. If an output of a pair is not used, TI recommends leaving the output floating close to the IC. Alternatively, place a 50-Ω termination at the end of an unused trace.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

6 Evaluation Board Inputs and Outputs

Table 5 contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable TICS Pro programming controls are noted for convenience.

Table 5. Description of Evaluation Board Inputs and Outputs

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="16">Clock Outputs
Populated:
CLKout0(J1),
CLKout0*(J2),
CLKout1(J3),
CLKout1*(J4),
CLKout2(J5),
CLKout2*(J6),
CLKout3(J7),
CLKout3*(J8),
CLKout4(J9),
CLKout4*(J10),
CLKout5(J11),
CLKout5*(J12),
CLKout8(J17),
CLKout8*(J18),
CLKout9(J19),
CLKout9*(J20)</td><td rowspan="17">Analog, Output</td><td colspan="2">Clock outputs with programmable output buffers.</td></tr>
<tr><td colspan="2">The output terminations by default on the evaluation board are shown here:</td></tr>
<tr><td>Clock Output Pair</td><td>Default Board Termination</td></tr>
<tr><td>CLKout0</td><td>LVPECL / LCPECL, 240 Ω</td></tr>
<tr><td>CLKout1</td><td>LVPECL / LCPECL, 240 Ω</td></tr>
<tr><td>CLKout2</td><td>LVPECL / LCPECL, 120 Ω</td></tr>
<tr><td>CLKout3</td><td>LVPECL / LCPECL, 120 Ω</td></tr>
<tr><td>CLKout4</td><td>CML, 68 nH - 20 Ω</td></tr>
<tr><td>CLKout5</td><td>50 Ω</td></tr>
<tr><td>CLKout6</td><td>CML, 68 nH - 20 Ω</td></tr>
<tr><td>CLKout7</td><td>50 Ω</td></tr>
<tr><td>CLKout8</td><td>LVDS / HSDS</td></tr>
<tr><td>CLKout9</td><td>LVDS / HSDS</td></tr>
<tr><td>CLKout10</td><td>LVDS / HSDS</td></tr>
<tr><td>CLKout11</td><td>LVDS / HSDS</td></tr>
<tr><td>CLKout12</td><td>LVPECL / LCPECL, 180 Ω</td></tr>
<tr><td>Not Populated:
CLKout6(J13),
CLKout6*(J14),
CLKout7(J15),
CLKout7*(J16),
CLKout10(J21),
CLKout10*(J22),
CLKout11(J23),
CLKout11*(J24),
CLKout12(J25),
CLKout12*(J26),
CLKout13(J27),
CLKout13*(J28)</td><td>CLKout13</td><td>LVPECL / LCPECL, 180 Ω</td></tr>
<tr><td></td><td></td><td colspan="2">Each CLKout pair has a programmable LVDS, LVPECL, LCPECL, HSDS, CML, or LVCMOS buffer. The output buffer type can be selected in TICS Pro in the Clock Outputs page Section A.9 through the CLKoutX_FMT control.
All clock outputs are AC-coupled to allow safe testing with RF test equipment.
If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is not recommended to use Norm/Norm or Inv/Inv mode.</td></tr>
<tr><td rowspan="5">OSCout
Populated:
OSCout_CLKin2(J29),
OSCout_CLKin2*(J30)</td><td rowspan="5">Analog, Output</td><td colspan="2">Buffered outputs of OSCin port.</td></tr>
<tr><td colspan="2">The output terminations on the evaluation board are shown here.:</td></tr>
<tr><td>OSC Output Pair</td><td>Default Board Termination</td></tr>
<tr><td>OSCout</td><td>LVPECL, 240 Ω</td></tr>
<tr><td colspan="2">OSCout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout buffer type can be selected in TICS Pro on the Clock Outputs page Section A.9 through the OSCout_FMT control.
OSCout is AC-coupled to allow safe testing with RF test equipment.
If OSCout is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state). Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is NOT recommended to use Norm/Norm or Inv/Inv mode.</td></tr>
<tr><td>Vcc</td><td>Power, Input</td><td colspan="2">Main power supply input for the evaluation board.
The LMK04832 contains internal voltage regulators for the VCO and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance.
On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See the schematics in section Section 8 for more details. The on board LDO is limited to 800 mA.</td></tr>
</table>

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

CONNECTOR NAME	SIGNAL TYPE, INPUT/OUTPUT	DESCRIPTION
Populated: J40	Power, Input	Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND). Apply power to either Vcc SMA or J40, but not both.
Clock Inputs Populated: CLKin0(J31), CLKin0*(J32), CLKin1*(J34) OSCout_CLKin2(J29), OSCout_CLKin2* (J30)	Analog, Input	**Reference Clock Inputs for PLL1 or PLL1 (CLKin0, 1, 2)** CLKin1*/FBCLKin*/Fin* is configured by default for a single-ended reference clock input from a 50-ohm source. The non-driven input pin (FBCLKin/CLKin1) is connected to GND with a 0.1 uF. CLKin0/CLKin0* is configured by default for a differential reference clock input from a 50-ohm source. CLKin1 is the default reference clock input selected in TICS Pro. If OSCout_CLKin2 is to be used as a CLKin2, then the PCB must be updated to operate as an input instead of an output. R35 can be populated to provide an external power supply for an external VCO at U2 or U3. R41, R50 can be populated to provide direct access to PLL2 Vtune node in the external VCO path.
Not Populated: CLKin1 (J33)		**Clock Distribution with CLKin1 or External VCO (Fin)** CLKin1 is shared for use as an RF Input (Fin) for Clock Distribution mode or for an external VCO mode.
		External Feedback Input (FBCLKin) for 0-Delay CLKin1 is shared for use as an external feedback clock input (FBCLKin) to PLL1 N or PLL2 N for 0-delay mode. See the LMK04832 Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop (SNAS688) for more details on using 0-delay mode with the evaluation board and the evaluation board software.
OSCin, PLL2 reference/PLL1 feedback Populated: OSCin* (J35) Not Populated: OSCin (J36)	Analog, Input	Feedback VCXO clock input to PLL1 and Reference clock input to PLL2. The single-ended output of the onboard VCXO (Y1/Y2/Y3) drives the OSCin* input of the device and the OSCin input of the device is connected to GND with 0.1 uF. VCXO Y1 and Y2 may also be used with differential VCXOs as is the default case for LMK04832EVM-002. An external VCXO may be optionally attached through these SMA connectors with minor modification to the components going to the OSCin/OSCin* pins of device. This is useful if the VCXO footprint does not accommodate the desired VCXO device or if the user desires to use the LMK04832 in single loop mode. A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF. Refer to the LMK04832 data sheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications (SNAS688). R74 allows connecting the OSCin port to provide external power to the VCXO if split rails are desired.
Test point: VTUNE1 (TP4)	Analog, Input	Tuning voltage output from the loop filter for PLL1. If an external VCXO is used, this tuning voltage can be connected to the voltage control pin of the external VCXO.
Test point: PLL2_VTUNE (TP2)	Analog, Input	Tuning voltage output from the loop filter for PLL2.
Test points: SDIO (TP13) SCK (TP12) CS* (TP14)	CMOS, Input/Output	10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04832.
Populated: SPI (J46)		10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04832. The programmable logic I/O signals accessible through this header include: RESET, SYNC, Status_LD1, Status_LD2, CLKin_SEL0, and CLKin_SEL1. These logic I/O signals also have dedicated SMAs and test points.
Test point: Status_LD1 (TP6)	CMOS, Input/Output	Programmable status output pin. By default, set to output the digital lock detect status signal for PLL1. In the default TICS Pro modes, LED D1 will illuminate green when PLL1 lock is detected by the LMK04832 (output is high) and turn off when lock is lost (output is low).
Test point: Status_LD2 (TP7)	CMOS, Input/Output	Programmable status output pin. By default, set to output the digital lock detect status signal for PLL2. In the default TICS Pro modes, LED D2 will illuminate green when PLL2 lock is detected by the LMK04832 (output is high) and turn off when lock is lost (output is low).

Table 5. Description of Evaluation Board Inputs and Outputs (continued)

<table>
<tr><th>CONNECTOR NAME</th><th>SIGNAL TYPE, INPUT/OUTPUT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="7">Test points:
CLKin0_SEL (TP5)
CLKin1_SEL (TP8)</td><td rowspan="7">CMOS,
Input/Output</td><td colspan="3">Programmable status I/O pins. By default, set as input pins for controlling input clock switching of CLKin0 and CLKin1.
To enable input clock switching, CLKin_SEL_AUTO_EN = 0, CLKin_SEL_PIN_EN = 1, CLKin_SEL_PIN_POL = 0, and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input).</td></tr>
<tr><td colspan="3">Input Clock Switching – Pin Select Mode
When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the Status_CLKinX pins select which clock input is active as follows:</td></tr>
<tr><td>CLKin_SEL1</td><td>CLKin_SEL0</td><td>Active Clock</td></tr>
<tr><td>0</td><td>0</td><td>CLKin0</td></tr>
<tr><td>0</td><td>1</td><td>CLKin1</td></tr>
<tr><td>1</td><td>0</td><td>CLKin2</td></tr>
<tr><td>1</td><td>1</td><td>Holdover</td></tr>
<tr><td>Test point:
SYNC (TP15)</td><td rowspan="2">CMOS,
Input/Output</td><td colspan="3">Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.
SYNC/SYSREF_REQ pin forces the SYSREF_MUX into SYSREF Continuous mode (0x03) when SYSREF_REQ_EN = 1.</td></tr>
<tr><td>Populated SMA:
SYNC (J45)</td><td colspan="3">SYNC/SYSREF_REQ pin can hold outputs in a low state, depending on system configuration. SYNC_POL adjusts for active low or active high control.
A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the SYNC/SYSREF page Section A.8 in TICS Pro.</td></tr>
<tr><td>Test point:
RESET (TP10)</td><td>CMOS,
Input/Output</td><td colspan="3">Programmable status I/O pin.</td></tr>
</table>

7 Recommended Test Equipment

Power Supply

The Power Supply must be a low-noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

TI recommends that an Agilent E5052 Signal Source Analyzer is used to measure phase noise and RMS jitter. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz, the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks AC performance, such as rise time or fall time, propagation delay, or skew, TI suggests using a real-time oscilloscope with 8+ GHz analog input bandwidth with 50-Ω inputs. To evaluate clock synchronization or phase alignment between multiple clock outputs, TI recommends using phase-matched, 50-Ω cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

8 Schematics

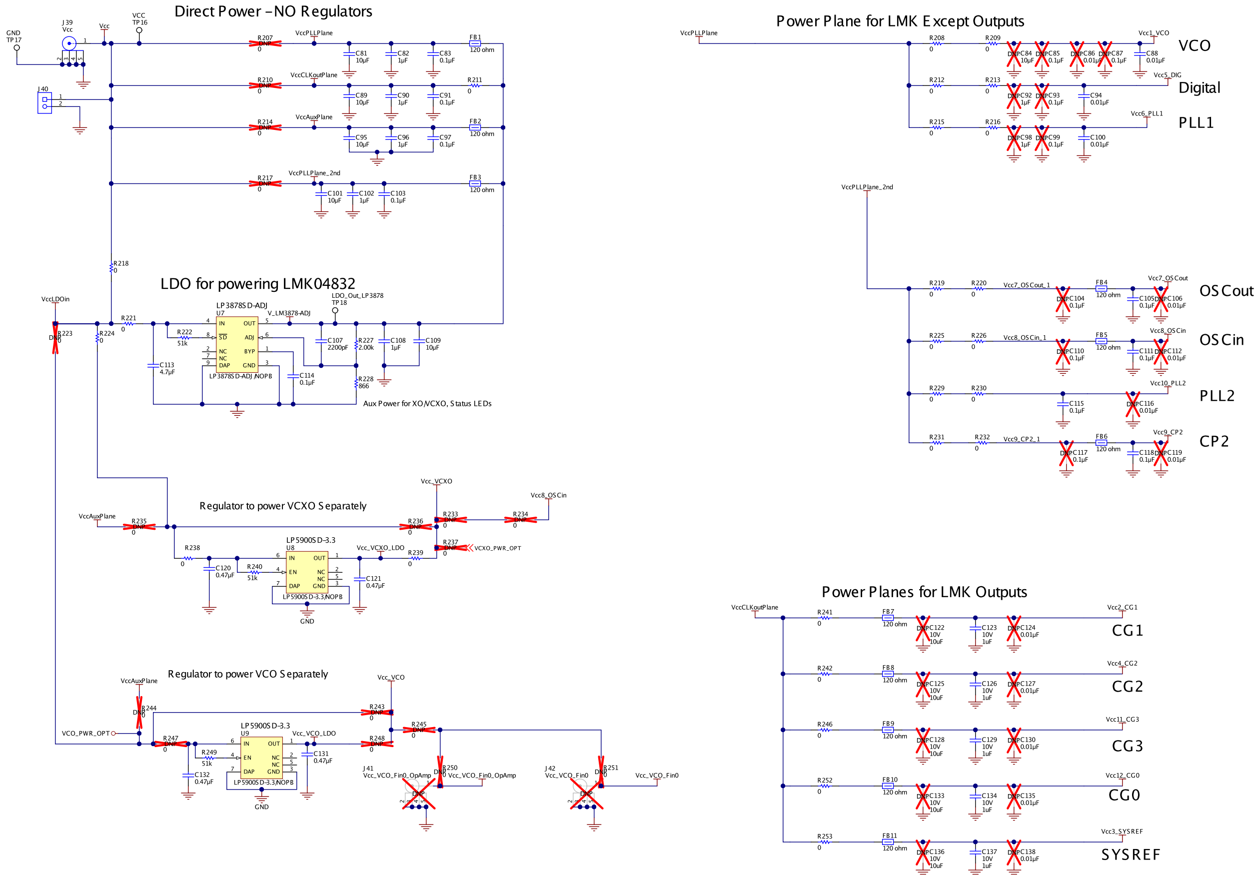

Figure 8. Schematic - Power Supply

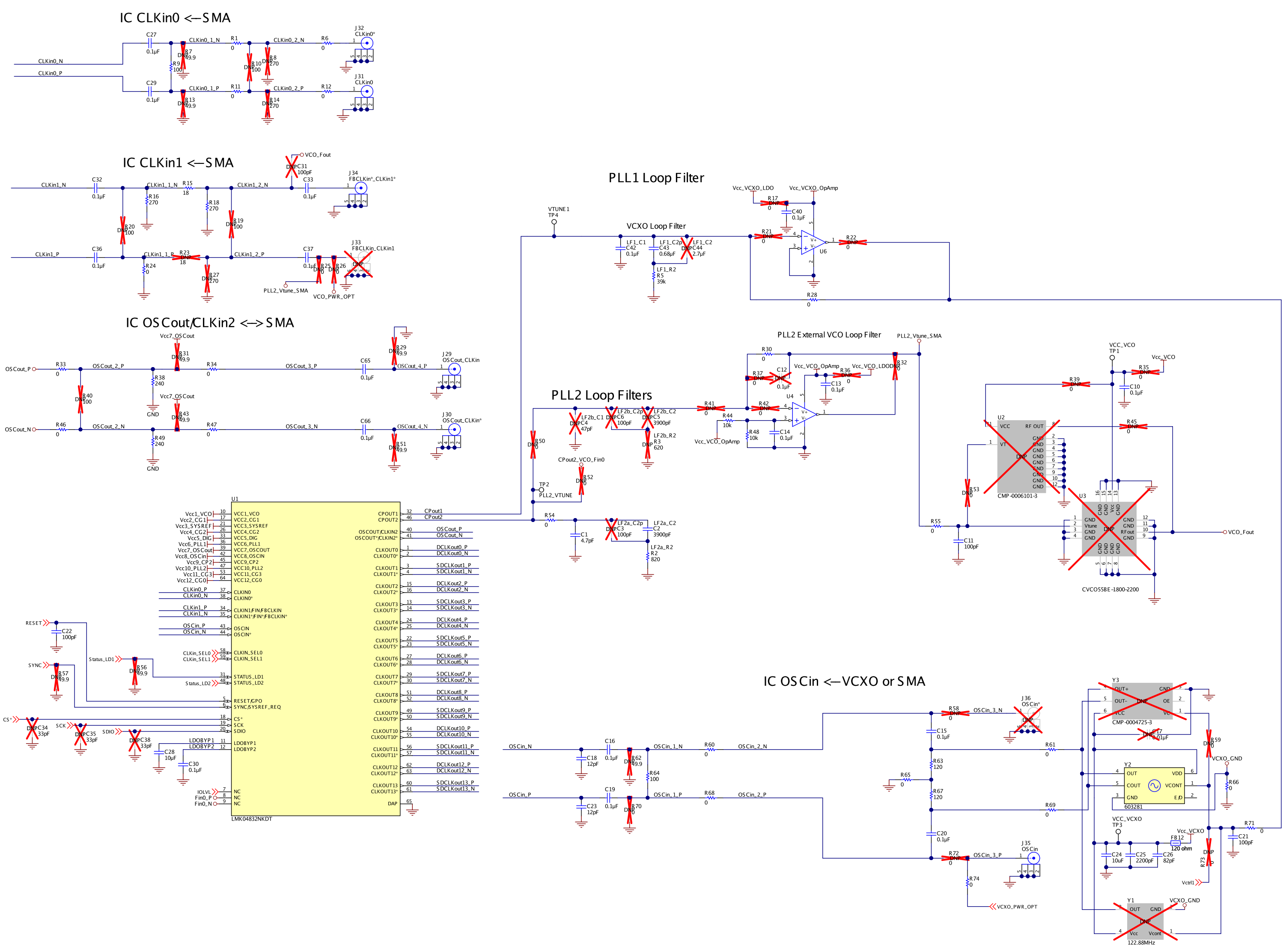

Figure 9. Schematic - LMK04832

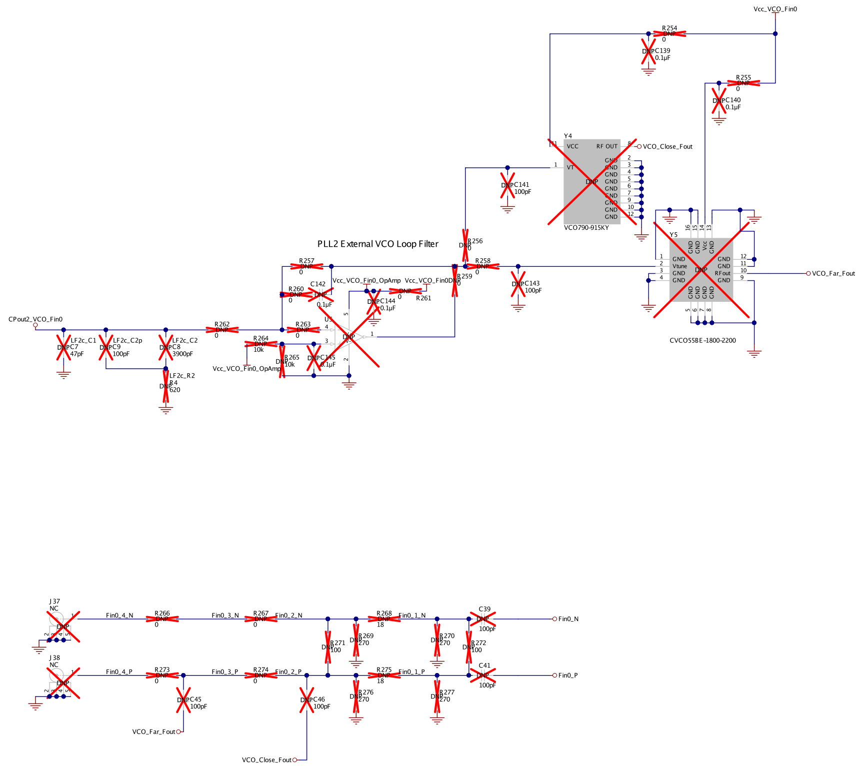

Figure 10. Schematic - PLL2 External Loop Filter and External VCO

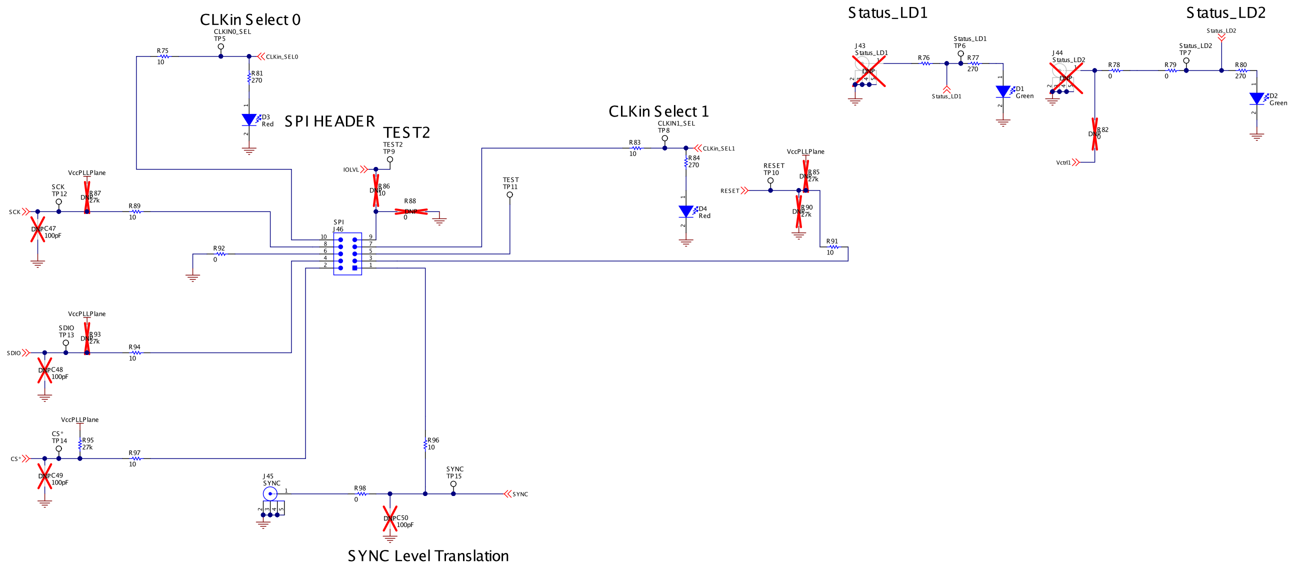

Figure 11. Schematic - Digital

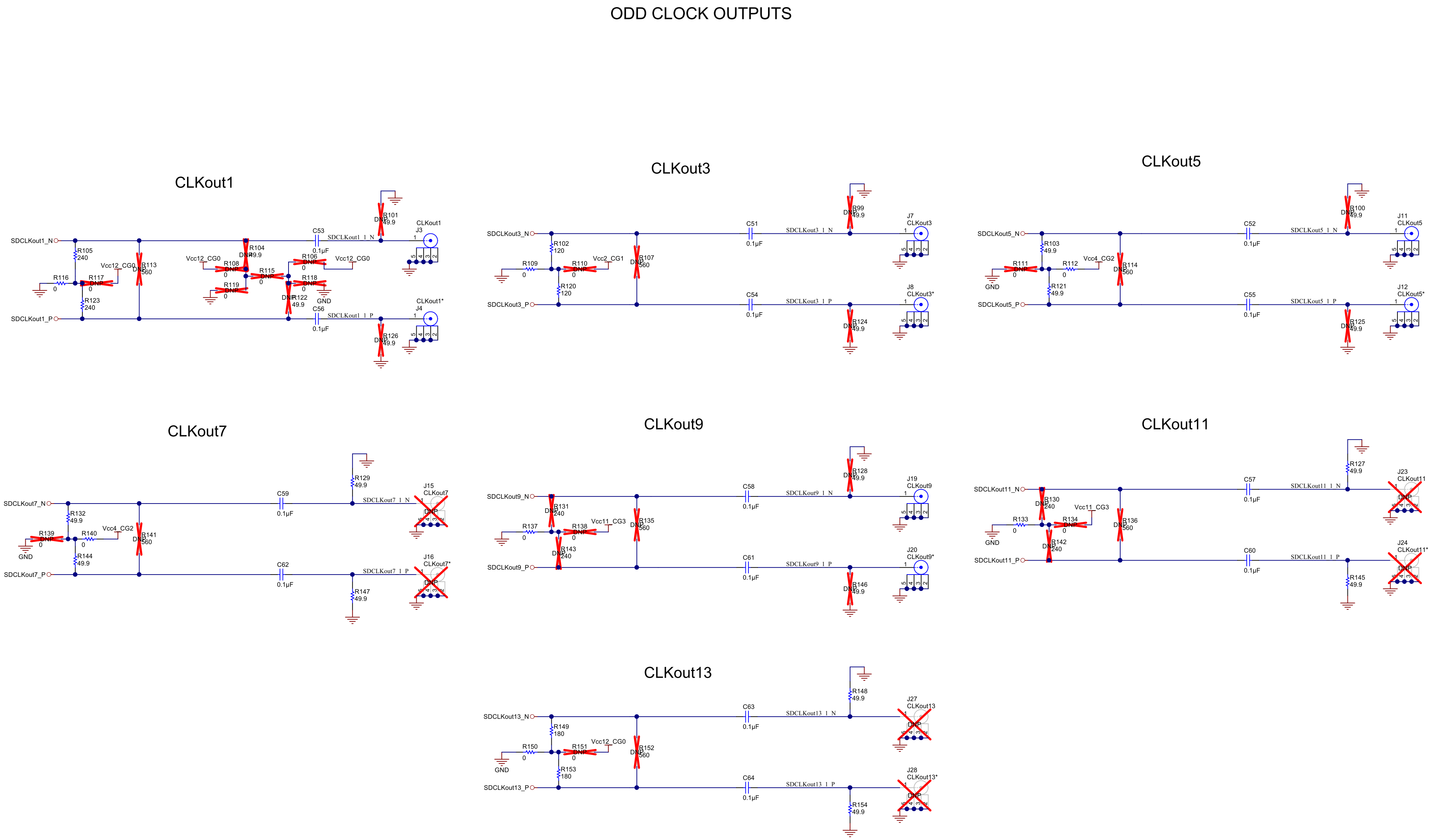

Figure 12. Schematic - Clock Outputs 1 of 2

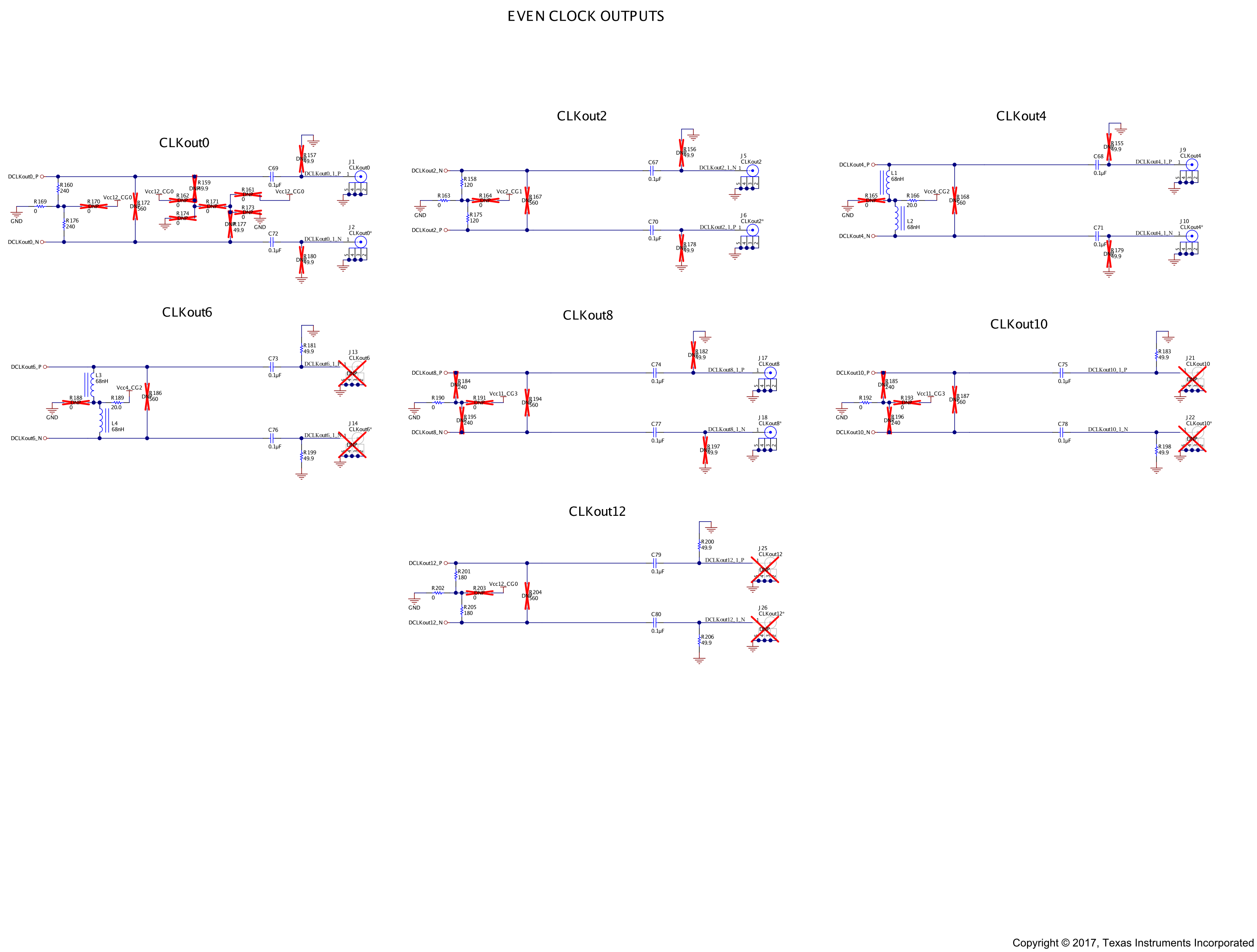

Figure 13. Schematic - Clock Outputs 2 of 2

9 Bill of Materials

Table 6. Bill of Materials

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
1	PCB	Printed Circuit Board	Any	HSDC004	1
2	C1	CAP, CERM, 4.7 pF, 50 V,+/-5%, C0G/NP0, 0603	AVX	06035A4R7CAT2A	1
3	C2	CAP, CERM, 3900 pF, 50 V, +/-10%, X7R, 0603	MuRata	GRM188R71H392KA01D	1
4	C10, C13, C14, C15, C40	CAP, CERM, 0.1 µF, 16 V, +/-10%, X7R, 0603	Kemet	C0603C104K4RACTU	5
5	C11, C21, C22	CAP, CERM, 100 pF, 50 V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	3
6	C16, C19, C27, C29, C32, C33, C36, C37, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80	CAP, CERM, 0.1 µF, 10 V, +/-10%, X5R, 0402	MuRata	GRM155R61A104KA01D	38
7	C18, C23	CAP, CERM, 12 pF, 50 V,+/-5%, C0G/NP0, 0402	MuRata	GRM1555C1H120JA01D	2
8	C20, C30, C42, C83, C91, C114	CAP, CERM, 0.1 µF, 25 V, +/-5%, X7R, 0603	Kemet	C0603C104J3RACTU	6
9	C24	CAP, CERM, 10 µF, 10 V, +/-20%, X5R, 0805	Kemet	C0805C106M8PACTU	1
10	C25, C107	CAP, CERM, 2200 pF, 50 V, +/-10%, X7R, 0603	Kemet	C0603C222K5RACTU	2
11	C26	CAP, CERM, 82 pF, 50 V, +/-10%, C0G/NP0, 0603	Kemet	C0603C820K5GACTU	1
12	C28, C81, C89, C95, C101, C109	CAP, CERM, 10 µF, 10 V, +/-10%, X5R, 0805	Kemet	C0805C106K8PACTU	6
13	C43	CAP, CERM, 0.68 µF, 10 V, +/-10%, X7R, 0603	MuRata	GRM188R71A684KA61D	1
14	C82, C90, C96, C102, C108	CAP, CERM, 1 µF, 10 V, +/-10%, X5R, 0603	Kemet	C0603C105K8PACTU	5
15	C88, C94, C100	CAP, CERM, 0.01 µF, 25 V, +/-10%, X7R, 0402	MuRata	GCM155R71E103KA37D	3
16	C97, C103	CAP, CERM, 0.1 µF, 25 V, +/-10%, X7R, 0603	Kemet	C0603C104K3RACTU	2
17	C105, C111, C115, C118	CAP, CERM, 0.1 µF, 25 V, +/-10%, X7R, 0402	MuRata	GRM155R71E104KE14D	4
18	C113	CAP, CERM, 4.7 µF, 10 V, +/-10%, X5R, 0603	Kemet	C0603C475K8PACTU	1
19	C120, C121, C131, C132	CAP, CERM, 0.47 µF, 16 V, +/-10%, X7R, 0603	Kemet	C0603C474K4RACTU	4
20	C123, C126, C129, C134, C137	CAP, CERM, 1 uF, 10 V,+/-20%, X5R, 0402	MuRata	GRM155R61A105ME15D	5
21	D1, D2	LED, Green, SMD	Lumex	SML-LX2832GC-TR	2
22	D3, D4	LED, Red, SMD	Lumex	SML-LX2832IC-TR	2
23	FB1, FB2, FB3, FB12	Ferrite Bead, 120 ohm @ 100 MHz, 0.5 A, 0603	MuRata	BLM18AG121SN1D	4
24	FB4, FB5, FB6, FB7, FB8, FB9, FB10, FB11	Ferrite Bead, 120 ohm @ 100 MHz, 0.4 A, 0402	TDK	MMZ1005Y121CT000	8

Table 6. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
25	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J17, J18, J19, J20, J29, J30, J31, J32, J34, J35, J45	Connector, End launch SMA, 50 ohm, SMT	Emerson Network Power	142-0701-851	23
26	J39	Connector, TH, SMA	Emerson Network Power	142-0701-201	1
27	J40	Terminal Block, 5.08mm, 2x1, TH	Molex	0395443002	1
28	J46	Header (shrouded), 100mil, 5x2, Gold, SMT	FCI	52601-S10-8LF	1
29	L1, L2, L3, L4	Inductor, Multilayer, Composite, 68 nH, 0.15 A, 1.5 ohm, AEC-Q200 Grade 1, SMD	TDK	MLK1005S68NJTD25	4
30	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1
31	R1, R6, R11, R12, R24, R33, R34, R46, R47, R60, R68, R74, R98, R109, R112, R116, R133, R137, R140, R150, R163, R169, R190, R192, R202	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	25
32	R2	RES, 820, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603820RJNEA	1
33	R5	RES, 39 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060339K0JNEA	1
34	R9, R64	RES, 100, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RFKED	2
35	R15	RES, 18, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040218R0JNED	1
36	R16, R18	RES, 270, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402270RJNED	2
37	R28, R30, R54, R55, R61, R65, R66, R69, R71, R78, R79, R92, R209, R211, R213, R216, R220, R221, R224, R226, R230, R232, R238, R239	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	24
38	R38, R49, R105, R123, R160, R176	RES, 240, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402240RJNED	6
39	R44, R48	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	2
40	R63, R67	RES, 120, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603120RJNEA	2
41	R75, R83, R89, R91, R94, R96, R97	RES, 10, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0JNEA	7
42	R76	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	1
43	R77, R80, R81, R84	RES, 270, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603270RJNEA	4
44	R95	RES, 27 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060327K0JNEA	1
45	R102, R120, R158, R175	RES, 120, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402120RJNED	4
46	R103, R121, R127, R129, R132, R144, R145, R147, R148, R154, R181, R183, R198, R199, R200, R206	RES, 49.9, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	16
47	R149, R153, R201, R205	RES, 180, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402180RJNED	4
48	R166, R189	RES, 20.0, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040220R0FKED	2
49	R208, R212, R215, R219, R225, R229, R231, R241, R242, R246, R252, R253	RES, 0, 5%, 0.75 W, AEC-Q200 Grade 0, 2010	Vishay-Dale	CRCW20100000Z0EF	12
50	R218	RES, 0, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA	1
51	R222, R240, R249	RES, 51 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060351K0JNEA	3
52	R227	RES, 2.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00FKEA	1

Table 6. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
53	R228	RES, 866, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603866RFKEA	1
54	S1, S2, S3, S4, S5, S6	HEX STANDOFF SPACER, 9.53 mm	Richco Plastics	TCBS-6-01	6
55	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18	Test Point, Miniature, White, TH	Keystone	5002	18
56	U1	Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs, NKD0064A (WQFN-64)	Texas Instruments	LMK04832NKDT	1
57	U4, U6	Precison Single Low Noise, Low 1/F corner Op Amp, DBV0005A	Texas Instruments	LMP7731MF/NOPB	2
58	U7	Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	Texas Instruments	LP3878SD-ADJ/NOPB	1
59	U8, U9	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	Texas Instruments	LP5900SD-3.3/NOPB	2
60	Y2	Ultra-Low Noise LVPECL VCXO with 162dBc/Hz NOISE Floor, SMD	Crystek Corporation	603281	1
61	C3, C47, C48, C49, C141, C143	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	0
62	C4, C7	CAP, CERM, 47 pF, 50 V,+/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H470JA01D	0
63	C5, C8	CAP, CERM, 3900 pF, 50 V,+/- 10%, X7R, 0603	MuRata	GRM188R71H392KA01D	0
64	C6, C9	CAP, CERM, 100 pF, 50 V,+/- 5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	0
65	C12, C139, C140, C142, C144, C145	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	Kemet	C0603C104K4RACTU	0
66	C17	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0402	TDK	C1005X7R1C103K050BA	0
67	C31, C39, C41, C45, C46, C50	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H101JA01D	0
68	C34, C35, C38	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0603	Kemet	C0603C330J5GACTU	0
69	C44	CAP, CERM, 2.7 µF, 10 V, +/- 10%, X5R, 0805	Kemet	C0805C275K8PACTU	0
70	C84	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	Kemet	C0603C106M9PACTU	0
71	C85, C87, C93, C99, C104, C110, C117	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0402	MuRata	GRM155R71E104KE14D	0
72	C86, C106, C112, C116, C119, C124, C127, C130, C135, C138	CAP, CERM, 0.01 µF, 25 V, +/- 10%, X7R, 0402	MuRata	GCM155R71E103KA37D	0
73	C92, C98	CAP, CERM, 1 µF, 10 V, +/- 10%, X5R, 0603	Kemet	C0603C105K8PACTU	0
74	C122, C125, C128, C133, C136	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0603	MuRata	GRM188Z71A106MA73D	0
75	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0

Table 6. Bill of Materials (continued)

ITEM	DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QUANTITY
76	J13, J14, J15, J16, J21, J22, J23, J24, J25, J26, J27, J28, J33, J36, J37, J38, J43, J44	Connector, End launch SMA, 50 ohm, SMT	Emerson Network Power	142-0701-851	0
77	J41, J42	Connector, TH, SMA	Emerson Network Power	142-0701-201	0
78	R3, R4	RES, 620, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603620RJNEA	0
79	R7, R13, R29, R31, R43, R51, R56, R57, R62, R99, R100, R101, R104, R122, R124, R125, R126, R128, R146, R155, R156, R157, R159, R177, R178, R179, R180, R182, R197	RES, 49.9, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040249R9FKED	0
80	R8, R14, R27, R269, R270, R276, R277	RES, 270, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402270RJNED	0
81	R10, R19, R20, R40, R271, R272	RES, 100, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402100RFKED	0
82	R17, R21, R22, R32, R35, R36, R37, R41, R42, R50, R52, R58, R59, R72, R82, R88, R207, R210, R214, R217, R223, R233, R235, R236, R237, R243, R244, R245, R247, R248, R250, R251, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0
83	R23, R268, R275	RES, 18, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040218R0JNED	0
84	R25, R26, R39, R45, R53, R70, R73, R106, R108, R110, R111, R115, R117, R118, R119, R134, R138, R139, R151, R161, R162, R164, R165, R170, R171, R173, R174, R188, R191, R193, R203, R234, R266, R267, R273, R274	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0
85	R85, R87, R90, R93	RES, 27 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060327K0JNEA	0
86	R86	RES, 10, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310R0JNEA	0
87	R107, R113, R114, R135, R136, R141, R152, R167, R168, R172, R186, R187, R194, R204	RES, 560, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402560RJNED	0
88	R130, R131, R142, R143, R184, R185, R195, R196	RES, 240, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402240RJNED	0
89	R264, R265	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0
90	U2, Y4	VCO, 800 to 1030 MHz, SMD	RF Micro Devices	VCO790-915KY	0
91	U3, Y5	VCO, 1800-2200MHz, SMD	Crystek Corporation	CVCO55BE-1800-2200	0
92	U5	Precison Single Low Noise, Low 1/F corner Op Amp, DBV0005A	Texas Instruments	LMP7731MF/NOPB	0
93	Y1	VCXO, CMOS 122.880 MHz, 3.3V, SMD	Crystek Corporation	CVHD-950-122.880	0
94	Y3	OSC, 122.88 MHz, 3.3 Vdc, SMD	Epson	VG-4513CB-122.8800M-GFCT3	0

TICS Pro Usage

TICS Pro is used to program the evaluation board with the USB2ANY interface adapter. TICS Pro can also be used to generate register maps for programming the device and current consumption estimates. This appendix outlines the basic purpose and usage of each page. TICS Pro is available for download at http://www.ti.com/tool/ticspro-sw.

A.1 Communication Setup

The Communication Setup window allows the USB2ANY or DemoMode to be selected. In case multiple evaluation boards are to be connected and run with multiple instances of TICS Pro, the drop-down box will allow specific USB2ANY devices to be selected. Pressing the identify button will identify which USB2ANY is currently selected. Devices used by other instances of TICS Pro will not display in this list.

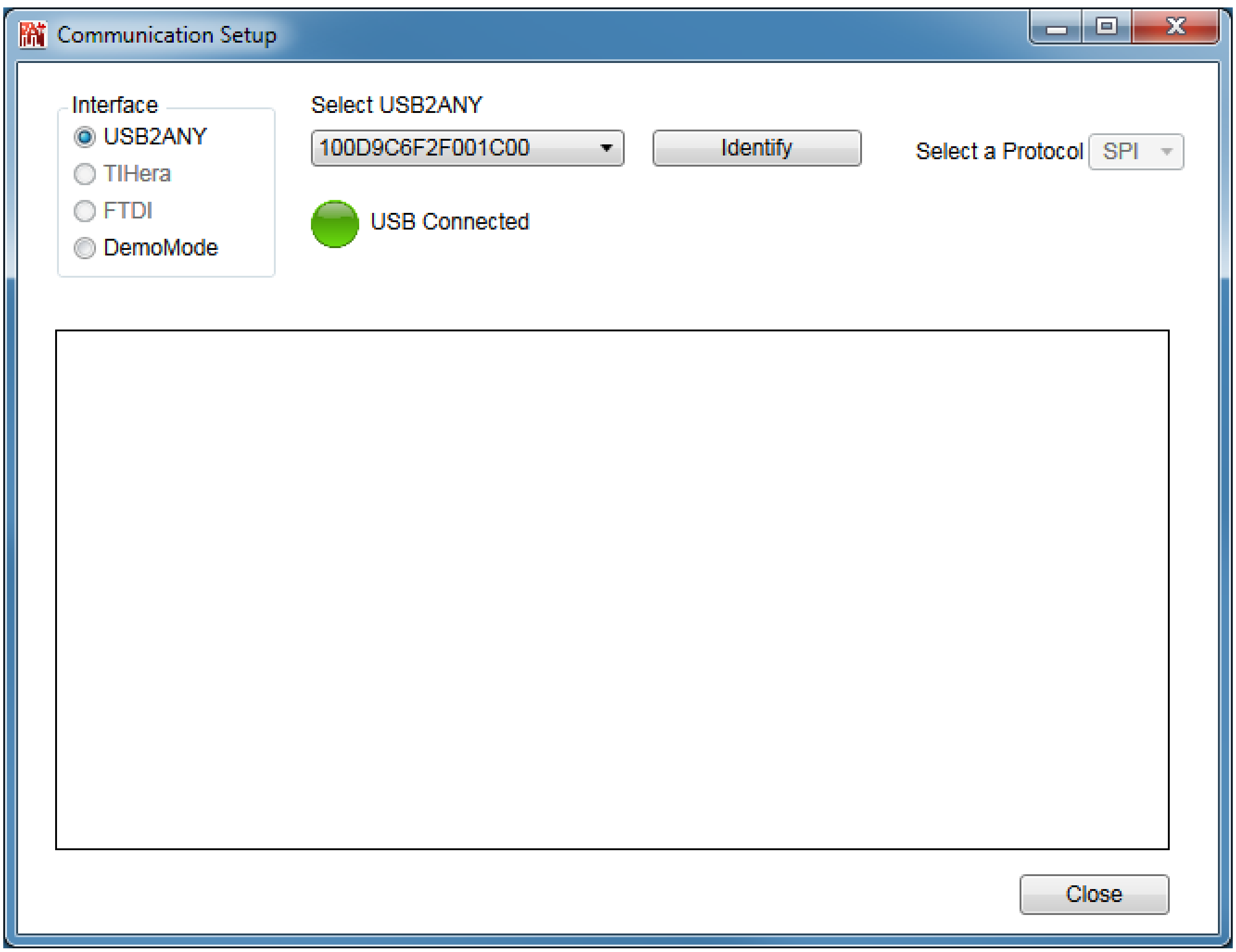

Figure 14. TICS Pro - Communication Setup Window

A.2 User Controls

The **User Controls** page has controls typically not included on one of the other dedicated pages.

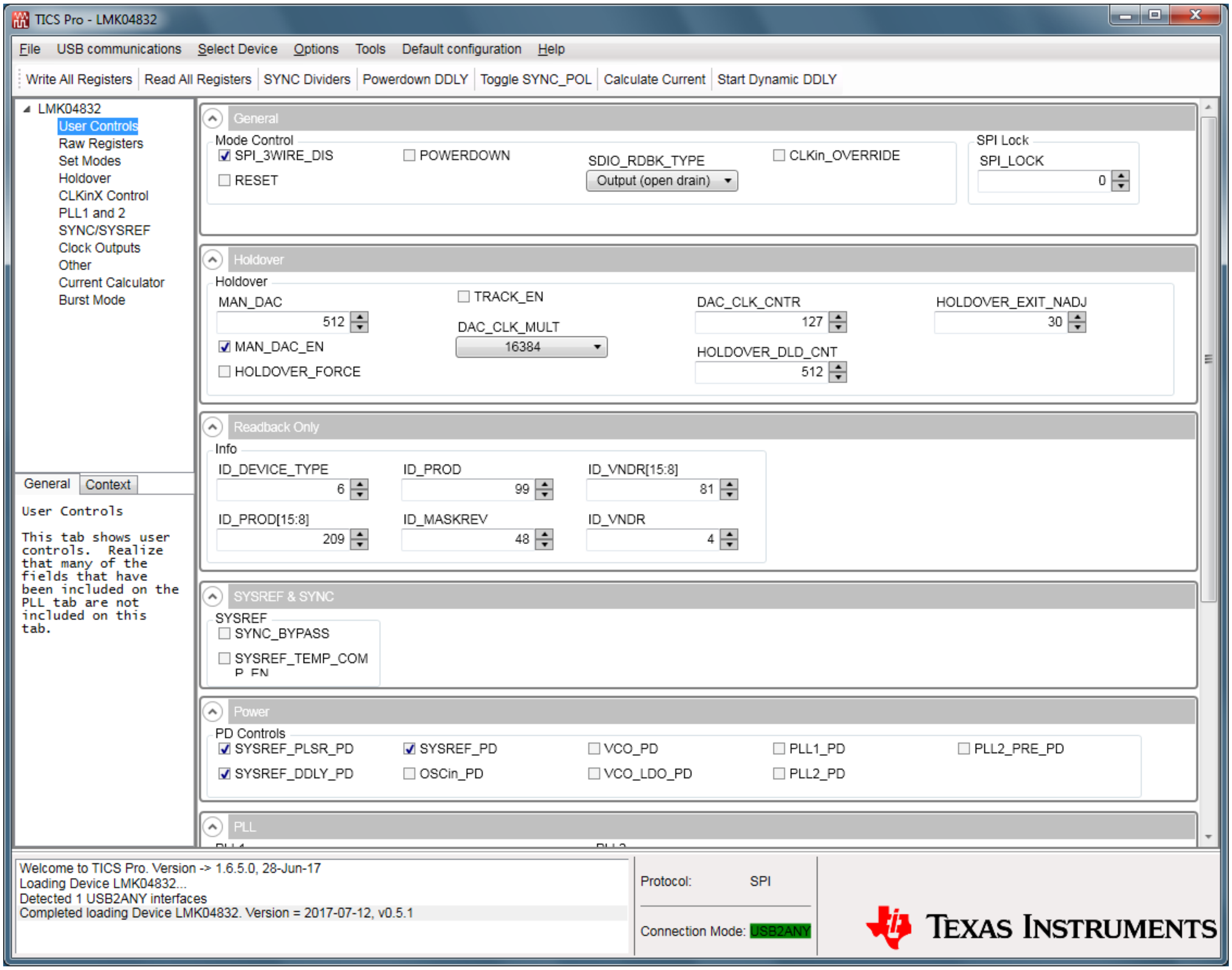

Figure 15. TICS Pro - User Controls Page

A.3 Raw Registers Page

The **Raw Register** page displays the register map including address. The address bits have the shaded background and are not editable. The unshaded bits are the data bits. This register map may be directly manipulated by clicking into the bit field, moving around with the arrow keys, and typing 1 or 0 to change a bit.

All registers may be read or written in addition to individual registers. For individual register read or write, the active register is highlighted in the list of registers and displayed in the top right. An individual register or field may be read back by entering the name into the bottom right and clicking the *Read* button.

Register maps may be exported, but also imported. The import format may simply be the address and register data in hex format as illustrated in the address/value column, one register to a line.

NOTE: Use the Export Register Map to create a text file with the register values for simple re-use of the register configuration.

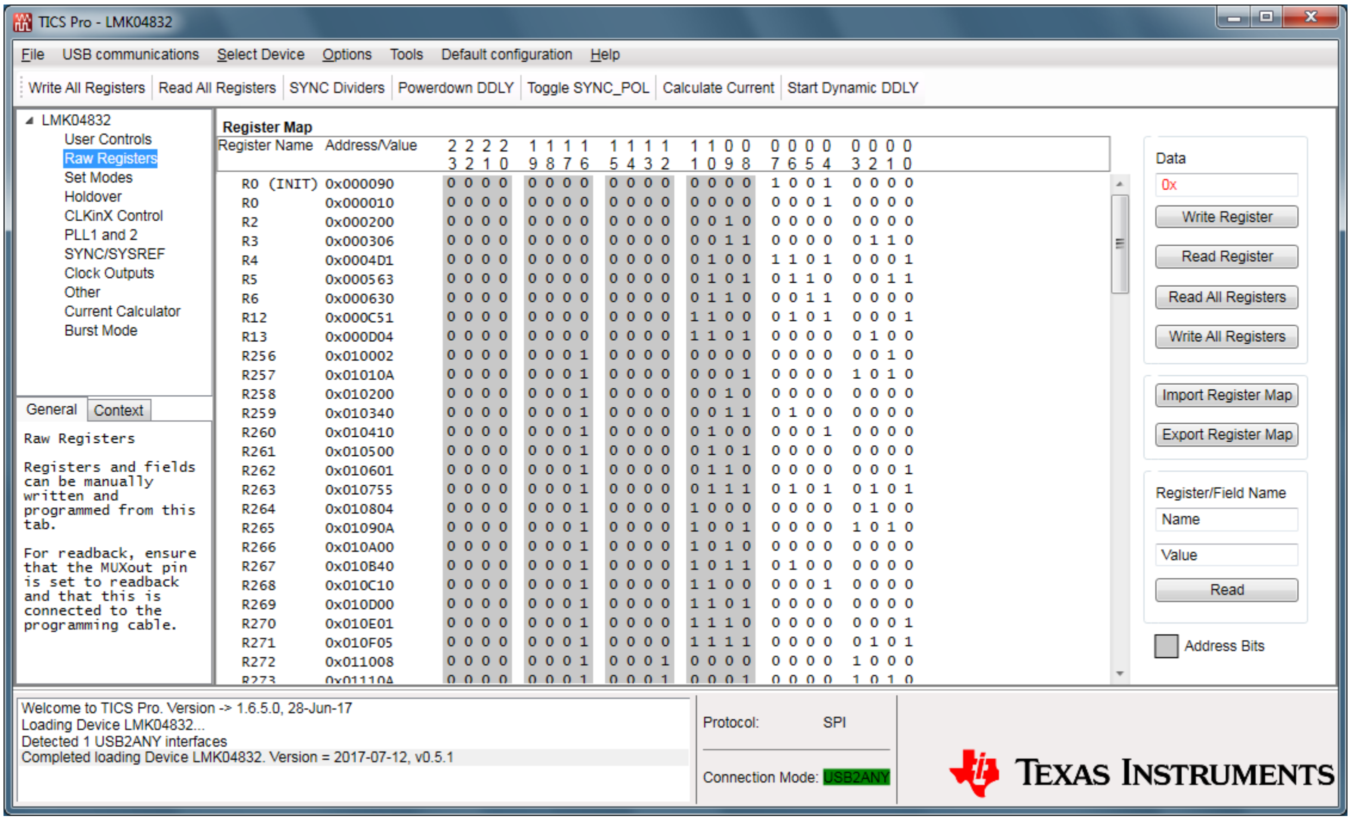

Figure 16. TICS Pro - Raw Registers Page

A.4 Set Modes Page

The **Set Modes** page allows the user to quickly configure the LMK04832 into a desired mode. If the LMK04832 is already in the desired mode, or several registers are already programmed as needed, the log will not display any or many register writes.

The top LMK04832 modes section allows the user to set high level usage profiles to allow the device to operate in dual loop, single loop, or distribution mode.

The bottom LMK04832 sub-modes section allows further JESD204B configuration, 0-delay configuration, or clock input configuration which may apply for many of the LMK04832 modes of operation.

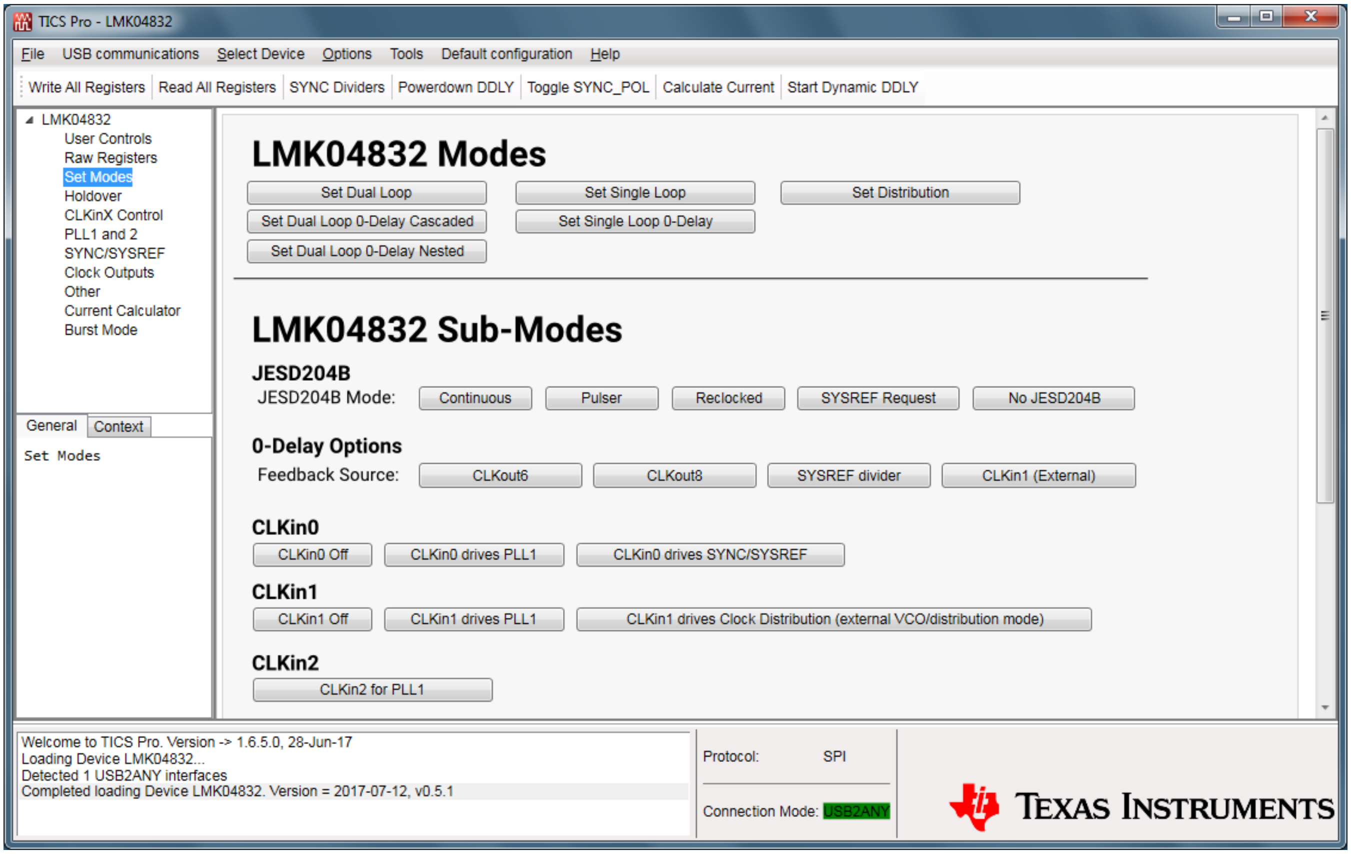

Figure 17. TICS Pro - Set Modes Page

A.5 Holdover Page

The **Holdover** page contains many registers pertaining to how the device will enter and exit holdover. To enable holdover and LOS detect for entry and exit of holdover:

- Set HOLDOVER_EN = 1 (checked)
- Set HOLDOVER_EXIT_MODE combo box to 0x00 (Exit based on LOS)
- Set LOS_EN = 1 (checked)
- Set LOS_TIMEOUT combo box to the LOS frequency threshold as desired. For example, if 200 MHz is set as the frequency threshold, the input must be above approximately 200 MHz to lock, otherwise PLL1 will enter holdover. If holdover is not enabled, PLL1 will be prevented from locking if the input frequency is less than the threshold frequency and LOS is enabled.

In addition to the above steps, auto clock selection mode must be used to allow the LMK04832 to automatically switch to holdover when enabled clocks for auto switching (CLKinX_EN) are lost.

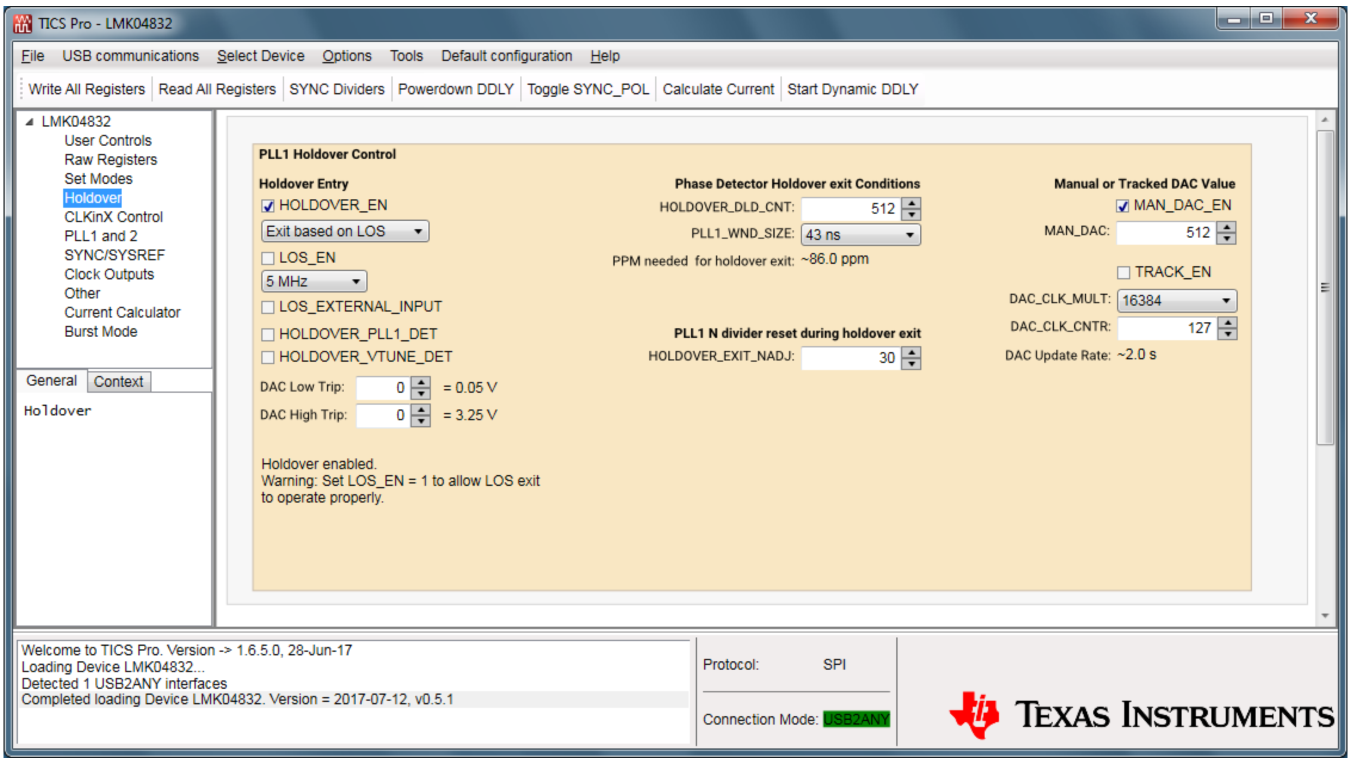

Figure 18. TICS Pro - Holdover Page

A.6 CLKinX Control Page

The **CLKinX Control** page allows entry of the input frequency at the different CLKinX pins, the mode by which the active CLKinX is selected, where the CLKinX inputs are routed to.

Also on this page are controls to reset the PLL1 R or PLL2 N divider.

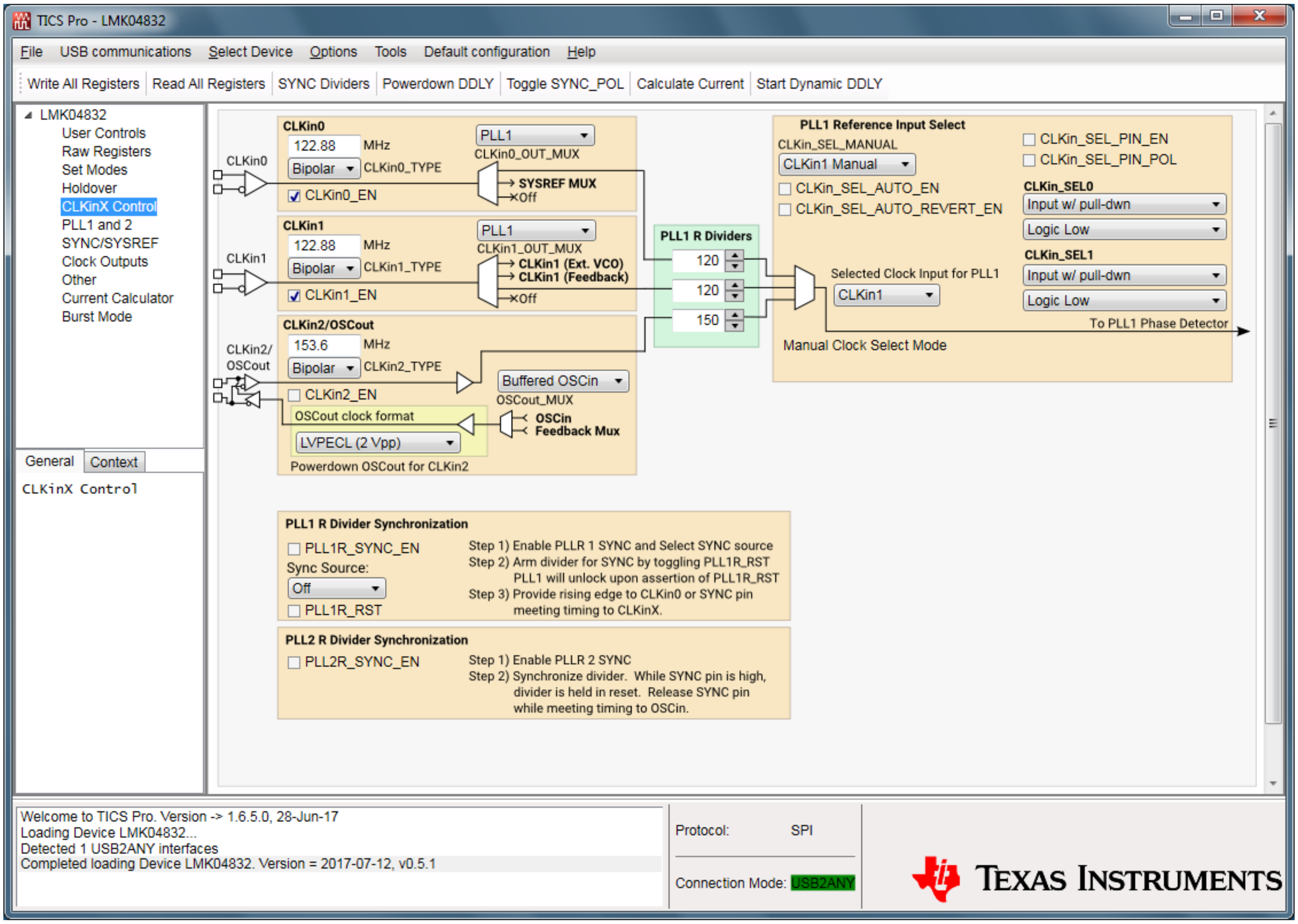

Figure 19. TICS Pro - CLKinX Control Page

A.7 PLL1 and 2 Page

The **PLL1 and PLL2** page illustrates the frequencies that the PLL1 and PLL2 operate at. In distribution mode, the CLKin1 frequency will directly be connected to the VCO/clock distribution path frequency. In addition to the basic PLL dividers and controls, when the PLLX_NCLK_MUX selects the feedback mux as a source, 0-delay modes are achieved. When enabling 0-delay red text will help guide the user through properly setting up 0-delay mode.

When using dual PLL mode, the OSCin Source combo box can be set to *External VCXO* which links the OSCin frequency with the external VCXO frequency. When using single PLL2 mode, the OSCin Source combo box can be set to *Independent* to allow the OSCin frequency to be unlinked from the external VCXO frequency.

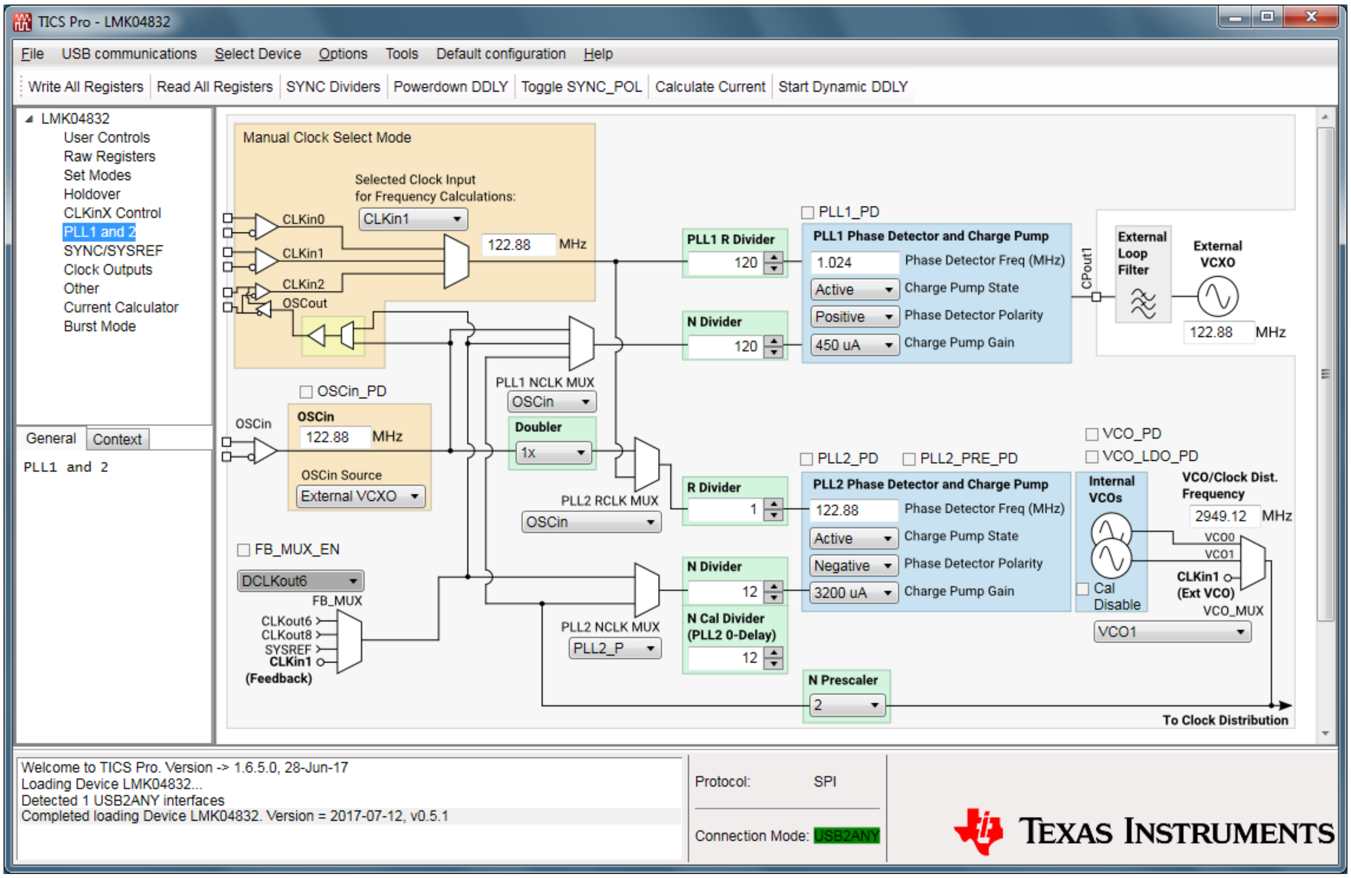

Figure 20. TICS Pro - PLL1 and 2 Page

A.8 SYNC / SYSREF Page

The **SYNC / SYSREF** page allows some mode set buttons for JESD204B features. The SYNC dividers button will stop all SYNC inputs, set normal SYNC mode, enable all dividers for SYNC, issue a SYNC by toggling SYNC_POL, set all dividers to ignore SYNC, then return any other changed parameter to its original state. This is a nice feature to ensure all outputs are synchronized together or to be run after changing the digital delay value which requires a SYNC to update. This functionality is also available on any other page through the toolbar as *SYNC Dividers*.

NOTE: To use SYNC or SYSREF, ensure that SYNC_EN = 1. To use SYSREF in continuous, pulser, or reclocked modes, be sure SYSREF_PD = 0.

The SCLKX_Y_DIS_MODE bits allow the clock outputs to be disabled or set to a low state. Because values 1 and 2 are only conditionally set by the SYSREF_GBL_PD bit, it is possible to power up/down several SYSREF outputs by programming only one register. When changing between 0x00 (Active) and (0x01) Conditional Low, keeping the SYSREF_CLR = 1 during transition will prevent glitch pulses from the SYSREF output.

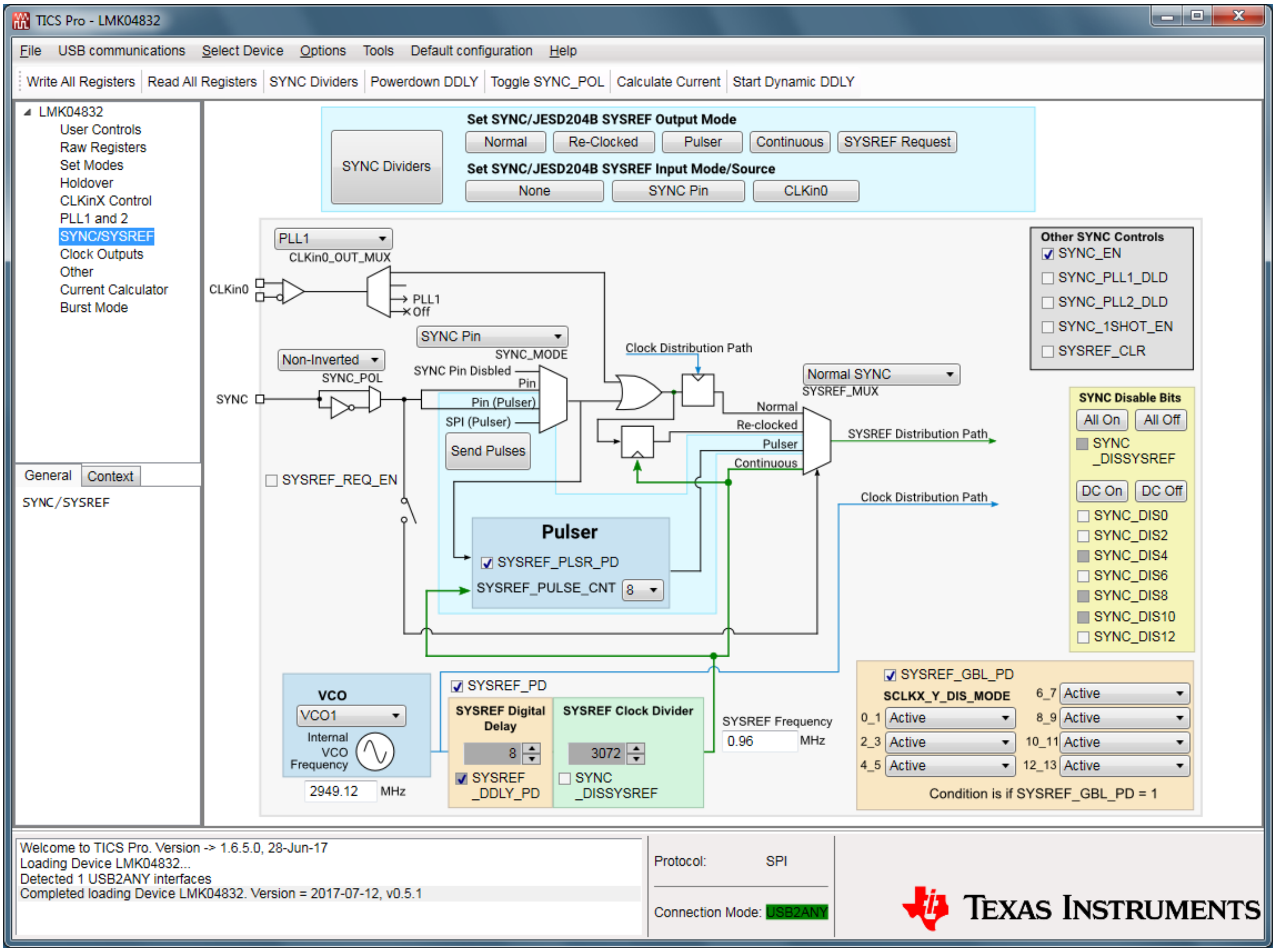

Figure 21. TICS Pro - SYNC / SYSREF Page

A.9 Clock Outputs Page

The **Clock Outputs** page allows control of all the clock outputs format and other options relating to the clock outputs. All the clock outputs are paired and allow two device clocks, two SYSREF clocks, or one of each. The naming convention uses X_Y for controls which can impact both CLKoutX (even clock) and CLKoutY (odd clock), X for controls impacting only CLKoutX and Y for controls impacting only CLKoutY.

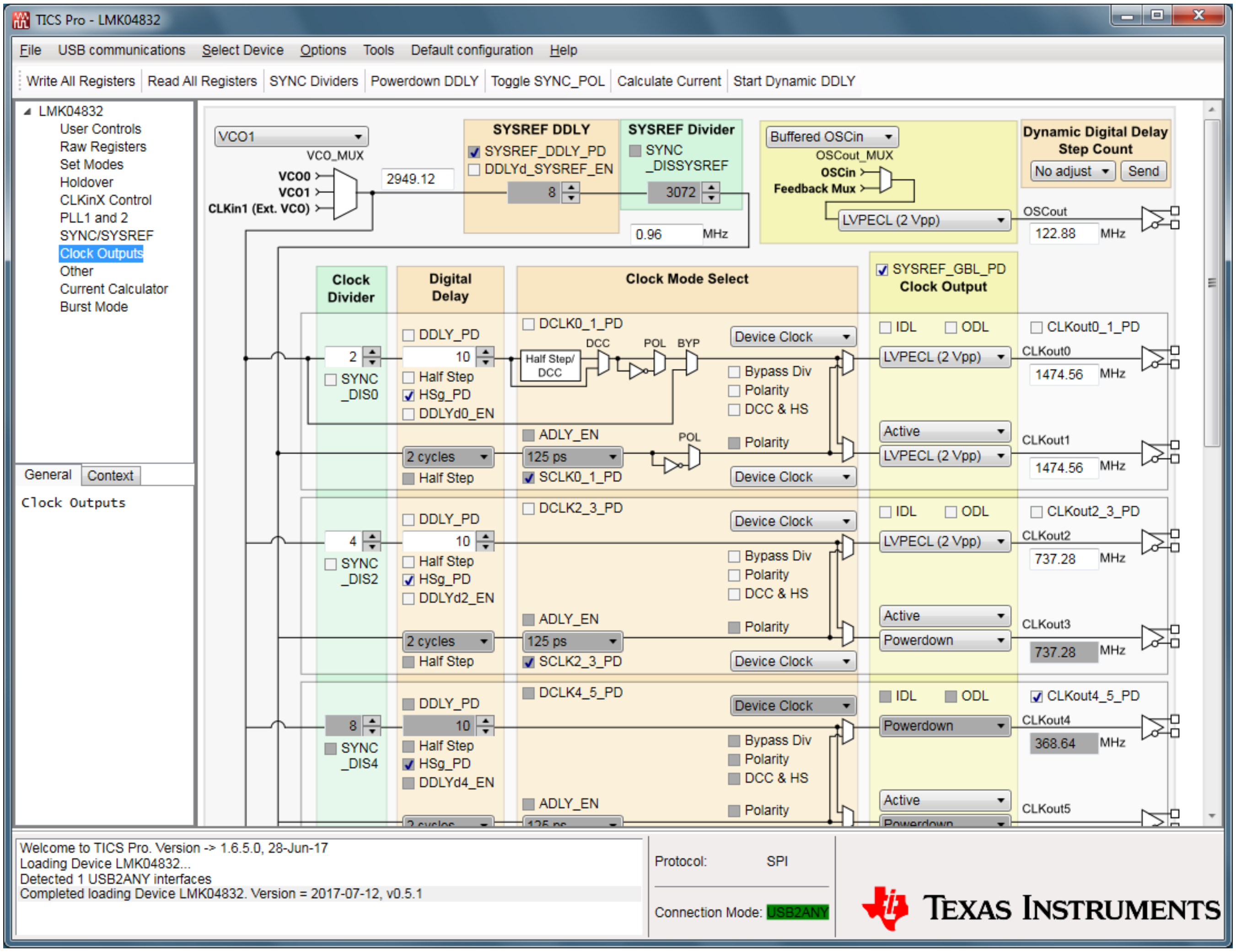

Figure 22. TICS Pro - Clock Outputs Page

A.10 Other Page

The **Other** page contains some registers to control the GPIO pins of the LMK04832. Each pin has two fields, the first is the _TYPE field which allows the input or output mode of the pin to be defined. The second is the _MUX field which, when set for output, controls what the pin will output.

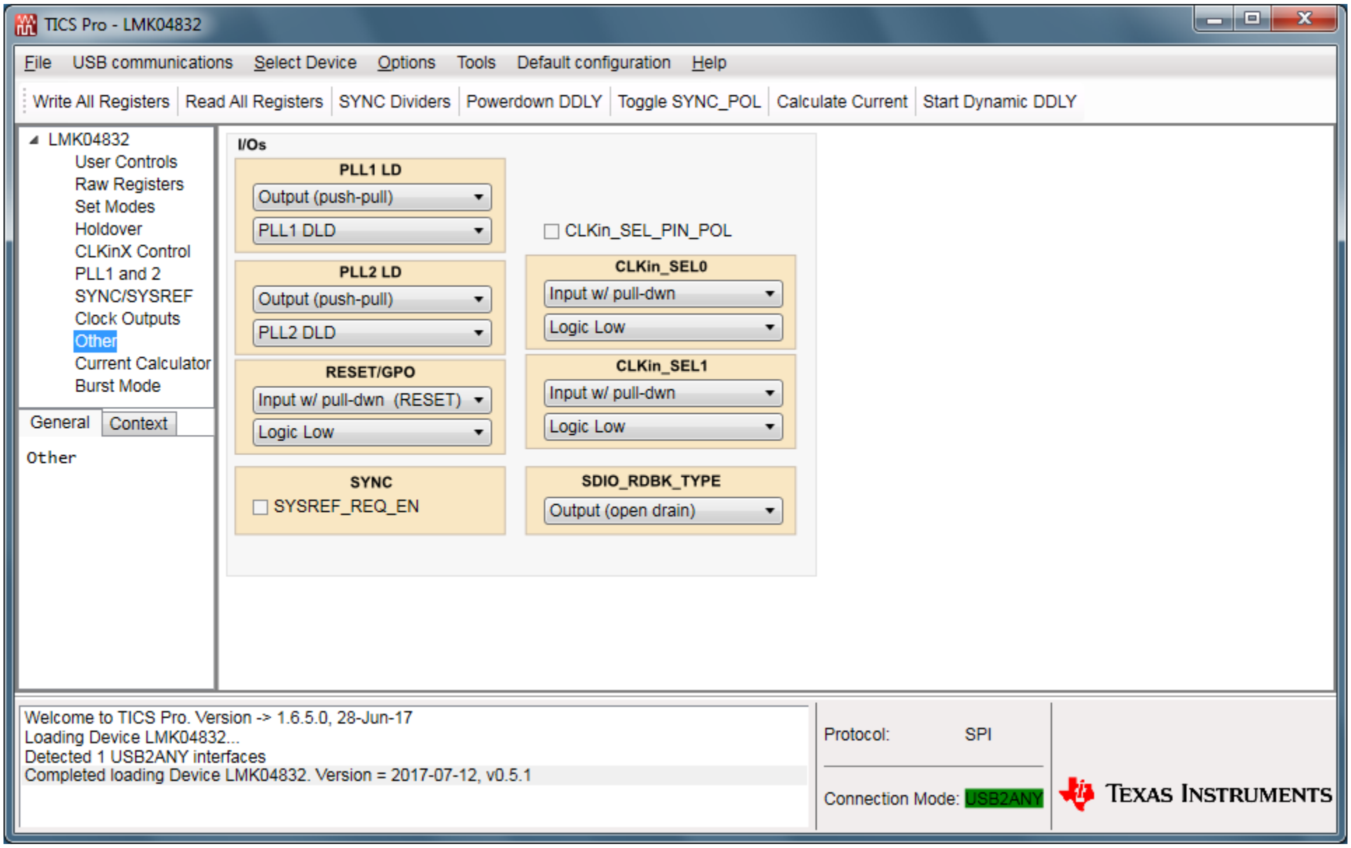

Figure 23. TICS Pro - Other Page

A.11 Current Calculator Page

The **Current Calculator** page allows the user to also set the same output format register as in the **Clock Outputs** page, but also set the hardware configuration connected to that output. With this information, along with the other programmed fields a current calculation estimate is made for the LMK04832. Also, power dissipated externally in emitter resistors, and so forth, is estimated and subtracted from the total power to find the IC Power the device must dissipate.

In the lower left is some boxes to account for extra I_{CC} due to LEDs, VCXO, or other.

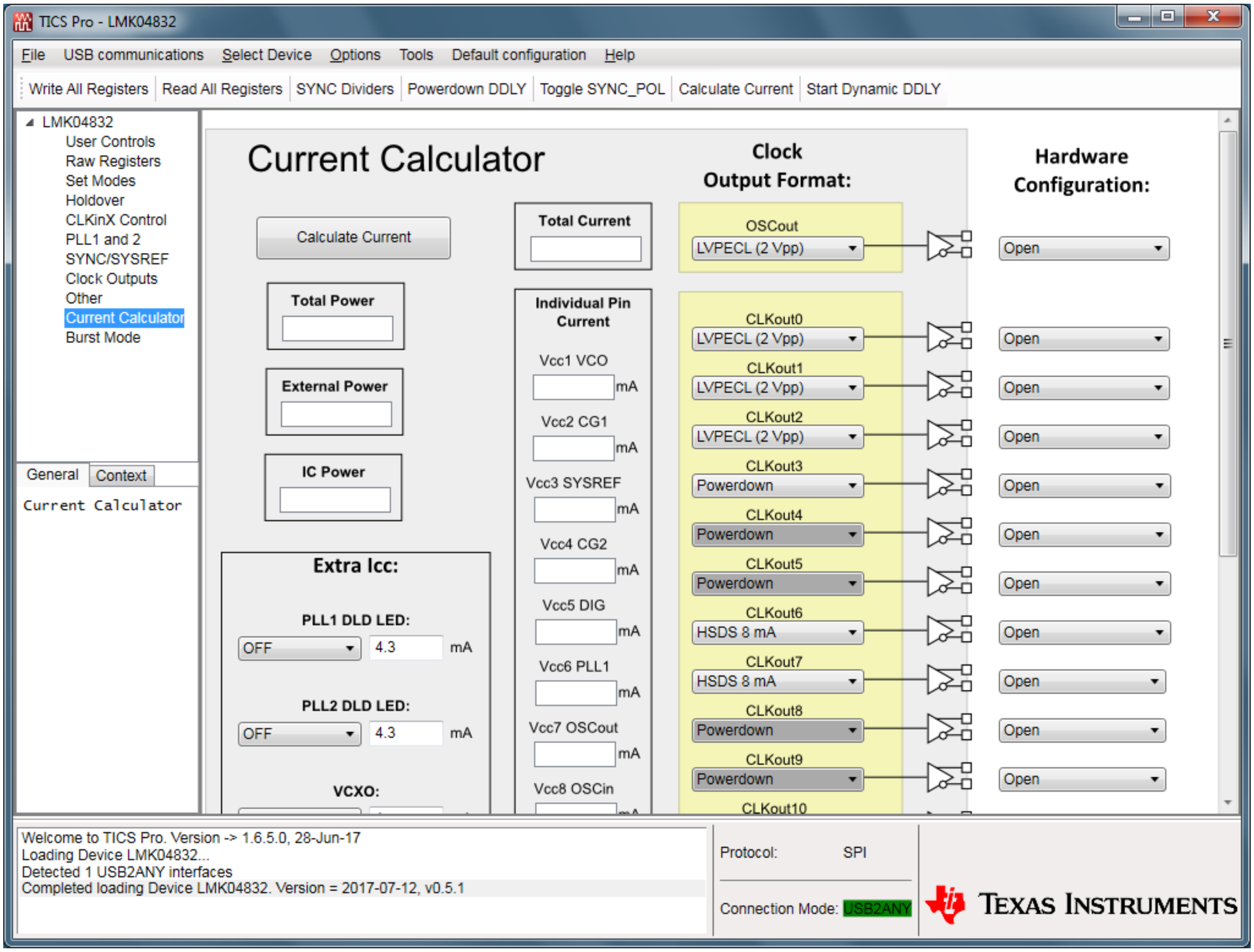

Figure 24. TICS Pro - Current Calculator Page

A.12 Burst Page

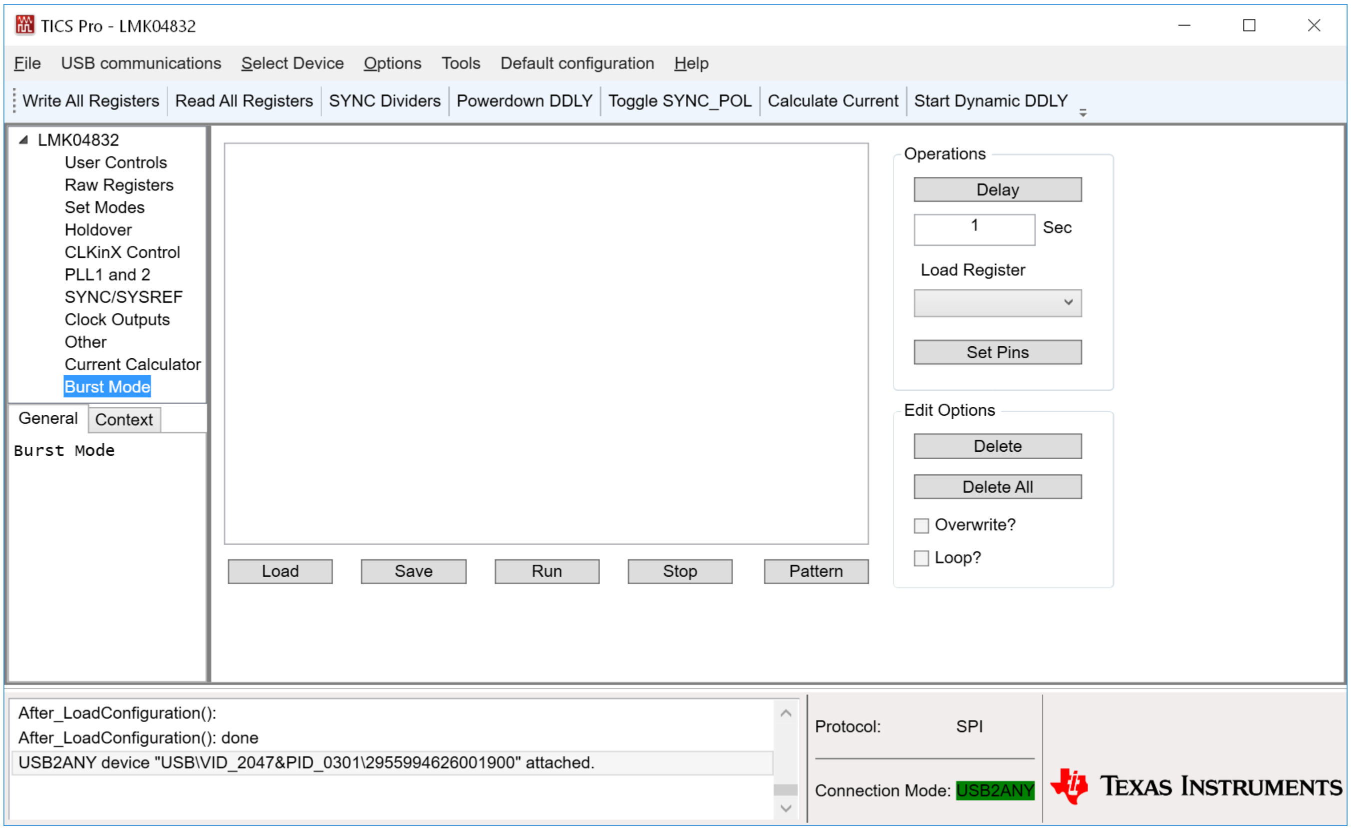

Figure 25. TICS Pro - Burst Page

The **Burst** page allows the user to program sequences of register programming or pin control.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2017) to A Revision **Page**

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   3.1 *United States*

   3.1.1 *Notice applicable to EVMs not FCC-Approved:*

   FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

   3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

   CAUTION

   This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

   Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

   FCC Interference Statement for Class A EVM devices

   NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。 http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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