Application Note

Eye Scan With TI PCI-Express Gen5.0 Redrivers

David Waier

ABSTRACT

This application note describes the Texas Instruments PCI Express Gen5.0 linear redriver family's Eye Scan feature functionality. The intended audience for this document includes hardware engineers using Texas Instruments PCI-Express Gen5.0 linear redrivers, including DS320PR410, DS320PR810, and DS320PR1601. Eye Scan is intended to be used as a supplemental vertical eye quality monitoring tool. Eye Scan's convenience, low run-time, and non-invasive nature are beneficial when performing PCIe redriver tuning.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

PCI-Express (PCIe) is a high-speed serial computer expansion bus standard common to desktop and server motherboards as an interface to graphics cards, network interface cards, hard disk drives, solid state drives, and various other hardware connections. When designing a motherboard or riser card for PCIe where the PCB's high-speed traces or connecting cable's insertion loss exceeds the *maximum* PCIe insertion loss requirement (36dB at PCIe Gen5.0, 32GT/s), a linear redriver can be used to compensate for added inter-symbol interference (ISI) induced by added insertion loss on these interconnect mediums. Texas Instruments PCIe Gen5.0 linear redrivers deploy continuous time linear equalizers (CTLE) on their receivers to provide a programmable high-frequency boost. This is followed by a linear output driver, creating a linear data path to preserve transmit preset signal characteristics while staying transparent to PCIe link training.

This application note describes the Texas Instruments PCIe Gen5.0 redrivers *Eye Scan* feature, which provides additional insight into vertical eye quality at the redriver's transmitter output pins. This document includes details on the Eye Scan feature capabilities and real-world examples of Eye Scan results.

2 Device Overview

The Texas Instruments PCIe Gen5.0 redrivers amplify high frequency content of incoming signals affected by ISI (Inter-Symbol-Interference). This amplification is done while adding minimal RMS jitter. PCIe Gen5.0 redrivers are designed for Gen4.0 and lower rates as well. Furthermore, these devices are protocol agnostic and can be used for CXL, SAS, and other applications.

Please see each device-specific data sheet referenced in Section 7 for details regarding internal block diagram, receiver equalization, linearity, and register programming.

3 Intention of Eye Scan

The Eye Scan feature of the Texas Instruments PCIe Gen5.0 redrivers was developed to allow users to determine an approximation of suitable equalization (EQ) boost settings for the PCIe redrivers, including CTLE and Flat Gain, in a quick and timely manner. Please note that this feature is designed to be used as an initial evaluation reference and cannot make sure of good system performance. The recommendation is to use other lane margining tools to monitor signal quality at each end of the PCIe link, or a compliance setup using equivalent BERT and or scope functionality to fine tune the redriver's EQ boost settings to guarantee BER performance.

3.1 An Introduction to Lane Margining

Before discussing the concept of Eye Scan, it is important to understand the concept of Lane Margining at the Receiver (commonly referred to as Lane Margining) in PCIe and how it is used as a metric for signal quality. Lane Margining allows for a user or system to determine how much margin or "cushion" is available on each PCIe lane at each lane's receiver. The receiver samples the incoming PCIe signal at its receiver at various points in the signal eye, typically beginning at the center of the eye (0 mV, 0 UI offset) and incrementally stepping up or down (voltage) and left or right (UI/time) until a set bit error rate (BER) threshold is reached at the sampling point. After stepping in each direction (up and down for voltage, left and right for UI/time), available lane margin can be determined based on the number of steps taken in each direction before the BER threshold was reached. For example, if the lane margining algorithm samples at steps of 5 mV and 0.02 UI, a lane margining result of {10 steps UP, 8 steps DOWN, 8 steps LEFT, 7 steps RIGHT} would give the following margin values:

- 50 mV margin UP
- 40 mV margin DOWN
- 0.16 UI margin LEFT
- 0.14 UI margin RIGHT

The lane margin values above sum to a total margin on this PCIe lane of (40 + 50) = 90 mV eye height and (0.16 + 0.14) = 0.3 UI eye width (where the conversion of UI to ps is data rate dependent).

In general, lane margining at the receiver allows system designers to monitor eye height and eye width at either a root complex or PCIe endpoint, which provides insight into the signal quality of the eye at a PCIe receiver. Eye Scan gives system designers a way to additionally monitor eye quality at the Texas Instruments PCIe redriver

transmitter, which can help provide insight into vertical eye quality and to find a range of well-performing redriver equalization (EQ) settings for a PCIe link.

3.2 How Does Eye Scan Work?

Inter-symbol interference (ISI) due to different data patterns and transmission lines can cause changes in vertical and horizontal eye openings. Thus, when monitoring PCIe link quality and stability with Eye Scan, normalizing techniques must be considered. Eye Scan works by counting the number signal *hits* at the PCIe redriver transmitter using a 64-level programmable DAC. The horizontal level of this DAC is swept for each of the DAC's 64 steps across a programmable range of voltage, limiting the incoming signal to the redriver's internal Eye Scan counter. This can be visualized using Figure 3-1.

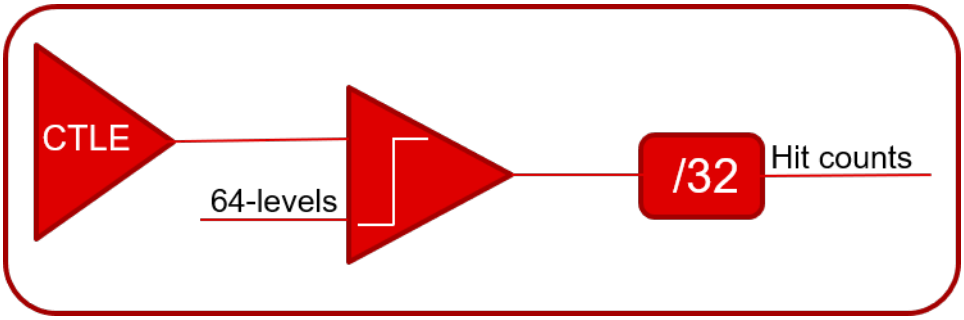

Figure 3-1. Eye Scan DAC and Hit Counts

At each DAC level, the number of signal *hits* is counted based upon the intersection of the signal with the DAC's voltage level, represented by horizontal lines in Figure 3-2. For each selected DAC level, the number of hit counts accumulate in a volatile redriver register and can then be stored in external memory as the DAC level is swept over the programmable DAC voltage range. The approach of Eye Scan is further detailed in Figure 3-2.

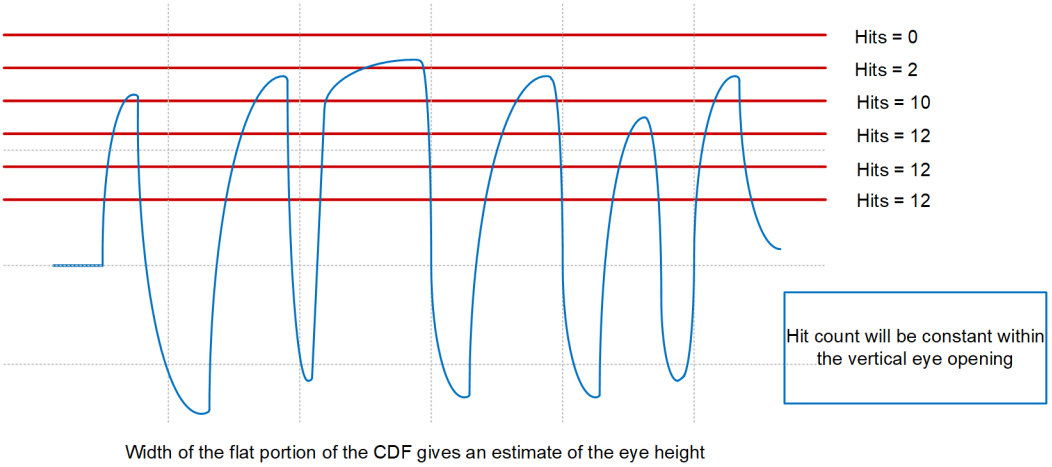

Figure 3-2. Eye Scan Hit Count Approach

To fully understand the concept of Eye Scan, the statistical concept of a Cumulative Distributive Function (CDF) must be introduced. A CDF of a real-valued random variable X is the function given by

$$F_X(x) = P(X \leq x) \tag{1}$$

Where the right side represents the probability that the random variable X takes on a value less than or equal to x. In this case, the random variable X is normally distributed with mean μ and standard deviation σ, that is

$$X \sim N(\mu, \sigma^2) \tag{2}$$

We can assume that the *hit* events of the high-speed waveform is normally distributed, thus a CDF of a normally distributed random variable *X* can be used when approximating the vertical eye opening at the redriver.

Using the above definition and CDF, the following conclusions can be made regarding hit count accumulation:

- A random bit pattern causes random vertical eye openings based on transmission media loss characteristics, thus multiple samples of the waveform are taken when accumulating hit counts.
- Zero hit counts accumulated at a DAC voltage level means that the voltage level is outside of the top or bottom of the vertical eye opening.
- Constant high hit counts accumulated at a DAC voltage level means that the voltage level is within the vertical eye opening.

An example of these conclusions is shown in Figure 3-3. The waveform is captured from an oscilloscope, where the top and bottom of the eye diagram are bounded by zero hit count values, while areas internal to the vertical eye opening are accumulated as near-constant hit count values.

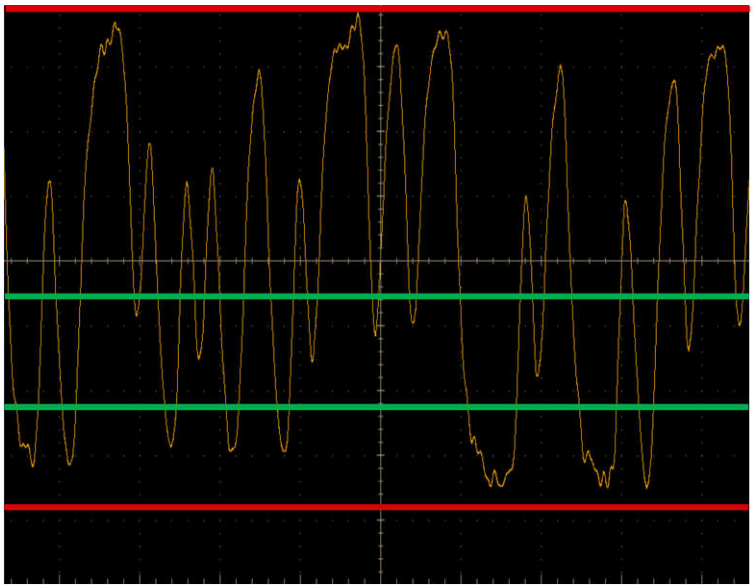

Figure 3-3. Zero Hit Counts (Red) vs. Constant Hit Counts (Green)

3.3 Programming Steps for Manual Eye Scan Capture

To programmatically capture the Eye Scan of varying equalization settings of the PCIe redriver, the following measures must be taken to verify that the capture is valid.

- Verify that the PCIe redriver is operating in either SMBus (I^2C) Primary or Secondary Mode before powering on the device (MODE pin L1 or L2).
- Connect an I^2C controller to the SDA/SCL pins of the PCIe redriver capable of meeting the redriver's SMBus/I^2C timing requirements (found in each device specific data sheet).

After powering on the PCIe redriver, the following steps can be taken to complete an Eye Scan sweep on a single channel. Please refer to device specific programming guides avaialble on ti.com for further device programming information.

1. Verify that the redriver's channel equalization settings (CTLE, Flat Gain) are configured as desired using direct SMBus/I^2C programming or using the Texas Instruments SigCon Architect GUI, available on ti.com.
   a. If modifying PCIe redriver settings after PCIe link-up has begun or completed, make sure to perform a PCIe *warm reset* (exercising PERST#) or a PCIe *link retrain* to verify that the PCIe link has properly re-trained with the re-programmed redriver equalization settings.
2. Verify that the PCIe link with the redriver has entered an active link-up state (L0) at the desired data rate.
   a. An active-traffic PCIe link maintains that a valid Eye Scan is captured.
3. Verify that the proper redriver channel to perform the Eye Scan capture on is selected.

4. Set the desired DAC granularity on the redriver channel to sweep the desired voltage range.
5. Begin sweeping the redriver channel's DAC level, dividing each captured hit count 32 to normalize for insignificant variations hit count values.
   a. Make sure to capture each DAC level's hit count value captured by the redriver before changing the DAC level to gather valid hit count datapoints.

To visualize the captured Eye Scan for the redriver channel, plot each of the 64 DAC hit count values vs. DAC voltage level (or DAC step). This plot is a 90° counter-clockwise rotation of the *vertical eye* captured at the redriver's transmitter. An example Eye Scan capture plot can be seen in Figure 3-4, where one EQ boost setting is selected for an Eye Scan capture, then each hit count data point is plotted.

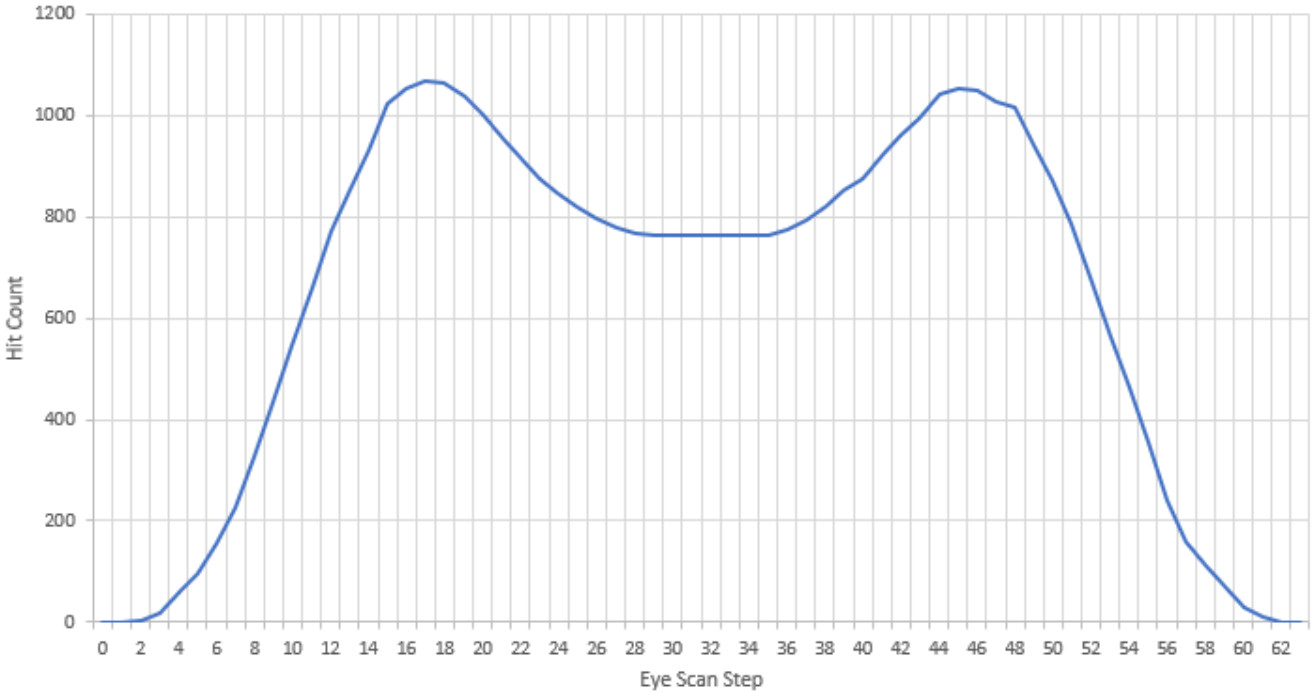

Figure 3-4. Example Eye Scan Hit Count vs. DAC Step

In Figure 3-4, a *flat* region is observed between the *peaks* of the hit count plot. This region represents an *open* portion of the vertical eye observed at the redriver's transmitter. This can be correlated with an oscilloscope's eye diagram capture of the same waveform directly after the redriver using the histogram feature of the oscilloscope to plot hits counted at each point along the vertical axis, shown in Figure 3-5. This comparison shows the strong correlation between the oscilloscope's capture and Eye Scan's capture of the vertical eye at the redriver transmitter. Please note that the oscilloscope histogram is not to scale.

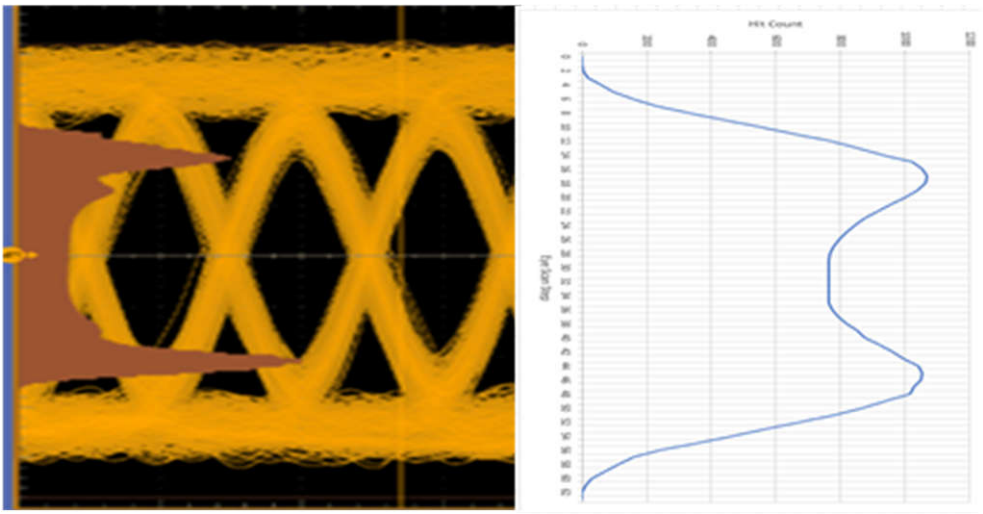

Figure 3-5. Histogram Plot of Captured Eye After Redriver vs. Eye Scan Capture Plot

3.4 Eye Scan Capture Registers

For information regarding register associated with Texas Instruments PCIe Gen5.0 redrivers' Eye Scan, please contact your local TI respresentative.

3.5 CTLE Sweep Result

In real-world PCIe channel mediums, varying insertion loss must be compensated for. To compensate for varying pre-channel (before the redriver) insertion loss, a higher EQ boost must be applied by the redriver to compensate for added insertion loss. A visualization of some of the redriver's EQ boost settings, specifically EQ Boost 1, using the Eye Scan feature and a plot is shown in Figure 3-6.

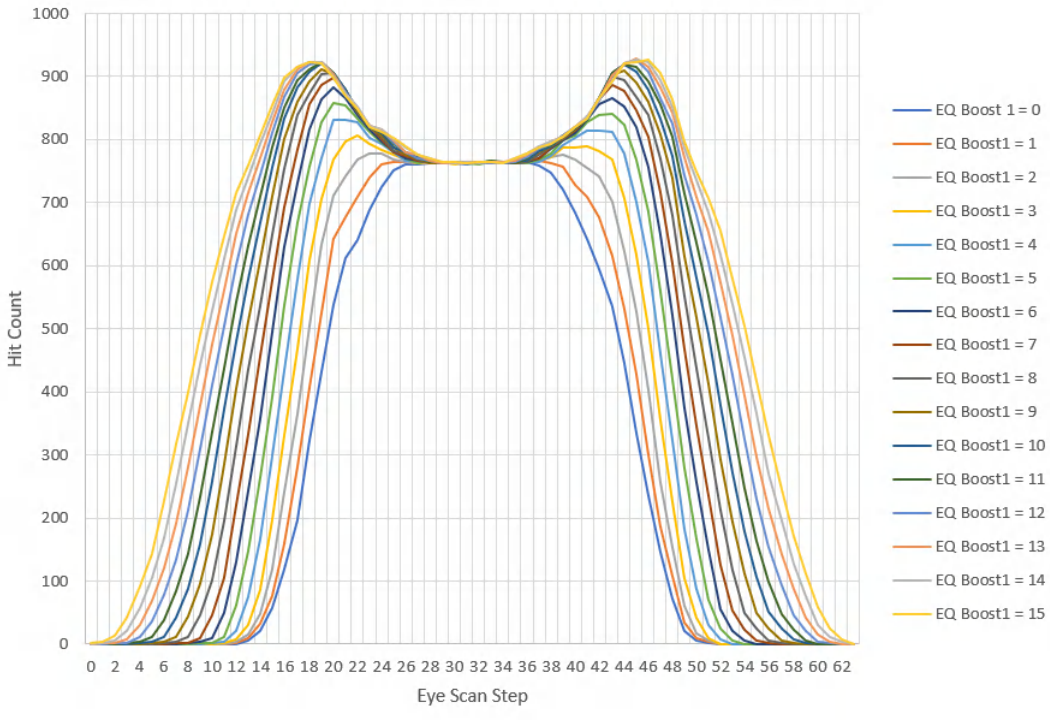

Figure 3-6. Eye Scan Results of Varying EQ Boost 1 Settings

As EQ Boost 1 is increased, the shape of the Eye Scan plot changes in multiple ways. In Figure 3-6, we can observe that at a low EQ Boost 1 value (example, EQ Boost 1 = 0), the hit count *flat* region of the Eye Scan

plot is relatively small and not accompanied by hit count *peaks*. However, as EQ Boost 1 increases, the Eye Scan plot begins to show two distinct hit count *peaks* with a distinct *flat* region between. The region between these hit count *peaks* is indicative of some *vertical eye opening*. While choosing the best EQ Boost settings can be challenging, in many applications the *best* EQ Boost settings show slight *under-equalization* at the redriver's transmitter. That is, when the hit count *peaks* are less defined, but above the minimum peak, a well-performing range of EQ Boost settings is selected.

3.6 Eye Scan DAC Range

The Eye Scan feature of Texas Instruments PCIe redrivers additionally allows for four different DAC granularities or DAC ranges to be programmatically selected. These ranges include ±100mV, ±200mV, ±300mV, and ±400mV, allowing users to select the voltage precision at which the DAC is to sample hit counts. This feature allows for users to observe the vertical eye at the redriver's transmitter with added granularly, which can help to pinpoint variation or irregularities in PCIe channel performance. Note that for any selected DAC range, 64 DAC steps are still swept. This allows the DAC range setting to act as a *zoom* feature into vertical eye quality at the redriver's transmitter; a reduced DAC range setting can more accurately provide insight into vertical eye quality.

The ranges available using Eye Scan can be visualized in Figure 3-7 where a single EQ boost setting was selected and subsequent Eye Scan plots were captured. These visualizations were created using the Texas Instruments SigCon Architect GUI and the associated PCIe Gen5.0 redriver device profiles, including DS320PR1601 and DS320PR410. The details of Eye Scan in the SigCon Architect GUI are discussed in Section 5.

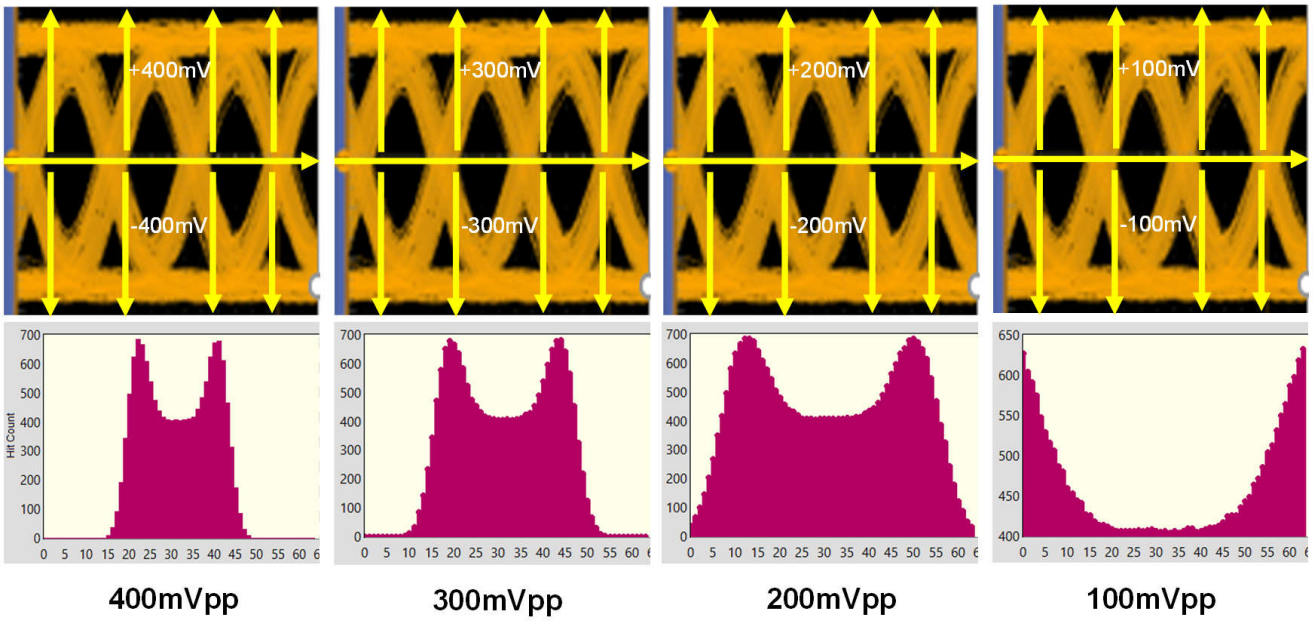

Figure 3-7. Eye Scan DAC Range Variation vs. Hit Count

4 Eye Scan Applications

Eye Scan can be leveraged to visualize vertical eye quality at the redriver's transmitter in two key application spaces: during PCIe Compliance and in a PCIe system configuration. While there is some overlap in each case, each application has specifics that are covered speicifically.

4.1 Eye Scan Application: PCIe Compliance

This section focuses on the specifics of Eye Scan during PCIe compliance. A typical PCIe TX compliance setup is visualized in Figure 4-1 using a Texas Instruments PCIe Gen5.0 redriver evaluation module (EVM) and a PCIe Gen5.0 capable Add-in-Card (AIC) endpoint to conduct testing and Eye Scan captures.

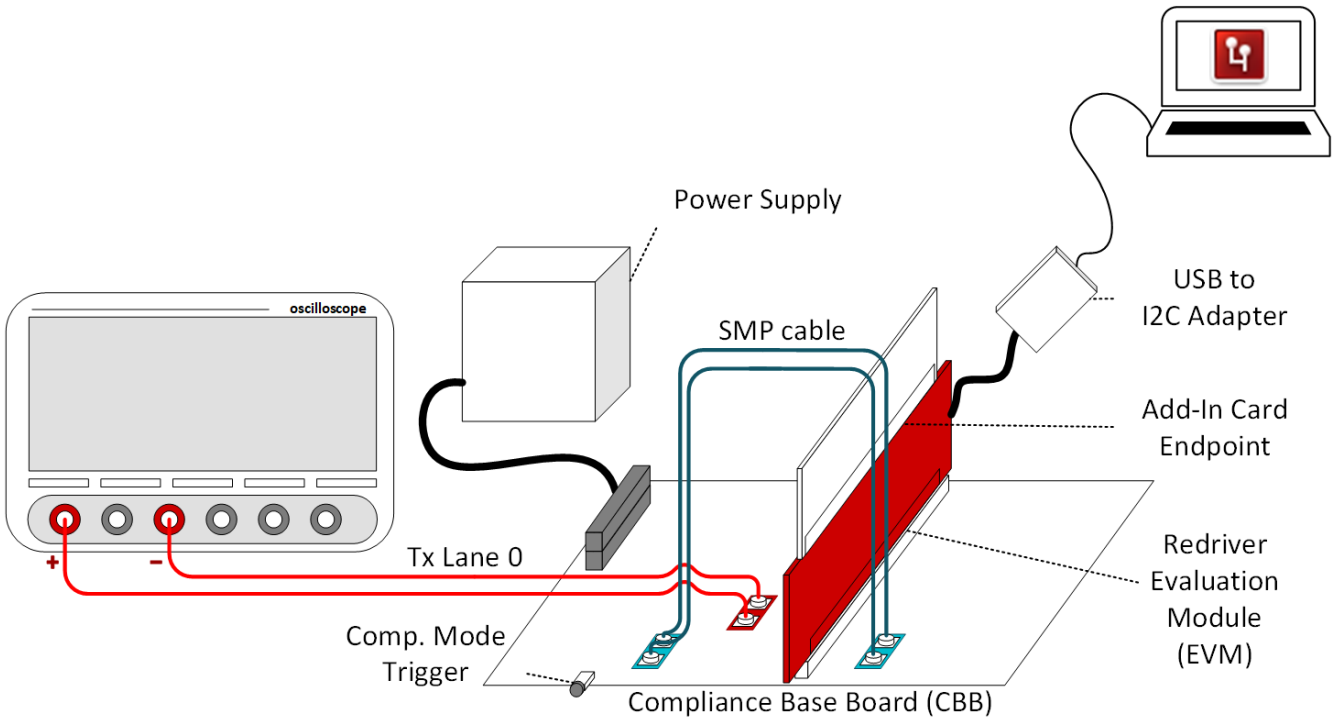

Figure 4-1. PCIe TX Compliance Setup

During PCIe compliance testing, Eye Scan can be used to observe vertical eye quality at the redriver's transmitter. Through I^2C programming, the redriver's EQ boost settings can subsequently be changed to adjust the boost applied at the redriver transmitter, which can assist in the redriver *tuning* process. For the redriver EQ boost setting selected, the Eye Scan algorithm is run and the resulting plot captured to understand if the PCIe channel is well-equalized,over-equalized, or under-equalized. Please note that in a typical PCIe compliance setup, minimal post-channel insertion loss is present. Thus, the Eye Scan capture more accurately represents the vertical eye seen at the receiver of the oscilloscope or post-processing software.

Understanding the effects of PCIe TX Presets on vertical eye quality is critical due to potential impact on channel performance and signal integrity. Eye Scan can easily capture the effects of PCIe TX Presets during compliance testing. As shown in Figure 4-2, the effects of preshoot and de-emphasis for Presets P5, P6, and P9 can be realized using Eye Scan captures and plots in comparison to oscilloscope captures. In each of the Preset captures, the EQ boost settings of the redriver are held constant. For reference, the PCIe TX Preset table for P4, P6, P7, and P9 is included in Table 4-1.

Table 4-1. PCIe TX Preset Table

TX Preset	Preshoot (dB)	De-emphasis (dB)
P4	0	0
P6	2.5 ± 1	0
P7	3.5 ± 1	-6 ± 1.5
P9	3.5 ± 1	0

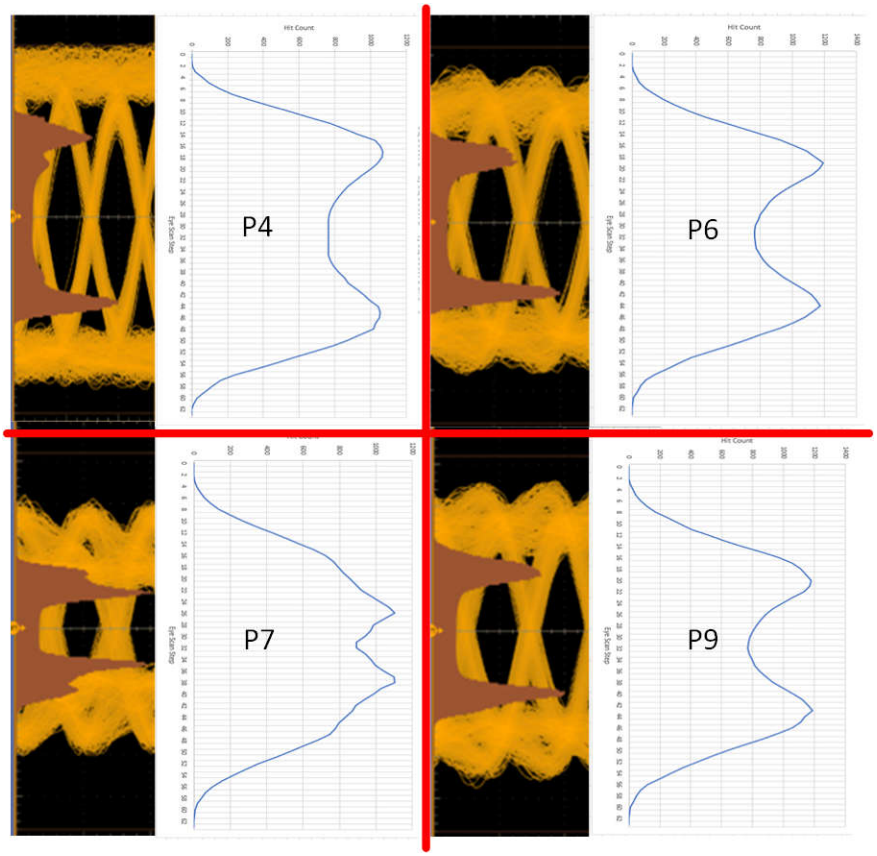

Figure 4-2. PCIe TX Preset Comparison From Oscilloscope and Eye Scan. From Top Left to Bottom Right: TX Preset P4, P6, P7, P9

As shown in Figure 4-2, Preset P4 applies no preshoot or de-emphasis, resulting in a relatively *clean* Eye Scan vertical eye capture and a wide flat region between hit count *peaks*. However, when preshoot is applied to the PCIe signal traveling through the redriver, these added emphases impact the high-frequency components of the signal, resulting in slightly altered Eye Scan vertical eye captures. The effects of preshoot are seen in Presets P6 and P9; preshoot, which applies boost just before the preceding edge of any waveform transitions, decreases the width between the hit count *peaks* of the Eye Scan plots. Conversely, the effects of de-emphasis is seen in Preset P7; de-emphasis, which applies boost just after waveform transitions, creates a *ripple* effect during the transitions between the hit count *peaks* of the Eye Scan plots.

4.2 Eye Scan Application: System

Eye Scan can also be leveraged to gain insight into the vertical eye quality at the redriver's transmitter in a PCIe system configuration. However, one must note that a PCIe redriver is best designed to handle *pre-channel* insertion loss, but in many system configurations, post-channel insertion loss is also present. Thus, Eye Scan vertical eye quality measurements can differ from vertical eye opening results shown with lane margining at the receiver (either at the root complex or at the endpoint).

A typical PCIe system configuration utilizing a redriver encompasses either of the following two setups. Figure 4-3 details a system configuration using a Texas Instruments PCIe redriver on a TI EVM, while Figure 4-4 details a system configuration using a Texas Instruments PCIe redriver on a system motherboard.

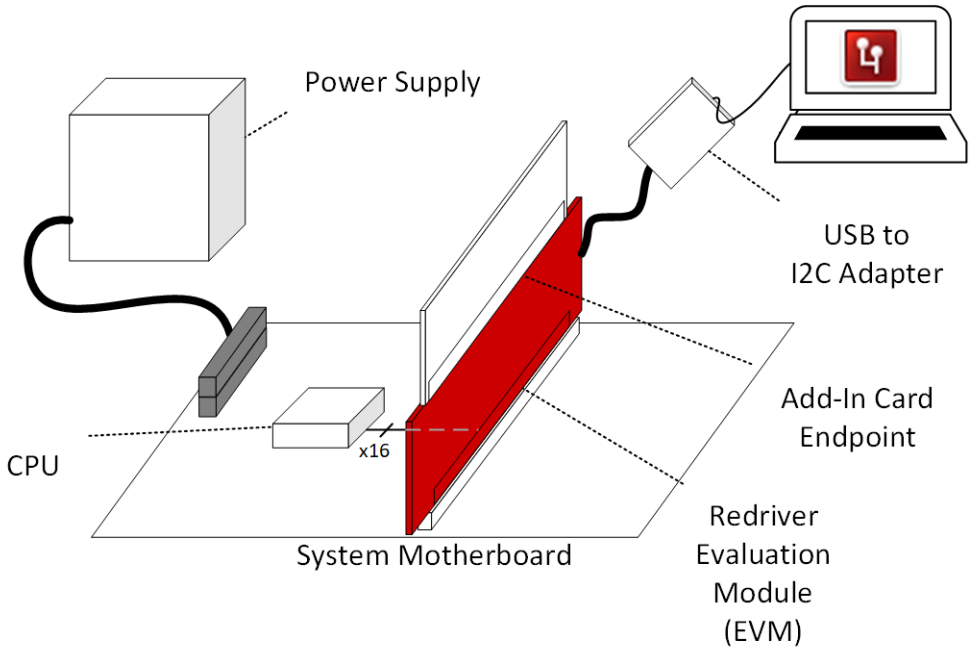

Figure 4-3. PCIe System Configuration Using a TI PCIe Redriver EVM

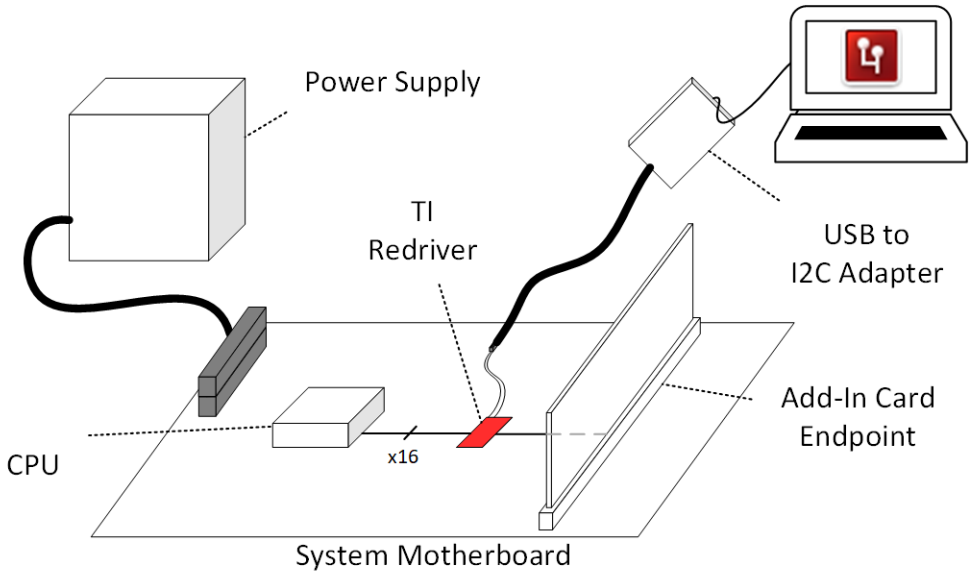

Figure 4-4. PCIe System Configuration Using a TI PCIe Redriver on a Motherboard

In each system configuration, Eye Scan can be utilized to provide insight on vertical eye quality at the redriver's transmitter, which can help find a range of EQ boost settings that improve PCIe eye performance (in addition to PCIe lane margining tools). To better visualize an example of Eye Scan in a system configuration, an Eye Scan plot for one Downstream and one Upstream PCIe channel in the SigCon Architect GUI can be seen in Figure 4-5 during an active PCIe Gen4 link-up.

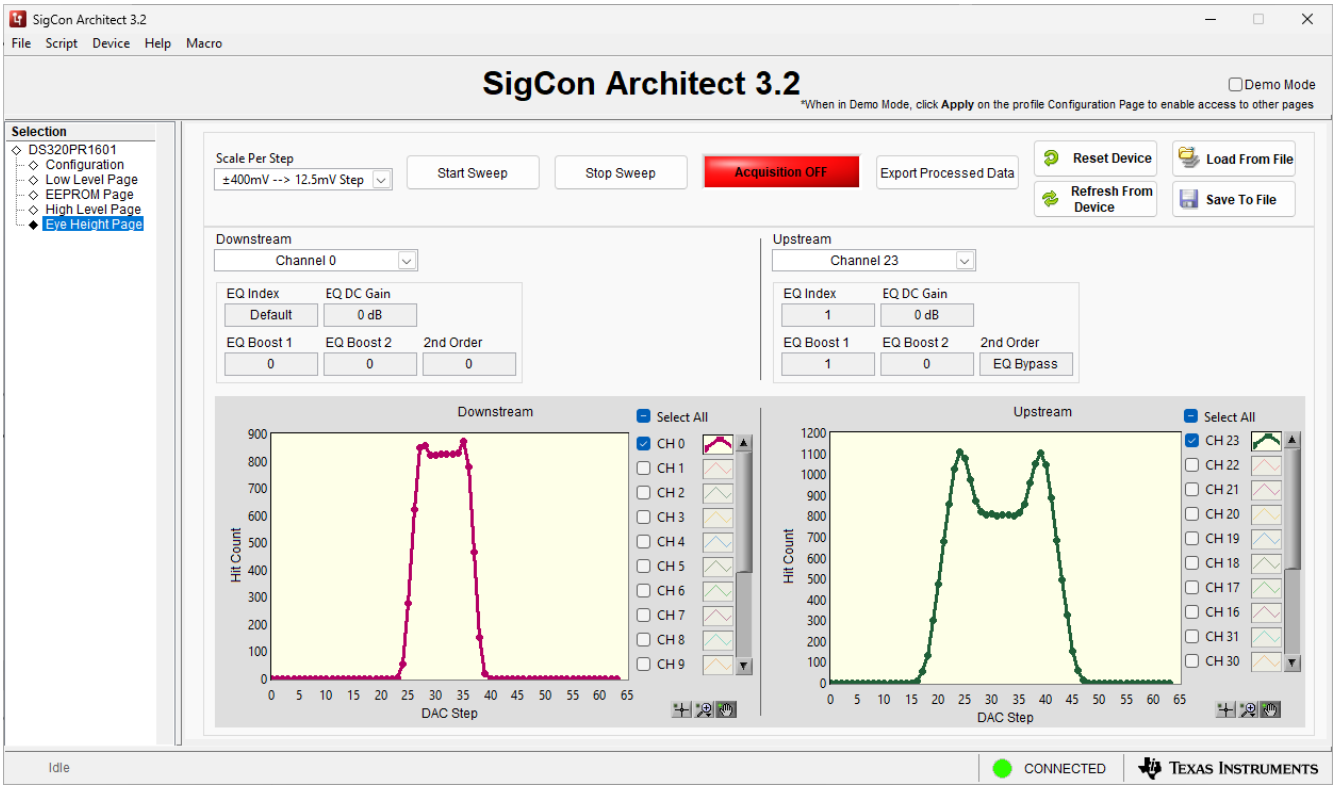

Figure 4-5. Example System Eye Scan Plot in the SigCon Architect GUI

5 Eye Scan in SigCon Architect GUI

The Eye Scan feature in the Texas Instruments SigCon Architect GUI Eye Height Page functions by capturing the manual Eye Scan sweep of the PCIe signal at the redriver's transmitter output pin, plotting each measured hit count value with the corresponding DAC level. The GUI can capture the Eye Scan for each selected device channel, allowing for users to pinpoint a single redriver channel or multiple/all redriver channels for Eye Scan capture. An example of the SigCon Architect GUI Eye Height Page before Eye Scan capture can be seen in Figure 5-1 while using the DS320PR1601 device profile. Annotations are provided for reference.

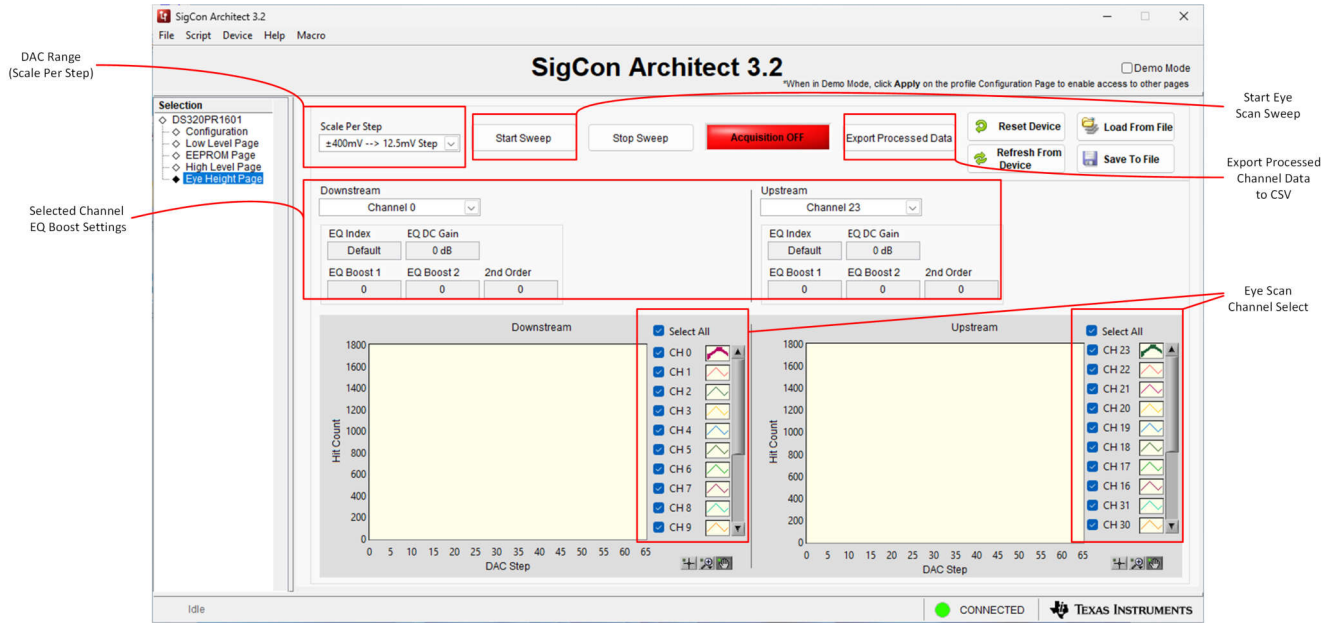

Figure 5-1. SigCon Architect DS320PR1601 Eye Height Page with annotations

In the Eye Height Page of the DS320PR1601 SigCon Architect GUI profile, users can select particular PCIe redriver channels to perform Eye Scan sweeps on and plot the subsequent results, allowing for increased flexibility when monitoring vertical eye quality at the redriver transmitter. These channels are divided between redriver *Downstream* channels and *Upstream* channels for convenience. As mentioned in Section 3.6, users can also select the DAC range or *Scale Per Step* for Eye Scan to sweep in the upper-left corner of the GUI. The channel EQ Boost settings for the selected Downstream and Upstream channels are also displayed for reference.

Once the desired PCIe redriver channels are selected for Eye Scan monitoring using the 'Eye Scan Channel Select' menus, users click the *Start Sweep* button to begin the Eye Scan sweep.

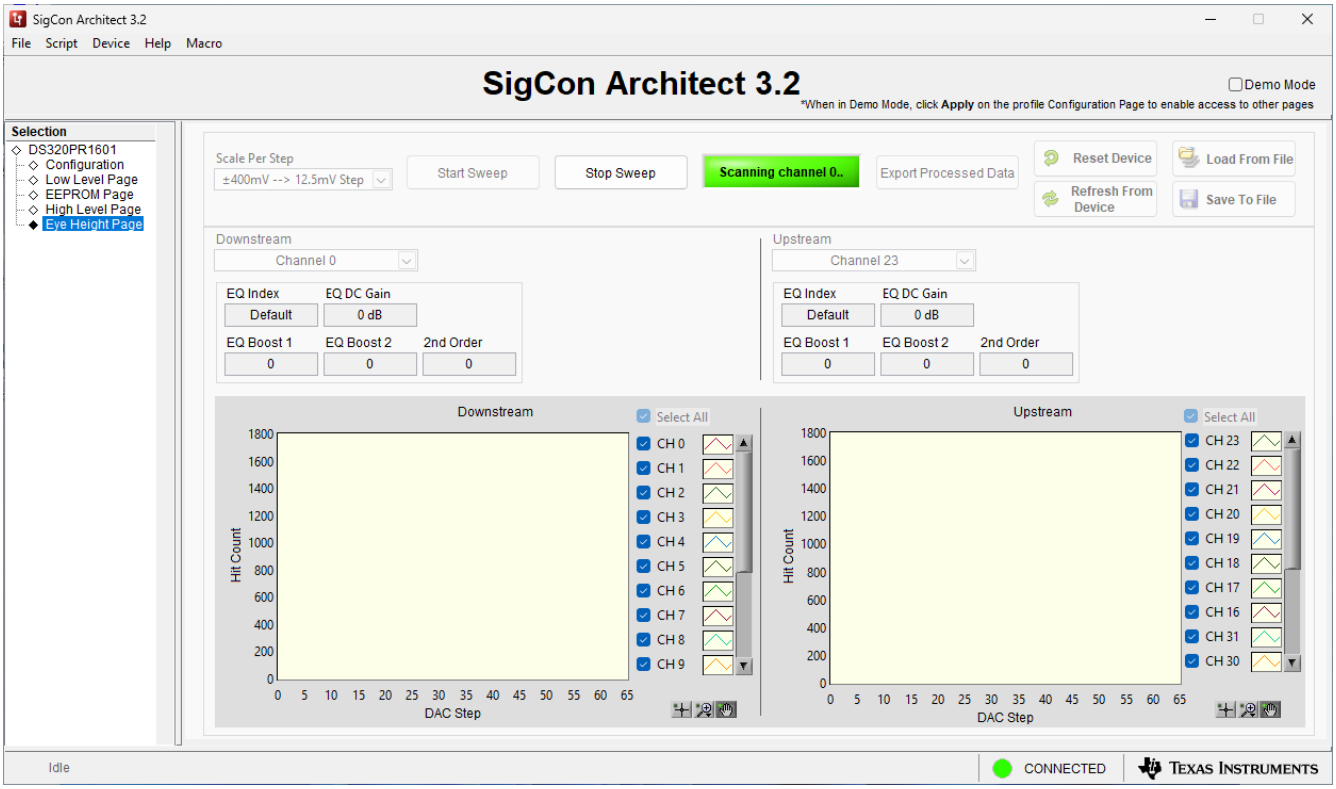

Figure 5-2. Eye Scan Sweep Initiated, Indicated by Green Scanning Channel X Display

After the Eye Scan capture has completed, users are presented with the plots of the selected Eye Scan channels. Each of these plots can be selected or de-selected for visualization in the graphical interface through the *Eye Scan Channel Select* menus. Users are able to export the captured Eye Scan result data points of channels selected in the *Selected Channel EQ Boost Settings* drop-down menu by clicking the *Export Processed Data* button. The SigCon Architect GUI Eye Height Page also allows for users to optionally customize the output style of the Eye Scan plots for preferred visualization by selecting the individual plot icons next to each channel in the *Eye Scan Channel Select* menu.

Figure 5-3. Example Eye Scan Plot Capture Using SigCon Architect

From Figure 5-3, we can observe that channels on the Upstream side of the PCIe redriver have a large margin of vertical eye quality (indicated by the relatively flat region of each channel), while channels on the Downstream side of the PCIe redriver have a small margin of vertical eye quality (indicated by short, spiked center region of each channel). This can be indicative of the need for additional EQ Boost setting tuning of the redriver Downstream channels to optimize vertical eye quality at the redriver transmitter. However, users must make note that the amount of *post-channel* loss present in the PCIe channel after the redriver when considering EQ Boost setting tuning. If a highly lossy post-channel is present at the transmitter of the PCIe redriver, vertical eye quality at the redriver transmitter is most likely not indicative of vertical eye quality at the PCIe receiver. Thus, care must be taken to verify that vertical eye quality (and overall eye quality) is within PCIe specification at the PCIe receiver.

The Texas Instruments SigCon Architect GUI and associated PCIe redriver device profiles are available for download via request on ti.com or can be requested by contacting your local TI representative. For further information regarding SIgCon Architect GUI profiles, please refer to the device-specific EVM User's Guide.

6 Summary

The Texas Instruments PCIe redriver Eye Scan feature allows for users to gain insight into vertical eye quality at the redriver's transmitter in multiple application spaces. Eye Scan can be used in assistance with PCIe lane margining tools to select a range of PCIe redriver equalization (EQ) boost settings for their PCIe application, potentially reducing redriver tuning time and effort during PCIe compliance or in PCIe system bring-up and link quality testing. Eye Scan's convenience, low runtime, and non-invasive nature are beneficial when performing PCIe redriver tuning.

7 References

- Texas Instruments, *DS320PR410 Four-Channel Linear Redriver for PCIe 5.0, CXL 2.0*, data sheet
- Texas Instruments, *DS320PR810 Eight-Channel Linear Redriver for PCIe 5.0, CXL 1.1*, data sheet.
- Texas Instruments, *DS320PR1601 32Gbps 16 Lane PCIe® 5.0, CXL 2.0 Linear Redriver*, data sheet.
- Texas Instruments, *How to Tune TI PCIe Gen5 Redrivers*, application note.
- PCI-SIG, *Pushing to the Limits: Understanding Lane Margining for PCIe®*, application note.

8 Revision History

Changes from Revision * (September 2023) to Revision A (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added hyperlink to *DS320PR410*	1
• Added hyperlink to *DS320PR410 Four-Channel Linear Redriver for PCIe 5.0, CXL 2.0*	16

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265