DS1776

Application Note 725 PI Bus

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PI Bus

National Semiconductor
Application Note 725
Joe Wert
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HISTORY

Throughout the 70's and early 80's the typical backplane was driven by standard TTL logic parts with tristateable outputs such as 54/74XX240 and 245. For design purposes these busses were modeled as lumped capacitances and transmission line effects were ignored because the bus data rates were generally not fast enough to require designers to be concerned with transmission line effects of the backplane. With the lower bus speeds there was sufficient bus settling time for reflections to dampen, and the signals to stabilize close enough to steady state to avoid problems. If a bus was heavily loaded and attempts were made to run the bus faster than 10 MHz, errors in data were frequently seen due to line reflections causing line voltage levels to transition through threshold more than once for a single transition of the buffer input. And as backplane densities increased, loading from the transceivers became so great that this increased the problem of driving the bus quickly and error free.

With today's higher bus data rates it has become imperative that the transmission line characteristics of the backplane be accounted for in backplane analysis. By doing so it becomes apparent that there may be better ways to drive backplanes than with traditional TTL family logic.

To solve some of the inherent problems with running densely loaded busses, the PI Bus structure was developed. PI Bus (parallel interface bus) was developed by IBM, Unisys and TRW for the VHSIC 2.2 Interoperability program. PI Bus has since been adopted by the Joint Integrated Avionics Working Group (JIAWG) section of SAE.

TRANSMISSION LINE PHYSICS

Several problems must be overcome to run a faster, more heavily loaded bus. When the bus propagation delay plus settling time decreases below about 100 ns the backplane must be considered as a transmission line. If the backplane is densely populated the problem of running it at high data rates is exacerbated.

Z_0 is the characteristic impedance of the backplane, and is calculated from the physical characteristics of the backplane. From *Figure 1*, a simple model of a transmission line, the following equation may be written:

$$Z_0 = [\ (R + jwl) / (G + jwc)\ ]^{1/2}$$

For high frequency, the R and G terms become insignificant due to the increases in the w terms,

$$w = 2\ \pi f \text{ where f is frequency}$$

and the equation simplifies to

$$Z_0 = (L/C)^{1/2}$$

where L is in units of inductance per unit length and C is in units of capacitance per unit length

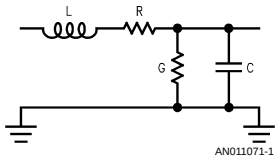

FIGURE 1.

EFFECTS OF CAPACITIVE LOADING ON BUS

Values for Z_0 can be calculated from the physics of the backplane construction. For a typical PI Bus epoxy-glass backplane the value for Z_0 is about 65Ω. The basic equation describing the impedance of a loaded bus is

$$Z_1 = Z_0 / (1 + C_1/C)^{1/2}$$

where C_1 is the additional load added to the bus by modules, connectors and connector mounting vias. So as the capacitive load of the modules increases, the impedance of the bus decreases. As the impedance of the bus decreases, the current required to drive the bus between state changes in a given time period increases (I = V/Z). The equation for the propagation delay of a signal on an unloaded transmission line is

$$T_{P0} = \ell (L/C)^{1/2}$$

where ℓ = length of the bus.

For a loaded bus,

$$T_{P1} = T_{P0}(1 + C_1/C)^{1/2}$$

describes the propagation delay on a transmission line. From the equation for the loaded bus, it is obvious that as the capacitive loading of the bus increases, the propagation delay for a given length of bus increases. As this time increases bus settling time increases, and hence affects how fast the bus may be operated. So a bus transceiver which had low capacitive loading would improve bus operation in several ways. A low capacitive transceiver would raise the value of Z_1, and hence the drive current requirements for a given performance would be reduced, the propagation delay for a given length of backplane would be reduced, and any bus settling time required would also be reduced.

OUTPUT V_{OH} SWING

The standard TTL swing for an output is from 0.2V to V_{CC} − two diodes (for CMOS 0V to V_{SS}). For a bipolar device, this swing could be as much as from 0.2V to 4.1V. The smaller

this swing between high and low, the less charge which must be moved in any given time to effect a change of state. So from the standpoint of power usage, smaller in this case would be better.

PI Bus developed as a bus to address both these conclusions in a manner similar to Future Bus. The bus side outputs are open Schottkys, and the bus is terminated on both ends by a resistor to a voltage source with limits of 1.9V to 2.1V (*Figure 2*). The resistors used to terminate the bus may be from 30Ω to 40Ω. By terminating the bus in this way, (Z_0 matches 40Ω termination with no loads on the bus, but including loading from raw backplane plus vias and mating connectors, and a 30Ω termination matches a fully loaded PI bus backplane) the bus is somewhat tuned to the Z_1 of the bus so that reflections can be minimized. By terminating the bus to a maximum of 2.1V, the maximum voltage swing on the bus will be from the V_{OL} minimum spec of 0.4V to the maximum 2.1V. Thus the voltage swing for the PI Bus transceiver would be 1.7V versus the 3.9V for a standard bipolar transceiver.

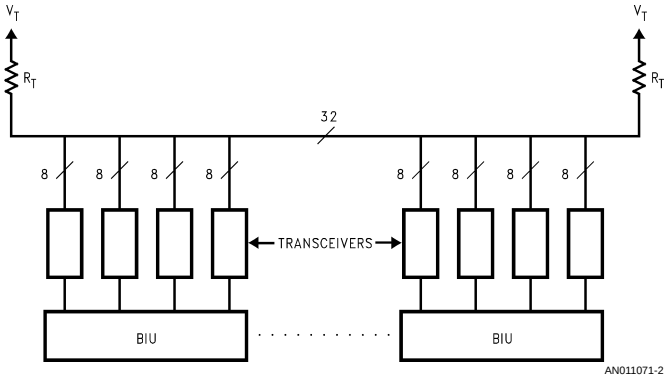

FIGURE 2.

OUTPUT CAPACITANCE OF TRANSCEIVER

In order to decrease the capacitive loading of each transceiver, Schottky diode outputs are used, and are reverse biased when not active low. The PI Bus driver output is shown in *Figure 3*. When the output is in a high state both the output Schottky diode and the collector-substrate diode of Q1 are reverse biased. By reverse biasing both the Schottky diode junction and the collector-substrate junction the parasitic capacitive loading of the bus driving output can be greatly decreased. The following equation gives an approximation of the impact reverse biasing has upon junction capacitance:

$$C_j = C_{j0}/(1 + V_d/V_0)^{1/2}$$

where C_{J0} equals the capacitance of the diode junction under unbiased conditions, and V_d equals the reverse biased voltage of the diode junction. V_0 is the built-in zero bias potential across a diode junction, and would be on the order of 0.7V. So, by reverse biasing the cathode of both D1 and Q1, their parasitic capacitive loading on the bus is decreased. If the bus were at 2.0V, and V_{CC} was at 5V, C_{J0} would be decreased by a factor of 2.1. Then of course, C1 and C2 are in series, so their total capacitance would be decreased according to the following equation:

$$C_T = C_P + [(C_1)\ (C_2 + C_3)] \div (C_1 + C_2 + C_3)$$

The capacitance of C3 (from D3) is basically negligible in comparison to C1 because it is approximately 0.5% the area Q1. The package capacitance (C_P) may vary from 0.3 pF to 1.5 pF, depending upon the package and the pin location on the package. The other capacitive loading on each bus pin would be the base-collector and base-emitter capacitance of Q7 (*Figure 8*), which connects to the anode of D1. For a typical TTL part (*Figure 5* and *Figure 6*), the capacitive loading of the output would be primarily C5 because C6 is in series with C7 and the parallel combination of C8 and C9. For Q4 and Q5 being about the same size devices, the capacitive loading of the TTL circuit would be several times larger than that of the Schottky terminated circuit.

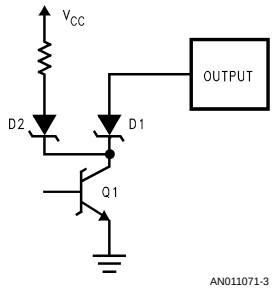

FIGURE 3. Simplified Circuit

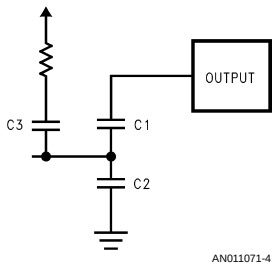

FIGURE 4. Parasitic Capacitance

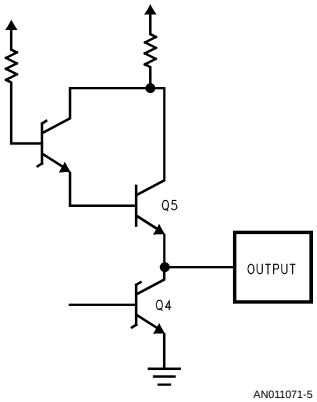

FIGURE 5.

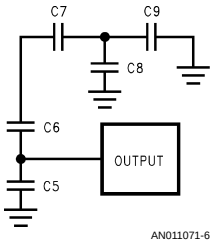

FIGURE 6.

PRECISION THRESHOLD

In order to handle the smaller output swing on the bus, it is necessary to use a more precise threshold circuit on the bus receiver input. *Figure 7* is a typical TTL input buffer. The threshold set by this type of circuit varies considerably with temperature, and typically ranges from about 1V at high temperatures to about 1.8V at low temperatures. Such movement could not be tolerated with a bus swing which could be as small as from 1.15V to 1.9V. The circuit shown in *Figure 8* is used on PI Bus transceivers to set a more precise threshold. A voltage reference with a very small V_{CC} and temperature dependence is placed on the chip to establish a precision threshold for the PI Bus to BIU input buffer. By using a differential pair with one of the pair controlled by the reference voltage, the threshold can be maintained within a 150 mV window centered at 1.52V.

OUTPUT RAMPS AND NOISE IMMUNITY

Ramped outputs have been touted as the solution to problems of bus reflections and crosstalk. The amount of ramp time put into rise and fall times directly related to the propagation delays of a transceiver, so longer ramps require longer delay times. An important question to ask is how much of a ramp buys what degree of decreased bus settling time. Many TTL parts have peak ramps of about 2V/ns. This rate of ramp certainly seems to increase bus settling times. The PI Bus transceiver will have a typical ramp rate of about 0.5V/ns.

Having some amount of noise rejection on the bus receiver input allows the bus buffer input to ignore small excursions above or below threshold without affecting the data being transmitted to the BIU. However the greater the amount of noise immunity, the greater the propagation delay on the path from the bus to the BIU. The PI Bus transceiver offers a compromise between noise immunity and prop delays with typically 4 ns of pulsewidth protection measured at 1.5V for a 1 to 2 volt input.

SUBMICRON BIU PROTECTION

To accommodate future submicron BIU processing, the PI Bus transceivers offer a feature for limiting the output V_{OH} excursion to the BIU. The V_X pin on the chip can be used as a clamp voltage to limit the V_{OH} of the BIU side output. The basic propagation delays on the transceiver with the exception of the BIU side low to high ramp rate are unaffected because the remainder of the transceiver is still powered by the normal V_{CC} pin. Only the BIU V_{OH} is controlled by the V_X pin. The *Figure 9* schematic shows how the V_X voltage sets the output V_{OH}.

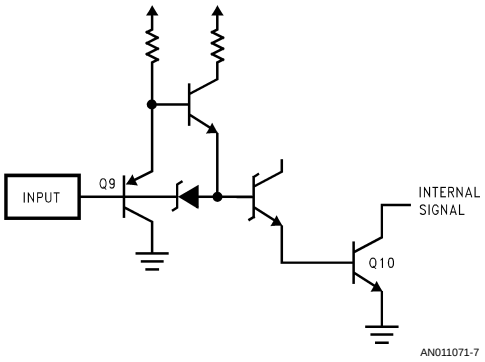

FIGURE 7. Typical TTL Input

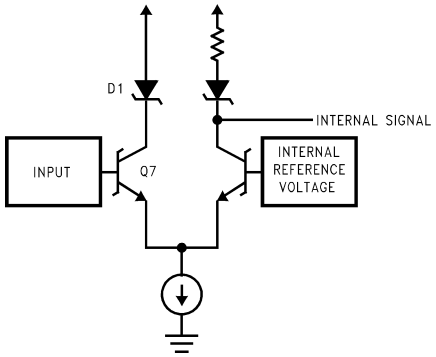

FIGURE 8. PI Bus Receiver Input

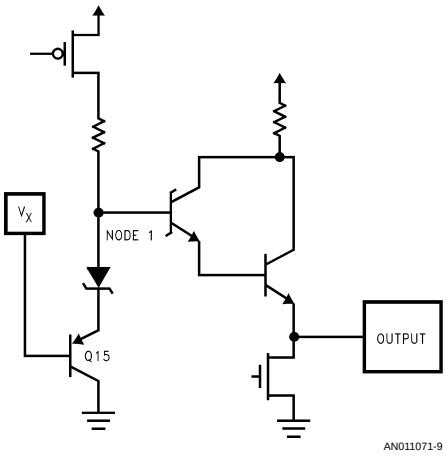

FIGURE 9.

LOW POWER

Many applications of PI Bus are designed with a redundant bus, and as such always have a full set of transceivers in the inactive mode. And in addition, on the active bus there may be 15 inactive (for a 16 drop bus) transceivers with one active transceiver. So in order to lower the power requirements for the PI Bus backplane application the National PI Bus transceiver, the DS1776, was designed using BiCMOS in order to take advantage of the power savings possible with the use of CMOS in appropriate portions of the circuit.

A pure bipolar transceiver would have an I_{CC} inactive specification of about 100 mA. By using a BiCMOS process it was possible to design a PI Bus transceiver with an I_{CC} inactive of 35 mA.

BIPOLAR vs CMOS vs BiCMOS TECHNOLOGY

A full bipolar transceiver could be built to provide excellent performance in most areas with the exception of power consumption in both the active and inactive modes. A pure CMOS part could be designed with a much lower I_{CC}, but it would have the following drawbacks. It would be slower than a bipolar part, no Schottky diode would be available to construct a low capacitance output with limited swing, and stable CMOS voltage references which have a reasonable silicon area are non-existent, so setting a precise input voltage threshold would be difficult.

By making judicious use of bipolar and CMOS circuits where each is appropriate, it was possible to design a PI Bus transceiver with an I_{CC} inactive of typically 35 mA and yet maintain the full features which make PI Bus a clean and quiet bus to run.

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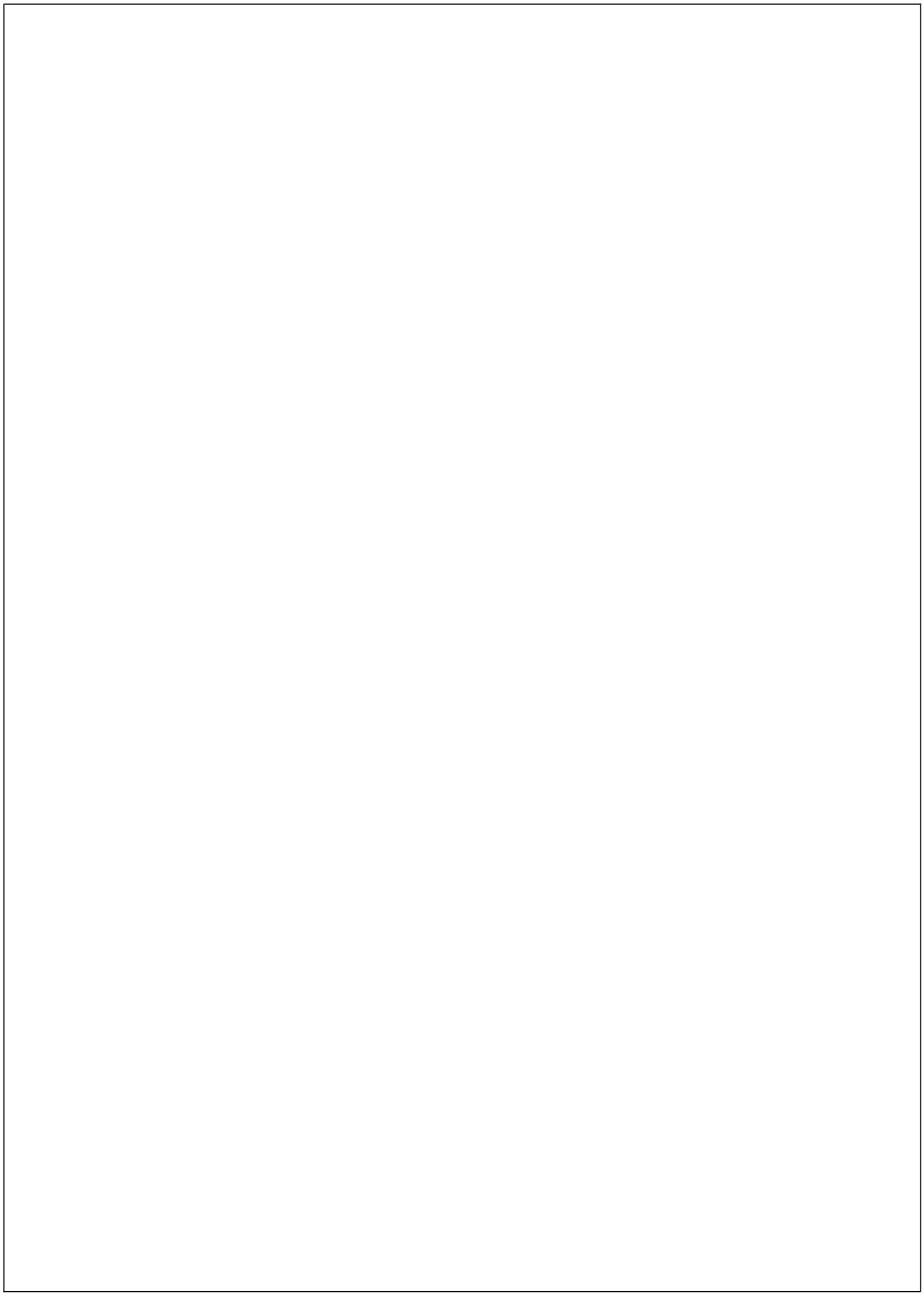

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