# *AN-927 Total Dose Testing of Advanced CMOS Logic at Low Voltage*


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# Total Dose Testing of Advanced CMOS Logic at Low Voltage

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**ABSTRACT**

This paper examines the impact of using an Advanced CMOS product in a low voltage (3.3 $V_{DC}$) application which is subjected to a total ionizing dose environment.

Results from this investigation(1) demonstrate a significant improvement in the total dose response of radiation-induced leakage current at 100 krads(Si) level. The improvement factor of low voltage (3.3 $V_{DC}$) was greater than 8x better than 5.0 $V_{DC}$.

**INTRODUCTION**

System designers are increasingly interested in low-voltage logic, particularly in the commercial areas of battery-operated notebooks and laptop computers. As a result, the Military/Aerospace industry benefits from such concerns. The utilization of low-voltage logic in military and space systems is consistent with the use of VHSIC technology insertion into these systems. Lower-powered systems in space applications is of critical importance; reduction of the operating voltage extends the life of a satellite's battery system while reducing its size and weight. Low-voltage systems are less affected by EMI (Electromagnetic Interference) and EMP (Electromagnetic Pulse) radiation effects which would generate degradation in a system's performance. With the increased use of complex ASICs in Mil/Aero systems, either internally- or externally-generated noise can have disastrous effects since ⅔ of their surface is covered by metal lines that act as many miniature antennae. From a device performance consideration, low-voltage application minimizes the affects due to reduced internal electric field strength.

Past studies performed in non-radiation environments have characterized specifically-designed 5.0V product use in low-voltage applications. The results of these studies show a significant power savings, but at the cost of degrading the propagation delay performance. However, FACT™ JAN-S CMOS product is designed to operate between the 2 $V_{DC}$ and 6 $V_{DC}$ range. Although not specifically designed for 3.3 $V_{DC}$ application, this process allows acceptable levels of propagation delay times when used in low-voltage applications. Typical increases in propagation times range from 23% to 43% in a 3.0V non-radiation application. This paper addresses the performance of FACT product in a similar 3.0V application but in a total ionizing dose radiation environment as well as its impact in a low voltage operation.

1] This paper is unclassified. Work was performed under Contract No. MDA904-881-62266.

**PROCESS TECHNOLOGY**

Product discussed in this paper is fabricated using National Semiconductor's FACT JAN process. The starting material is N+ <100> for the substrate with an N-type <100> EPI layer. The EPI layer thickness is less than 8.0 μm.

MOSFET isolation is accomplished by using the LOCOS process for the field oxide (unhardened). The single polysilicon self-aligned gate process has a gate oxide thickness of 250 angstroms. The effective gate length for both P- and N- channel MOSFETS is 1.3 μm.

Two low temperature oxides are used for interlayer dielectrics. The dual-layer metalization process uses a sputtered AL-1.5% Si metal which is plasma etched. The PECVD silicon nitride is the final passivation layer. *Figure 1* shows the final cross section of this process.





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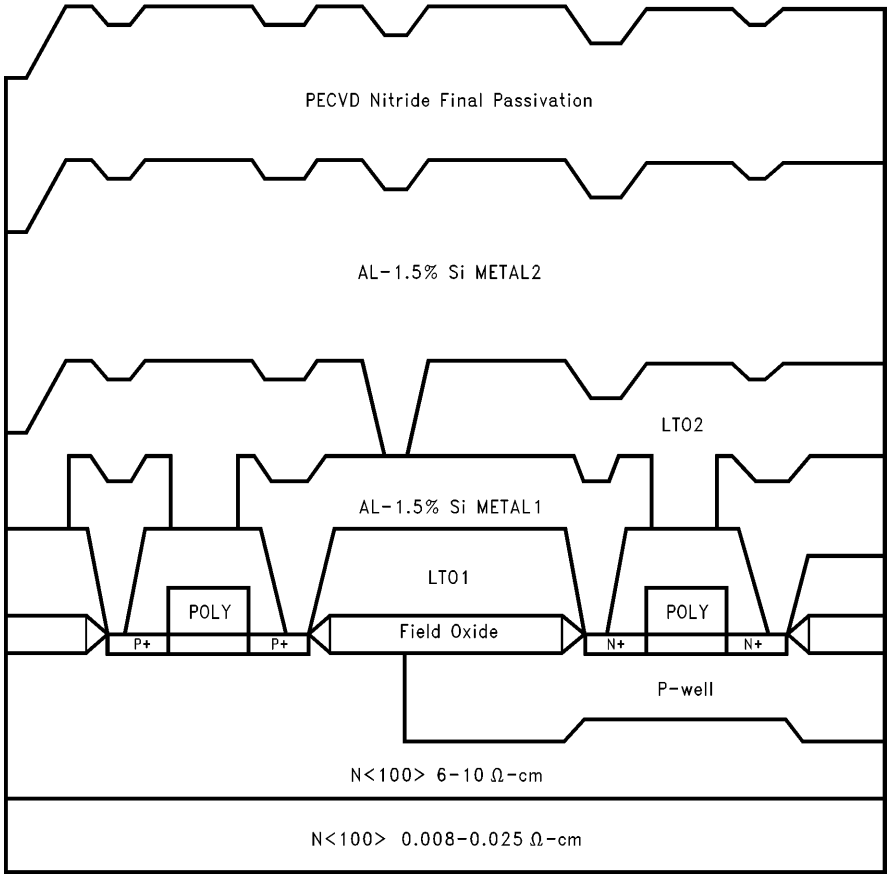


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**FIGURE 1. Cross Section of FACT JAN Product**

## TOTAL DOSE TEST METHODOLOGY

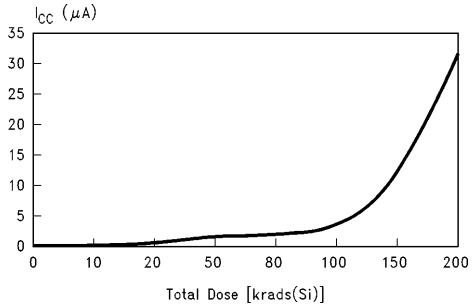
Total dose testing was conducted using MIL-STD-883D, Method 1019.4. The example demonstrated in this paper—the 54AC245—was biased such that inputs were high; the outputs were in the high impedance state (disabled) with no output loads. No remote power supply was employed during the period between radiation test levels. All pins were shorted during transportation between the AECL-220, Gammacell and MCT-2000 automatic tester. Post-irradiation parametric testing was performed within five minutes of each total dose irradiation level.

## DISCUSSION OF TEST RESULTS

Test results indicate that all test parameters were within the established pre-irradiation limits with the exception of $I_{CC}$ (standby current). Results have been reported and published for 5V operation, but not for low-voltage operation. The radiation-induced leakage current degraded in both operating conditions (3.3 $V_{DC}$ and 5 $V_{DC}$).

The results provided in this paper show a significant reduction in radiation-induced leakage currents (compare *Figures 2* and *3*). The radiation-induced current of low-voltage operation is reduced by a factor of eight at a total dose level of 100 krads(Si). The familiar non-linear radiation response of the standby current shown in *Figure 3* does not occur in low-voltage operation at total dose levels between 200–700 krads(Si).

**$I_{CC}$ (Standby) vs Total Dose**
**54AC245 - Octal Bidirectional**
**Transceiver with TRI-STATE I/O**

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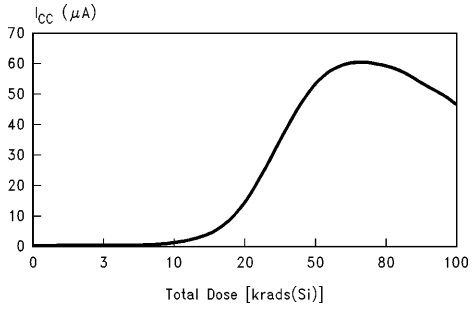
DOSE RATE - 120 rads (Si) TEMP: 25°C
RADIATION INPUT BIAS - HIGH—HIGH Z STATE
$V_{IN} = V_{CC} = 3.3\ V_{DC}$

**FIGURE 2. Low Voltage Total Dose Test**

**$I_{CC}$ (Standby) vs Total Dose**
**54AC245—Octal Bidirectional**
**Transceiver with TRI-STATE I/O**

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DOSE RATE - 119 rads (Si) TEMP: 25°C
RADIATION INPUT BIAS - HIGH—HIGH Z STATE
$V_{IN} = 5.0\ V_{DC}$, $V_{CC} = 5.5\ V_{DC}$

**FIGURE 3. High Voltage Total Dose Test**

*Figure 4*, a 54AC14 hex inverter circuit with a Schmitt trigger input, compares low-voltage versus high-voltage radiation biasing results for standby leakage current. For the same total dose level up to 100 krads(Si), the leakage current is significantly reduced between the high and low voltage result. For the high-voltage bias condition, a maximum current of 300 $\mu$A occurred at a total dose level of 50 krads(Si); the same value of standby leakage current under low-voltage radiation bias did not occur until approximately 350 krads(Si). For both radiation bias conditions, the maximum post-irradiation-parametric limit for JAN -S RHA-level R product was not exceeded.

**$I_{CC}$ (Standby) vs Total Dose**
**54AC14—Hex Inverter with**
**Schmitt Trigger Input**

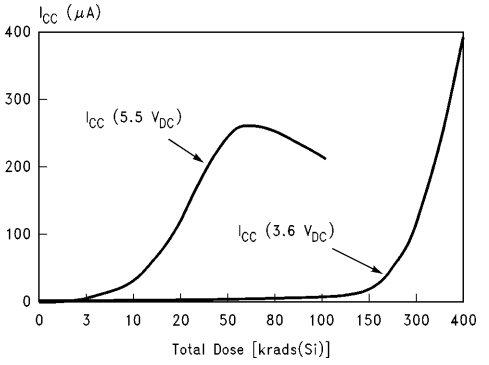


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**FIGURE 4. Low Voltage/High Voltage Total Dose Test—54AC14**

*Figure 5*, a 54AC161 Synchronous Presetable Binary Counter, shows similar radiation responses for the two different radiation bias conditions. Both figures demonstrate the impact of hole reduction due to the low-voltage biasing at total dose level less than 250 krads(Si).

**$I_{CC}$ (Standby) vs Total Dose**
**54AC161—Synchronous**
**Presetable Binary Counter**

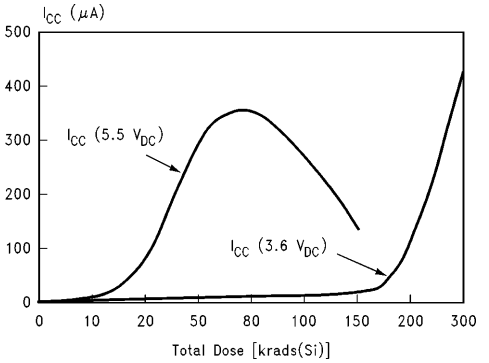


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**FIGURE 5. Low Voltage/High Voltage Total Dose—54AC161**

The only parameters of FACT-AC product that degrade from their pre-radiation values are standby leakage current ($I_{CC}$) and TRI-STATE leakage current ($I_{OZ}$). The magnitude of these radiation-induced leakage currents varies due to layout design values and type of transistor design.

The improvement in the radiation response of FACT product tested under low-voltage operation (3.0 $V_{DC}$–3.6 $V_{DC}$) is explained by these mechanisms:

(a) Charge trapping and its associated charge yield

(b) Interface state charge density

Both conditions are known to affect the electrical performance of a CMOS device in a total ionizing dose radiation environment.

Besides affecting parasitic leakage currents, total dose irradiation also degrades the threshold voltages and channel mobilities of CMOS devices. As ionizing radiation is accumulated, positive trapped charge (holes) is generated in both the gate and field oxides. The field oxide trapped charge causes generation of parasitic leakage paths. This occurs while the trapped charge in the gate oxide causes the p-channel's threshold voltage to increase (become more negative) as the n-channel's threshold voltage decreases. At some higher total dose level, it will rebound to a higher threshold voltage level than its pre-irradiation value. This eventually causes functional failure.

Holes that are generated and trapped in the oxide are the net charge that remains after the initial recombination. This initial recombination of charge occurs in a very short time—a few pico seconds. Net charge is a function of the electric field and temperature. This trapped hole charge contributes to the negative threshold voltage shift and interface-trap build up in CMOS devices [1].

At lower applied electric fields across the oxide, there is increased efficiency of electron-hole recombination. This is due to the smaller quantity of trapped holes that escapes initial recombination [1]. Attributable to the polysilicon gate of the FACT process, interface states build peaks between 1 MV/cm and 2 MV/cm and decrease at higher electric fields [2]. Under low-voltage operation, the applied electric field across the gate oxide is approximately 1.44 MV/cm. Although operating within optimal conditions for high efficient interface-state generation, the total dose radiation response for FACT product is much improved due to the yield production of trapped holes within the gate oxide.

Using low-voltage operation in radiation environments increases the total ionizing dose radiation capability of the device. The low-power supply voltage reduces the electric fields within the device's oxide, causing less generation of trapped oxide charge (TOC) and interface states. Diminishing these effects not only reduces the radiation-induced leakage current, but also minimizes transistor threshold voltage shifts. The total ionizing dose enhancement of the ''hot-electron'' effect is reduced.

*Figures 6* and *7* depict the propagation time for a particular timing parameter versus total dose. It must be noted that the propagation time for FACT product (54ACxxx) does not exceed the pre-irradiation parametric limit.

**54AC14—Hex Inverter with Schmitt Trigger Input**

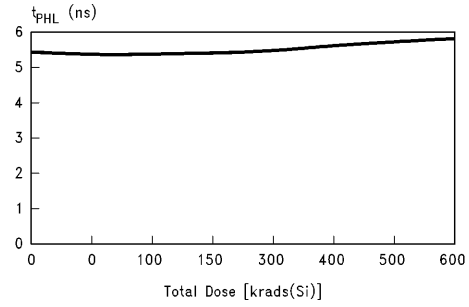


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**FIGURE 6. Low Voltage Total Dose Test—54AC14 Propagation Time Versus Total Dose**

**54AC161—Synchronous Presetable Binary Counter**

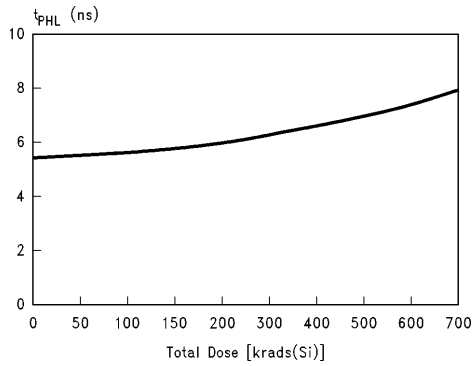


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**FIGURE 7. Low Voltage Total Dose - 54AC161 Propagation Time Versus Total Dose**

A review of radiation test data at low voltage bias conditions shows minimal propagation time differences between specified total dose levels for low-voltage and high-voltage radiation biasing. Table I shows differences in propagation times at a total dose level of 150 krads(Si) for the 54AC161 Synchronous Presetable Binary Counter. Data in this Table shows propagation times measured at 3.0 $V_{DC}$. Data indicates less radiation damage is generated at low-voltage irradiation with respect to propagation times.

**TABLE I. Comparison of Post Irradiation Propagation Times at Different Radiation Bias Conditions for 54AC161 Synchronous Presetable Binary Counter**

| Timing Parameter | 3.6 $V_{DC}$ Bias Prop. Time (ns) | 5.5 $V_{DC}$ Prop Time (ns) | % of Difference (%) |
|---|---|---|---|
| LH1 | 7.197 | 7.325 | 1.78 |
| LH2 | 8.955 | 9.186 | 2.58 |
| LH3 | 5.731 | 5.886 | 2.70 |
| HL1 | 5.753 | 5.889 | 2.36 |
| HL2 | 8.174 | 8.435 | 3.20 |
| HL3 | 6.684 | 6.618 | 1.00 |
| HL4 | 6.973 | 5.998 | 0.42 |
| HL5 | 8.750 | 8.891 | 1.58 |

For the exact same group of parts (54AC161) irradiated at low voltage to a total dose level of 700 krads(Si), Table II shows the percent of difference in propagation times from the pre-irradiation *mean* value. The propagation times were measured at two different operating voltages, $V_{CC}$ = 3 $V_{DC}$ and $V_{CC}$ = 4.5 $V_{DC}$.

**TABLE II. % of Difference in Propagation Times at Different Operating Voltages**

| Timing Parameter | $V_{CC}$ = 3.0 $V_{DC}$ % of Difference (%) | $V_{CC}$ = 4.5 $V_{DC}$ % of Difference (%) |
|---|---|---|
| LH1 | 38 | 14 |
| LH2 | 43 | 20 |
| LH3 | 46 | 25 |
| HL1 | 11 | 9 |
| HL2 | 9 | 6 |
| HL3 | 11 | 7 |
| HL4 | 9 | 8 |
| HL5 | 4 | 4 |

Based on the data shown in Table II, propagation times measured at $V_{CC}$ = 4.5 $V_{DC}$ show improvement over the same timing parameters measured at $V_{CC}$ = 3.0 $V_{DC}$. The results indicate that performing low-voltage irradiation then operating at a higher voltage minimizes the impact of total dose radiation damage on the circuit.

Functionally for FACT logic (54ACxxx) under low-voltage irradiation bias is between 1.4X to 2X better, as compared with the failure level at high-voltage operation.

Under high-voltage radiation bias, the threshold voltage shifts are more significant than at low-voltage irradiation. This is due to greater production of holes which result from the higher electric fields applied across the thermally-grown oxides [3]. When FACT product is irradiated under low-voltage radiation bias conditions, the applied electric fields across the gate and field oxides are decreased. In concert, fewer holes escape the electron-hole recombination mechanism and fewer holes are trapped at the $Si/SiO_2$ interface [4].

Typically, FACT product (54ACxxx) experiences functional failure at 350 krads(Si) under 5.5 $V_{DC}$ radiation bias condition. However, under low-voltage radiation bias conditions, similar product will functionally fail between 500 krads(Si) and 700 krads(Si).

Technical papers have recently published data that indicates significant interface state buildup for MOSFETs biased at zero volts. There are circumvention schemes which require ''powering-down'' of a system during passage through a radiation environment and at a later period of time, powering the system backup. This approach may not be an effective way to minimize the long-term buildup of interface traps [1].

## CONCLUSION

Data presented here provides system designers with an alternative to increase their system's radiation survivability. Using a programmable power supply in a low-voltage logic design application permits the digital system to operate through a total dose environment while minimizing the radiation damage to the CMOS digital devices. This is accomplished by reducing the power supply voltage to the system during passage through the radiation region and then returning to high-voltage operation. Similar techniques could also be applied to other radiation environments. Radiation-induced latchup performance is improved in single event and dose rate environments, but care must be employed when considering radiation-induced data upsets. Tradeoffs must be considered in determining the low-voltage value to be used due to data retention voltage levels.

The data presented in this paper supports the use of low-voltage logic product in military and space systems, and furnishes system designers with a viable alternative to nuclear/space radiation survivability of their systems.

**Note:** Radiation testing was performed on products manufactured using the FACT JAN-qualified process. Because the JAN process differs from the MIL-STD-883/SMD and commerical processes, non-JAN devices should not be presumed to exhibit similar performance.

## ACKNOWLEDGEMENTS

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