

# LM4250

*A Micropower Voltage Reference*



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# A Micropower Voltage Reference

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A low-drift voltage reference can be easily made by converting a zero temperature coefficient current to a voltage. JFETs biased slightly below pinch-off exhibit a zero temperature coefficient drain current ( $I_D$ ) as shown in *Figure 1*. With the above property and a micropower operational amplifier, used to convert the drain current to a voltage, a low power consumption voltage reference can be built as shown in *Figure 2*. The consumption of LM4250 op amp is programmed through resistor  $R_{SET}$ . Potentiometer P1 should be adjusted for low output ( $V_{REF}$ ) temperature coefficient. Actually, it can be trimmed for positive, negative or zero temperature coefficient. The output voltage is trimmed through P2 and it is expressed by:

$$V_{REF} = I_{D1} (P_2 + R_1 + R_2),$$

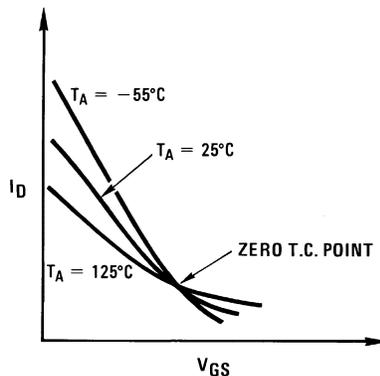
$$R_2 = R_3, I_{D1} \cong I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

With the values shown in *Figure 2*, the temperature coefficient of the output is 0.002%/°C and the overall standby current less than 100  $\mu$ A. The characteristics of the LM4250

are a function of its supply current, which depends on  $R_{SET}$ , and  $V^+$ .  $V^+$  can be provided by  $V_{REF}$  through the addition of a second FET, J2, shown in *Figure 3*. This way the parameters of the op amp will be independent of the unregulated input. The reference voltage can be taken from the wiper of the potentiometer P2 ( $V_{REF} = V^+$ ) or from the source of J2 ( $V_{REF} > V^+$ ). In the first case, the output impedance of the circuit is quite high and buffering may be required according to the application. The output impedance in the second case is low, essentially the  $1/g_m$  of (J2) divided by the loop gain of the circuit. In this case, a small temperature coefficient due to the supply current of the LM4250 is going to be added and be compensated for by an additional trimming of P1.  $V_{REF}$  is computed by:

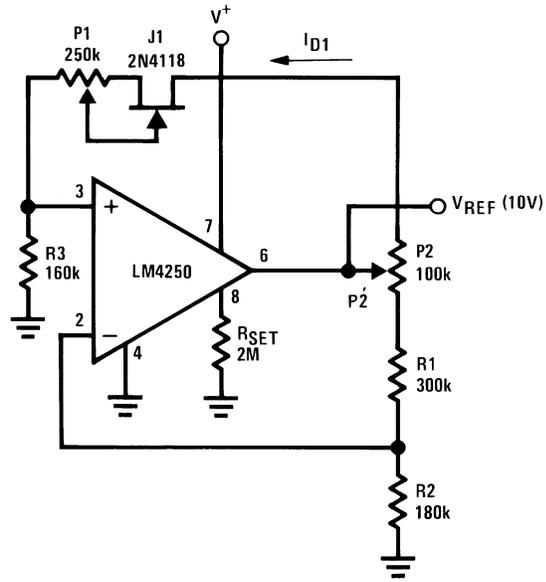
$$V_{REF} \cong I_{D1} [P_2 + R_1 + R_2] + P_2 [I_S + I_{D1}],$$

$$R_2 = R_3, I_S \cong \frac{6(V^+ - V_{BE})}{R_{SET}}$$



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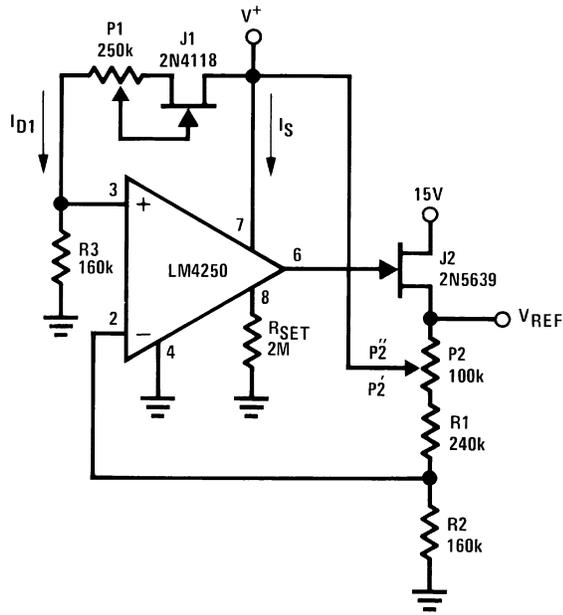
FIGURE 1. FET Transfer Characteristics



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P1 = Drift Adjust  
 P2 =  $V_{REF}$  Adjust

FIGURE 2. Basic Voltage Reference



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FIGURE 3. Improved Voltage Reference

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