Three elements of architectural change represent a new piece in the distributed-power puzzle

Literature Number: SNVA572

Technology Edge

Three elements of architectural change represent a new piece in the distributed-power puzzle

Paul Greenland, Director of Marketing, Analog Power Management

In recent years we have seen a revolution in the distributed-power architecture for the rapidly evolving information infrastructure. This article reviews three elements of this architectural change: the introduction of the intermediate bus architecture, the advent of digital control, and the trend toward the manageability of power at the point of load. Each element represents a new piece in the distributed-power puzzle, and an opportunity to take overall system availability and performance to the next level.

Intermediate bus architecture

Roughly five years ago, power management met an inflection point in system design. The forced-air-cooling budget for racks in telecom and datacom applications had reached a ceiling.

The proliferation of DSPs, FPGAs, and digital ASICs – driven by the endcustomer's insatiable thirst for bandwidth and content – had increased the number and complexity of loads to the point at which the conventional distributedpower architecture, shown in Figure 1, using a single isolated multi-output modular DC-DC converter (brick) on each card became a tapped-out resource. Individual load currents reached a level at which I*R drops in the PC-board traces between the single brick and each point of load contributed to voltage inaccuracies.
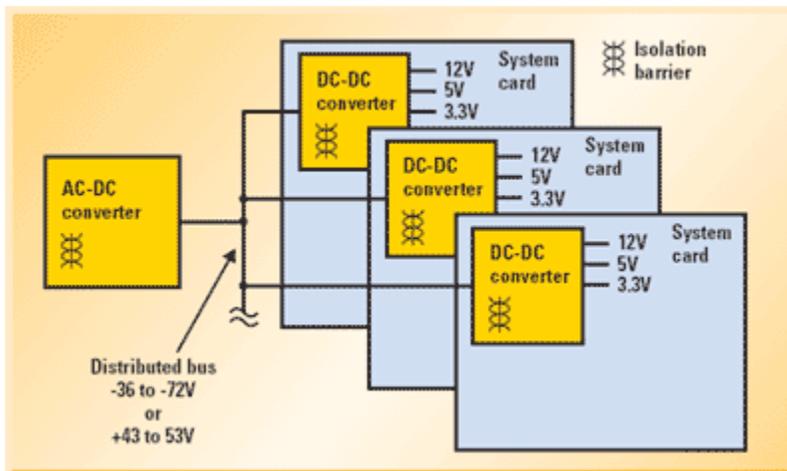

Figure 1: The conventional distributed-power architecture using a single isolated multi-output modular DC-DC converter on each card became a tapped-out resource

The answer was to separate the isolation, step-down, and point-of-load regulation into two distinct stages replacing the multi-output brick. This metamorphosis, illustrated in Figure 2, is not without its challenges; each stage has to occupy less than half the volume of the original solution and the series combination has to exhibit higher overall efficiency.

Typically the architecture uses a low-cost, loosely-regulated first stage, which performs the isolation and step-down function, with an efficient high-precision second stage close to the point of load. The first stage is called the Intermediate Bus Converter (IBC). The IBC is usually regulated against line voltage variation, by setting up a constant volt x second product in the power transformer. Load regulation is usually coarse, typically ±10%.
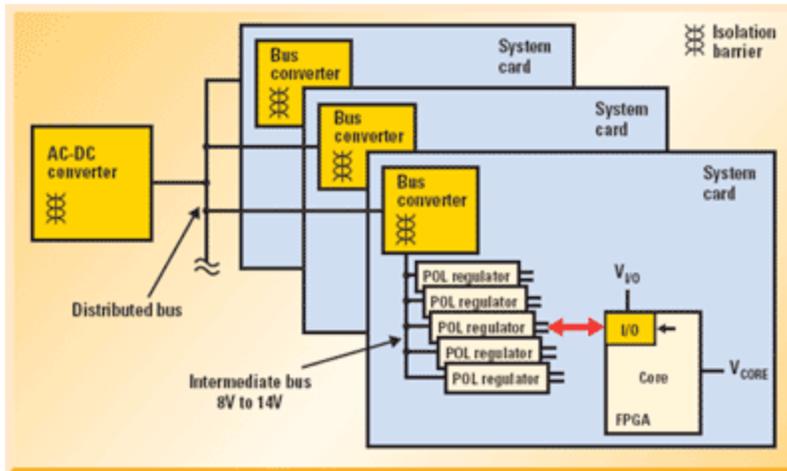
Figure 2: Each stage of the intermediate bus architecture has to occupy less than half the volume of the original solution

In many cases all regulation takes place on the primary side, monitoring the output voltage reflected through the turns-ratio to an auxiliary winding which also serves to power the primary control, drive, and regulation circuit after startup. Conversely, the regulators at the point of load have tight load regulation, typically less than ±1% and are not isolated. The primary distributed bus is -36 to -72V or +43 to 53V, for telecom or datacom, respectively. The intermediate bus is usually 8 to 14V.

This fundamental change in distributed-power architectures has stimulated a great deal of development in ICs, regulators, and modular DC-DC converters. Point-of-load regulators have been the subject of recent industry-sponsored efforts to establish a standard.

Three alliances[1] have been formed to establish common packaging and interface standards. This is also an area where traditional roles in the supply chain have changed; semiconductor manufacturers are manufacturing modular power converters and power supply manufacturers have started introducing chip-scale regulators with silicon content of their own design.

Digital power
Economy, flexibility, and reliability are the primary motivations for considering digital control. As process geometries have shrunk to smaller feature sizes, digital implementation can often be achieved in a smaller die area, with lower power consumption than its analog counterpart.

Digital control offers the promise of improved noise immunity and sophisticated, adaptive on-the-fly control allowing the power supply designer to consider power factor correction and resonant conversion topologies hitherto considered too complex for analog control. The transition to digital control is, however, a risky proposition.

Notoriously conservative power supply designers who have invested years of hard won experience in analog control have to learn to use a whole new vocabulary and toolset. Lead-lag compensation becomes Proportional-Integral-Derivative (PID) control. Sampling theory and time domain analysis are the norm and customers expect elaborate graphical user interfaces to input control coefficients and model power system performance.

Up to now, digital control has been focused on applications where the time constants in the load system have been long enough to permit real-time calculation of pulse width, and reference to lookup tables. An example is battery charging with power factor correction, such as the "rectifier" in a telephone exchange.

Another area where digital control is well established is in medical applications, where the FDA has stringent rules for the amount of energy delivered to the patient. In medical equipment, the repeatability and auto-calibration capability of digital control makes it a natural choice.

Power system manageability
As system engineers addressed the increase in the number and complexity of loads in the distributed-power architecture,

the issue of load power manageability arose. Complex loads, particularly FPGAs and DSPs, require separate supplies for core and I/O.

The core processor technology, where feature size is driven by Moore's Law, often operates at, or below 1V, while the I/O is held at a conventional potential (such as 3.3 or 5.0 V) by the communication interface standard. Since these subcircuits are often separated by a reverse-biased ESD diode in the IC, the power rails have to be applied and removed from the IC in a particular order, tracking one another to prevent latchup and potential destruction.

Furthermore, sophisticated loads often require "voltage margining" during automatic test procedures and may give an indication of their status and immediate power consumption for energy efficient application. An example of this type of technique is that of "run-time control" in which the voltage applied to a core tracks the clock frequency, effectively supplying the core with the exact energy it needs for a particular operating state. Power manageability includes the capability to dynamically configure the power supply to optimize a sensed parameter such as temperature, airflow or signal integrity, and to automatically compensate for the sensor's characteristics.

Integrated power system manageability was highlighted as a requirement once the real estate allocated in systems for discrete manageability approached that allocated to power delivery. This precious board area corresponds to lost content and bandwidth, driving the requirement for higher integration and ultimately a standard communications protocol for diagnostics, built-in test, and power system configuration. The need for high-power, high-reliability systems with fail-safe features is also driving this element.

In summary, power management is gaining recognition as a true enabling technology, capable of differentiating the performance of the final system. Consequently, semiconductor manufacturers with insight into the real value that effective power management brings are engaging with customers at the architectural stage of development, rather than at the tail end of the process when the ability to provide an optimal solution is heavily constrained. The latest developments in distributed-power architectures are prime examples of where timely collaboration can yield sustainable advantages.

To learn more about National's Power products, visit: power.national.com

[1]Distributed-power Open Standards Alliance (DOSA), Point-of-Load Alliance (POLA) and the Board Mounted Power Supplies (BMPS) project by the Power Supply Manufacturers Association (PSMA).

IMPORTANT NOTICE