Application Report
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Selecting an Ideal Ripple Generation Network for Your COT Buck Converter

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ABSTRACT

Fast transient response, simple control scheme, and low cost are features that distinguish Constant-On-Time (COT) buck converters from others. Simplicity of the control scheme is reflected in a single requirement for power electronics engineers: a design of a simple passive network that generates a low amplitude resistive ripple component at the feedback (FB) node that ensures a precise start of the on-time pulse. This application report provides a brief overview of the COT control scheme, derives components for the most common ripple generation networks, and discusses pros and cons of each network using an LM5166 low-I_Q synchronous buck converter design example.

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1 COT Overview

In simple terms, the Constant-On-Time (COT) control scheme depends on a timer circuit (ON-TIMER block) and a voltage comparator (COT Comparator block) to determine the precise timing of the buck switch (high-side MOSFET) and synchronous rectifier (low-side MOSFET) switching as illustrated in Figure 1.

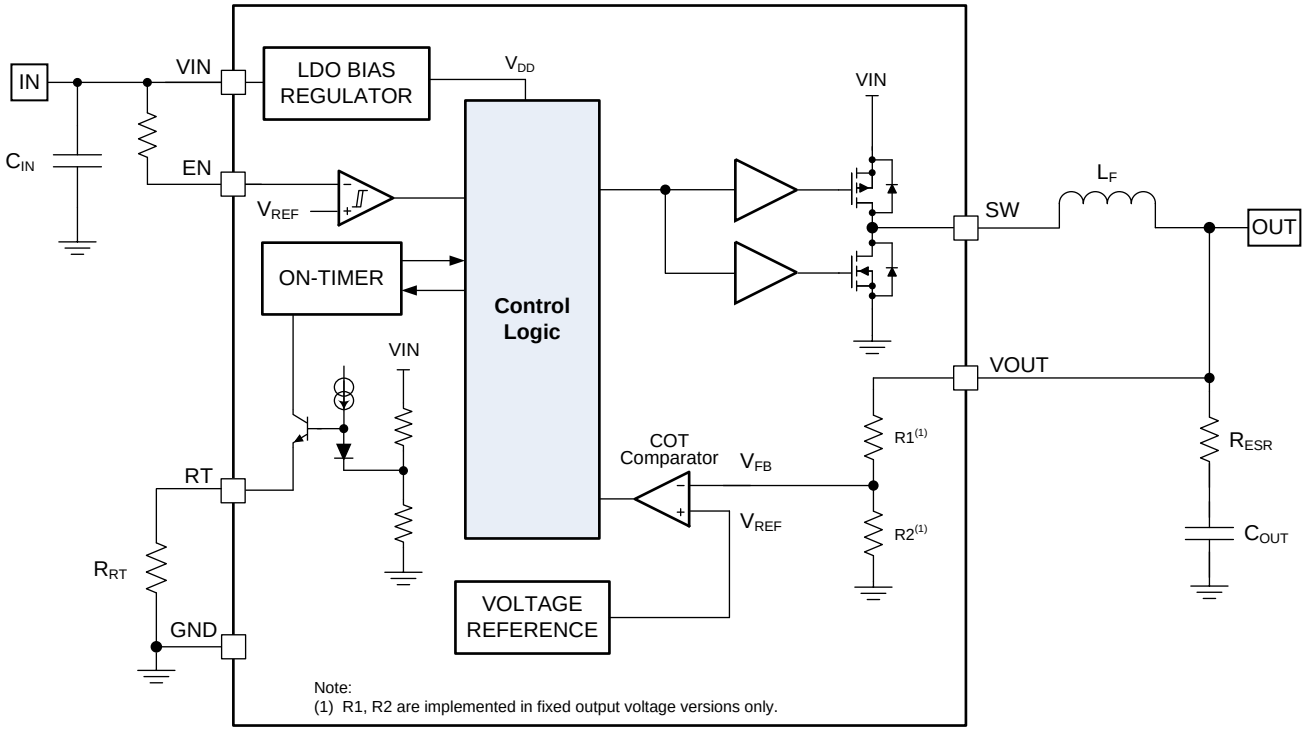


Figure 1. Simplified Block Diagram of a COT-Controlled Synchronous Buck Converter

The scheme uses a signal from the timer circuit to terminate the on-time. The signal is issued when a small current (µA range), which is proportional to the input voltage (V_{IN}) and an external resistor (R_{RT}), charges an internal capacitor above a pre-set voltage reference. For most COT-based converters, the PWM on-time, t_{ON}, is defined by Equation 1.

$$t_{ON} = \frac{k \cdot R_{RT}}{V_{IN}} \tag{1}$$

In Equation 1, k is a constant related to a specific on-timer implementation and may vary between COT buck converters. From a power supply designer's perspective, selecting the R_{RT} resistor based on a target switching frequency is all that is required.

The scheme registers the end of the off-time when the feedback voltage drops below the reference voltage. The off-time, t_{OFF}, is defined by Equation 2.

$$t_{OFF} = \frac{L_F \cdot \Delta I_L}{V_{OUT} + (R_{DCR} + R_{DSON}) \cdot I_{OUT}} \tag{2}$$

In Equation 2, L_F is the buck inductance, ΔI_L is the inductor peak-to-peak ripple current, R_{DCR} is the inductor DC resistance, and R_{DSON} is the on-state resistance of the buck converter's low-side switch.

For a precise termination of the off-time (or start of the on-time) and validity of Equation 2, the feedback voltage must decrease monotonically in phase with the inductor current. Furthermore, this change in feedback voltage during the off-time must be large enough to dominate any noise present at the feedback node. This can be accomplished with several passive circuits or networks to ensure a sufficient resistive ripple component is present on the feedback node. The following section discusses the most common ripple generation networks.

2 Ripple Generation Networks

There are three common ripple generation networks used with COT based buck converters: Type 1, 2, and 3. The following sections walk through the component selection process, present empirical data collected on the actual LM5166 circuits using these networks, and discuss the results.

2.1 Type 1 Network

Type 1 ripple generation network uses a single R_{ESR} resistor in series with the output capacitor as shown in Figure 2, an example of a 5-V, 500-mA buck converter that uses LM5166X (a 5-V fixed output voltage option). The network can be used with either fixed output (internal feedback resistors) or adjustable output (external feedback resistors) device options and is the simplest and most economical to implement.

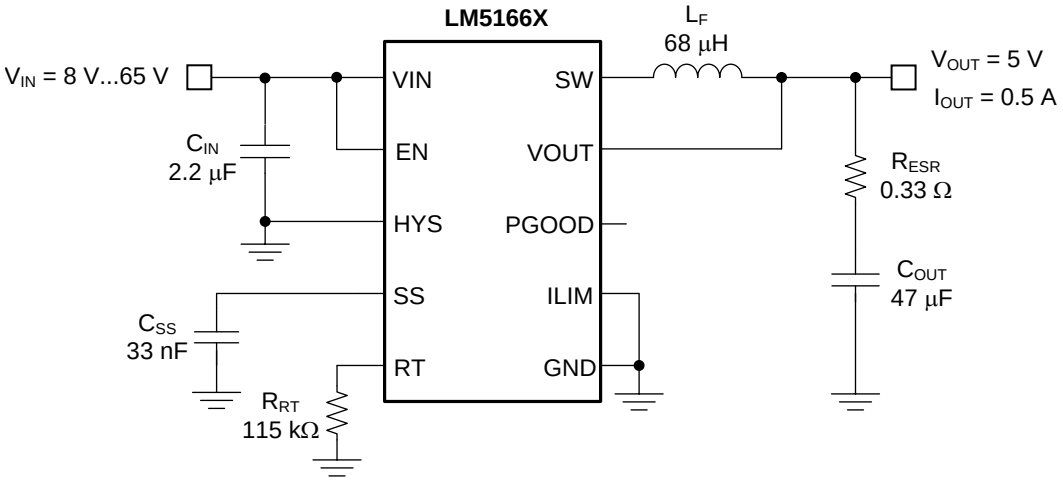


Figure 2. Synchronous Buck Converter Circuit With Type 1 Ripple Generation Network, $V_{IN(nom)}$ = 24 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 250 kHz

For the circuit shown in Figure 2, the output voltage ripple has two components:

- Capacitive ripple caused by the inductor ripple current charging or discharging the output capacitor.
- Resistive ripple caused by the inductor ripple current flowing through the ESR of the output capacitor and series resistor R_{ESR}

The capacitive ripple component is 90º out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters with multiple on-time bursts in close succession, followed by a long off-time (a characteristic of hysteretic converters). Equation 3 and Equation 4 define the value of the R_{ESR} resistance that presents the required amplitude and phase of the ripple at the feedback node.

$$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}} \quad (3)$$

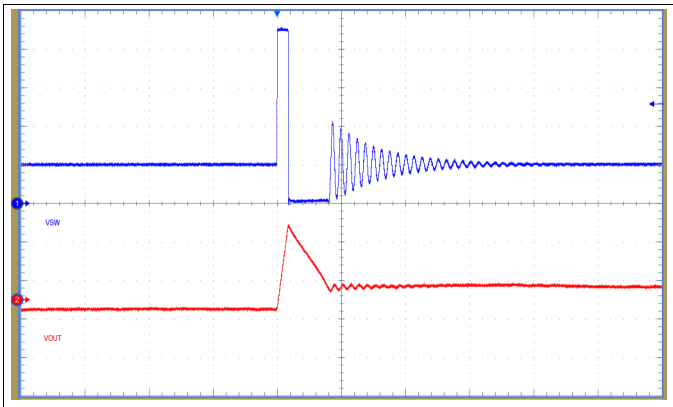
Equation 3 defines the minimum R_{ESR} that ensures a 20-mV resistive ripple component is present at the feedback node. For the LM5166, the 20-mV term is conservatively selected based on the feedback voltage comparator hysteresis of 4 mV (typical). Note that other COT buck converters may have different comparator hysteresis, therefore the term may need to be adjusted accordingly. The comparator monitors the feedback node voltage and signals the control logic when the voltage drops below the reference (V_{FB1} = 1.223 V). Other COT converters may use different values for the minimum feedback node ripple requirement, depending on the comparator hysteresis and the expected noise at the feedback node.

$$R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}} \quad (4)$$

Equation 4 ensures that the generated ripple on the feedback node is in phase with the inductor current. In most cases, Equation 3 dictates the selection of R_{ESR} while Equation 4 becomes important at low V_{IN} values.

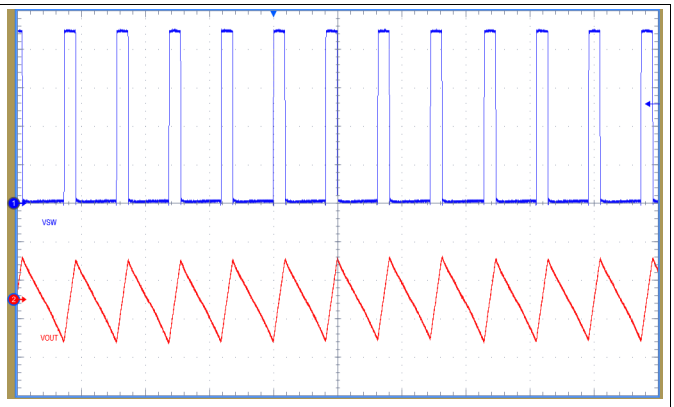
For the circuit shown in Figure 2, the R_{ESR} is derived at an input voltage V_{IN} of 24 V. At a V_{IN} of 12 V, the amplitude of the ripple on the feedback node drops to approximately 14 mV given the same R_{ESR} of 0.33 Ω. This is still sufficient for stable operation of the circuit provided that minimal noise is present at the feedback node. As the V_{IN} drops further, the ripple on the feedback eventually becomes less than 4 mV. At this point, the circuit stops behaving as a COT based converter and transitions to hysteretic behavior. A general recommendation is to derive R_{ESR} at the typical V_{IN} while ensuring at least 12 mV of ripple is present at the minimum V_{IN}. This approach gives the lowest output ripple with the Type 1 ripple generation network. A more conservative approach is to derive the R_{ESR} at the minimum V_{IN} yielding a higher output voltage ripple at the nominal and maximum V_{IN} operating conditions.

The following figures show the steady-state and transient load performance of the converter circuit shown in Figure 2. The peak-to-peak output voltage ripple measurement (ΔV_{OUT}) is given for each figure as well.



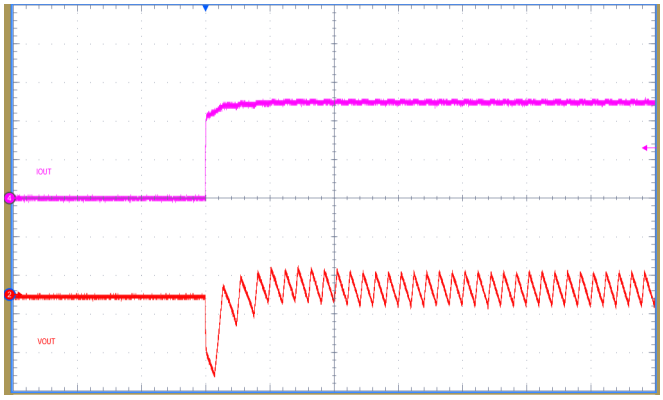
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 40 mV/Div
ΔV_{OUT} = 90 mV

Figure 3. Type 1 Network: No Load Switching Waveforms



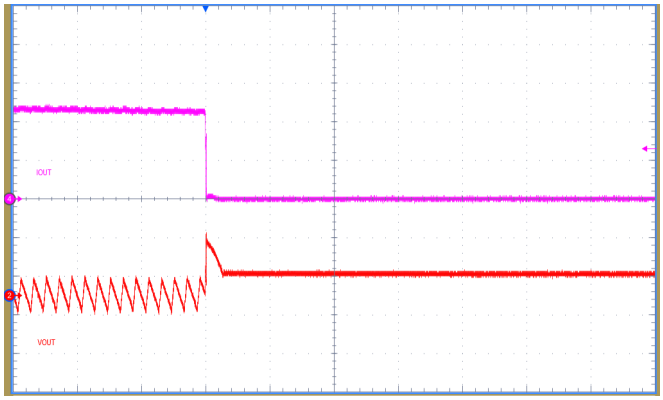
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 40 mV/Div
ΔV_{OUT} = 90 mV

Figure 4. Type 1 Network: 300-mA Load Switching Waveforms



Time Scale: 20 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 288 mV

Figure 5. Type 1 Network: Load-ON Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 0 mA to 500 mA at 2 A/µs



Time Scale: 20 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 212 mV

Figure 6. Type 1 Network, Load-OFF Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 500 mA to 0 mA at 2 A/µs

As Figure 3 and Figure 4 exemplify, the output voltage ripple with Type 1 network is less than 2% under light-load conditions as well as when in operating in CCM. The load transient response settling time is very short (approximately $1/F_{SW}$) while transient peak deviation from the regulated voltage is acceptable (<5%) as shown in Figure 5 and Figure 6.

2.2 Type 2 Network

Type 2 ripple generation network uses a C_{FF} capacitor in addition to the R_{ESR} resistor. As the output voltage ripple is AC-coupled by C_{FF} to the feedback node, the R_{ESR} value and ultimately the output voltage ripple are reduced by a factor of V_{OUT} / V_{FB} as shown in Figure 7, an example of a 5-V, 500-mA buck converter with a Type 2 ripple network. The network can be used only with adjustable output (external feedback resistors) device options.

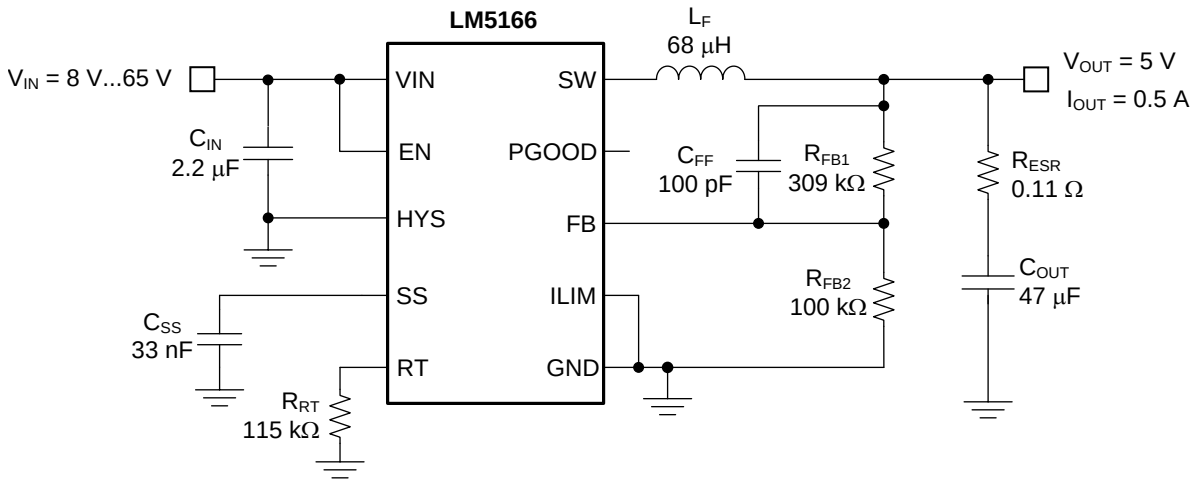


Figure 7. Synchronous Buck Converter Circuit With Type 2 Ripple Generation Network, $V_{IN(nom)}$ = 24 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 250 kHz

For the circuit shown in Figure 7, Equation 5, and Equation 6 define the value of the R_{ESR} resistor that ensures required amplitude and phase of the ripple at the feedback node.

$$R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}} \tag{5}$$

Similar to Equation 3, Equation 5 defines the minimum R_{ESR} that ensures a 20-mV ripple is present at the feedback node. The 20 mV term in the equation can be used for both the LM5165 or LM5166 buck converter circuits. Other COT converters may require different values depending on the comparator hysteresis and the expected noise on the feedback node.

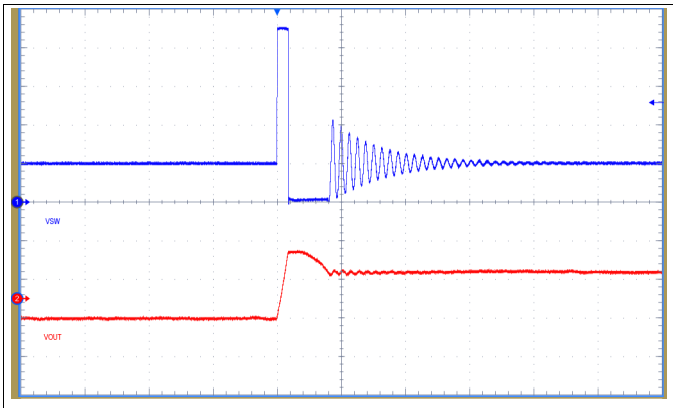
$$R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}} \tag{6}$$

Equation 6 is the same as Equation 4. It is displayed here for the completeness of the equation set for this section of the report. For the circuit shown in Figure 7, the R_{ESR} is derived at the nominal input voltage of 24 V. The selected value of 0.11 Ω is slightly higher than the minimum calculated and gives a calculated ripple of 25 mV. At an input voltage of 12 V, the amplitude of the ripple at the feedback node drops to approximately 19 mV given the same R_{ESR} of 0.11 Ω. The generated ripple at FB is sufficient for stable circuit operation at both 12 V and 24 V input voltages. As the V_{IN} drops further, the ripple at the feedback node eventually becomes less than 4 mV and the circuit transitions to hysteretic behavior. Similar to Type 1 network recommendations, a general recommendation for the Type 2 network is to derive the R_{ESR} value at the typical V_{IN} while ensuring at least 12 mV of ripple is present at minimum V_{IN}. A more conservative approach is to derive the R_{ESR} value at the minimum V_{IN}, yielding a slightly higher output voltage ripple when operating at nominal and maximum V_{IN}.

$$C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \,||\, R_{FB2})} \tag{7}$$

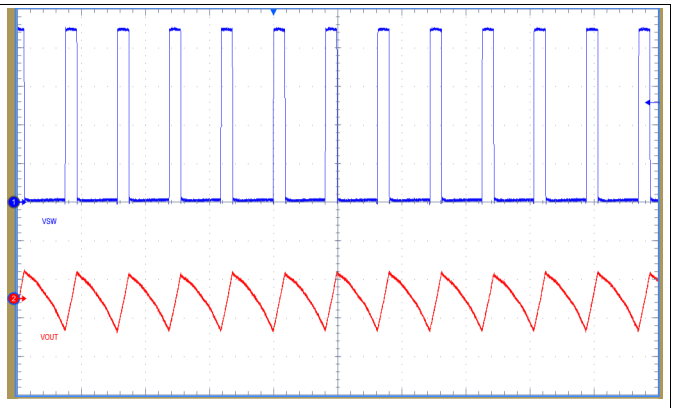
Equation 7 defines the minimum feed-forward capacitance, C_{FF}. For the circuit in Figure 7, the C_{FF} is derived at the nominal switching frequency, F_{SW}, at full load and V_{IN} of 24 V. The selected C_{FF} of 100 pF is an order of magnitude greater than the calculated value to ensure minimal phase shift of the voltage ripple at the feedback node while maintaining acceptable transient response.

The following figures show steady-state and transient load performance of the converter circuit shown in Figure 7. The peak-to-peak output voltage ripple measurement (ΔV_{OUT}) is given for each figure as well.



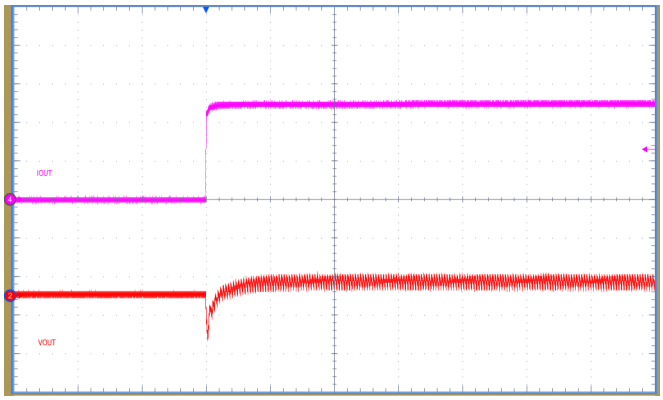
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 20 mV/Div
ΔV_{OUT} = 37 mV

Figure 8. Type 2 Network: No Load Switching Waveforms



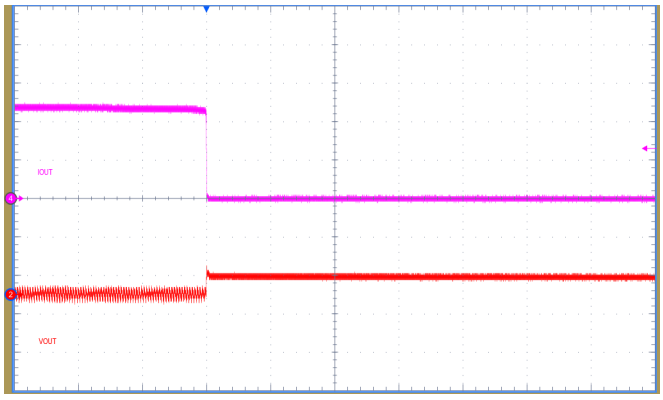
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 20 mV/Div
ΔV_{OUT} = 32 mV

Figure 9. Type 2 Network: 300-mA Load Switching Waveforms



Time Scale: 100 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 180 mV

Figure 10. Type 2 Network: Load-ON Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 0 mA to 500 mA at 2 A/µs



Time Scale: 100 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 100 mV

Figure 11. Type 2 Network: Load-OFF Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 500 mA to 0 mA at 2 A/µs

As Figure 8 and Figure 9 exemplify, the output voltage ripple with a Type 2 network can be as low as 20 mV when operating in CCM. The transient load response settling time is acceptable while deviation from the regulated voltage setpoint is good (<2%) as shown in Figure 10 and Figure 11.

2.3 Type 3 Network

A Type 3 ripple generation network uses an RC filter consisting of R_A and C_A, and the switch node voltage (V_{SW}) to generate a triangular ramp that is in phase with the inductor current. This triangular ramp is then AC-coupled into the feedback node with the capacitor C_B as shown in Figure 12, an example of a 5-V, 500-mA buck converter with Type 3 ripple network. Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is crucial. The network can only be used with adjustable output (external feedback resistors) device options.

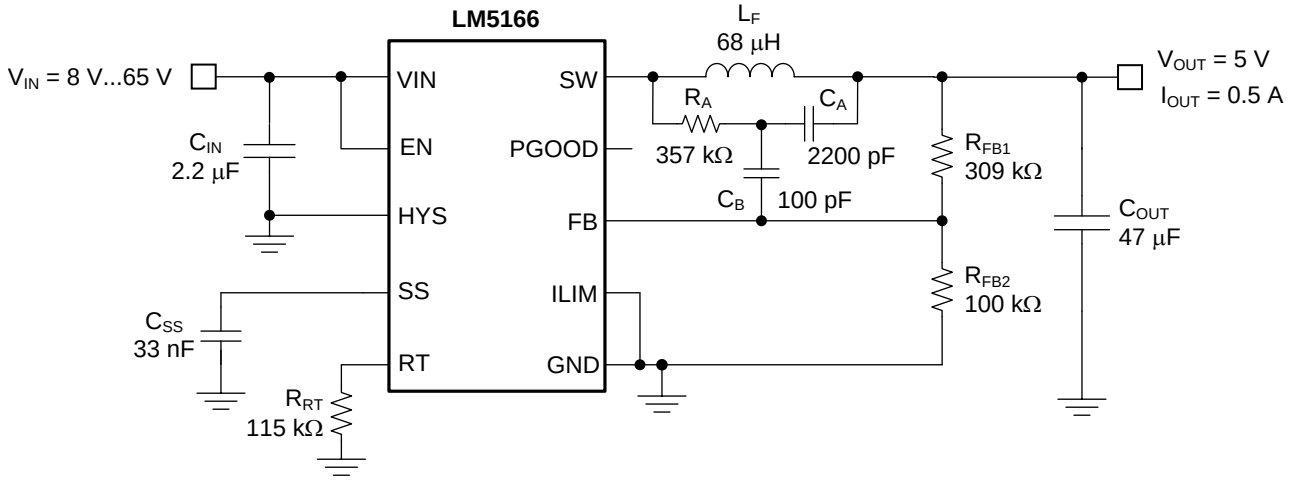


Figure 12. Synchronous Buck Converter Circuit With Type 3 Ripple Generation Network, $V_{IN(nom)}$ = 24 V, V_{OUT} = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 250 kHz

Equation 8 and Equation 9 define the values of the R_AC_A filter components to provide the required amplitude and phase of the ripple at the feedback node.

$$C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \,||\, R_{FB2})} \tag{8}$$

For the circuit of Figure 12, the minimum C_A is calculated at the nominal switching frequency (F_{SW}) at full load and V_{IN} of 24 V. A capacitance of 2200 pF is selected so that the value of R_A is within practical impedance range (typically 100kΩ < R_A < 1 MΩ for low-I_Q converters) while meeting the minimum value defined by Equation 8. Capacitor values of 1000 pF and 3300 pF are acceptable as well.

$$R_AC_A \leq \frac{(V_{IN\text{-}nom} - V_{OUT}) \cdot T_{ON\,(@V_{IN\text{-}nom})}}{20\,mV} \tag{9}$$

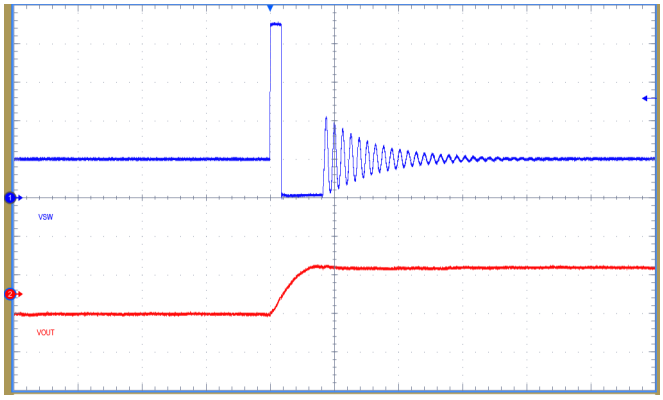
Based on Equation 9 and with C_A of 2200 pF, the R_A value of 357 kΩ ensures a 20-mV ripple component at the feedback node. This value is calculated at a V_{IN} of 24 V. At a V_{IN} of 12 V, the amplitude of the ripple at the feedback node drops to approximately 15 mV given the same R_A and C_A component values. Similar to recommendations for Type 1 and Type 2 networks, a general recommendation for a Type 3 network is to derive the R_A and C_A components at the typical V_{IN} while ensuring at least 12 mV of ripple is present at minimum V_{IN}. A more conservative approach is to derive the component values at minimum V_{IN}.

While the amplitude of the generated ripple does not affect the output voltage ripple, it slightly impacts the output load regulation by approximately a half of the increase in the amplitude of the generated ripple. For example, a converter circuit with Type 3 network that generates a 40-mV ripple component at the feedback node will have approximately 20 mV worse load regulation than the same circuit with Type 3 network that generates a 20-mV ripple at the feedback node.

$$C_B \geq \frac{T_{TR-Settling}}{3 \cdot R_{FB1}} \tag{10}$$

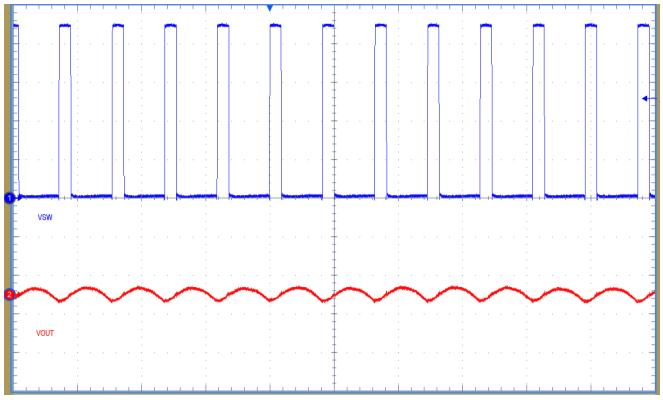
Equation 10 defines the coupling capacitance, C_B, based on the load transient response settling time, $T_{TR–Settling}$. For the circuit in Figure 12, C_B is derived based on a settling time of 50 µs. The selected capacitance for C_B of 100 pF is high enough to avoid excessive discharge during sleep intervals when operating at light loads. Use a C0G or NPO dielectric for C_B to avoid capacitance falloff with applied DC voltage.

The following figures show steady-state and transient load performance of the buck converter circuit in Figure 12. The peak-to-peak output voltage ripple measurement (ΔV_{OUT}) is given for each figure as well.



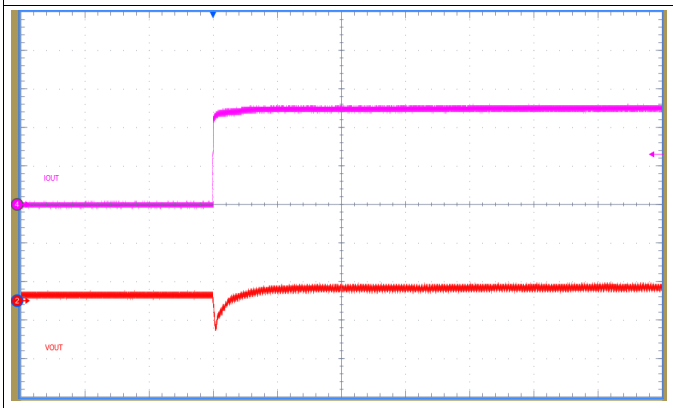
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 20 mV/Div
ΔV_{OUT} = 27 mV

Figure 13. Type 3 Network: No Load Switching Waveforms



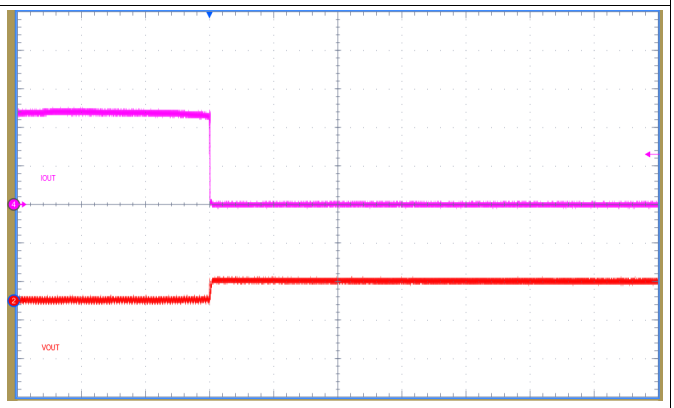
Time Scale: 5 µs/Div
CH1: V_{SW}, 5 V/Div
CH2: V_{OUT}, 20 mV/Div
ΔV_{OUT} = 10 mV

Figure 14. Type 3 Network: 300-mA Load Switching Waveforms



Time Scale: 100 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 124 mV

Figure 15. Type 3 Network: Load-ON Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 0 mA to 500 mA at 2 A/µs



Time Scale: 100 µs/Div
CH4: I_{OUT}, 200 mA/Div
CH2: V_{OUT}, 100 mV/Div
ΔV_{OUT} = 72 mV

Figure 16. Type 3 Network: Load-OFF Transient, V_{IN} = 24 V, V_{OUT} = 5 V, 500 mA to 0 mA at 2 A/µs

As Figure 13 and Figure 14 exemplify, the output voltage peak-to-peak ripple with a Type 3 network can be less than 10 mV when operating in CCM. Figure 15 and Figure 16 confirm that the transient load response duration is acceptable and the peak deviation from the regulated output voltage setpoint is good (<2%).

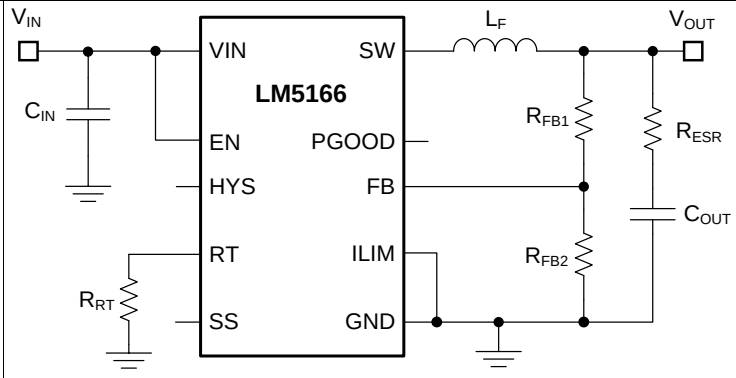
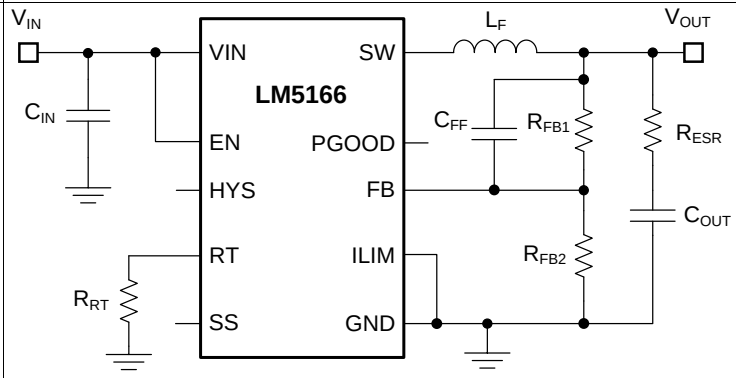
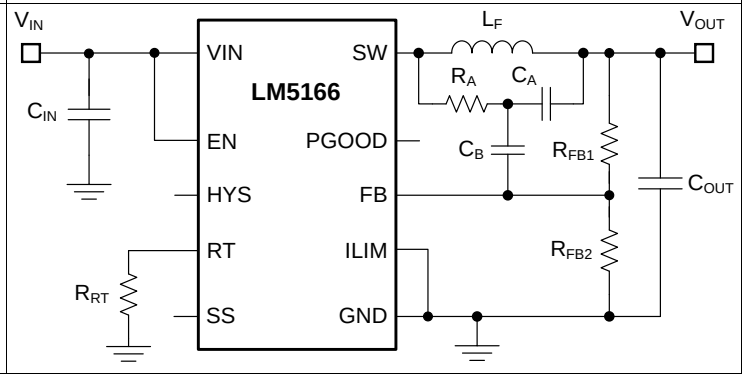
3 Summary

Constant-On-Time buck converters require a small resistive ripple at the feedback node (FB) for proper operation. A Type 1 network consisting of a single resistor in series with the output capacitor ensures sufficient ripple is present. With a few extra passive components (Type 2 or Type 3), the output voltage ripple can be brought to levels that can satisfy the most stringent output voltage ripple requirements.

Table 1. Summary of Ripple Generation Networks

TYPE 1	TYPE 2	TYPE 3
Supports Fixed or Adjustable V_{OUT} Options	Supports Adjustable V_{OUT} Options	Supports Adjustable V_{OUT} Options
Consists of a single component: R_{ESR}	Consists of two components: R_{ESR} and C_{FF}	Consists of three components: R_A, C_A and C_B
Ripple at V_{OUT} ≥ 1%	Ripple at V_{OUT} ≥ 12 mV	Ripple at V_{FB} ≥ 12 mV, Ripple at V_{OUT} ~0 mV
Fastest transient response	Fast transient response	Fast transient response

Table 2. Ripple Generation Circuits and Relevant Expressions

TYPE	SCHEMATIC	CALCULATION
Type 1 Lowest Cost		$R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ (11) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (12)
Type 2 Reduced Ripple		$R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}}$ (13) $R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (14) $C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (15)
Type 3[1] Lowest Ripple		$C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (16) $R_A C_A \leq \frac{(V_{IN\text{-}nom} - V_{OUT}) \cdot T_{ON\,(@V_{IN\text{-}nom})}}{20mV}$ (17) $C_B \geq \frac{T_{TR-Settling}}{3 \cdot R_{FB1}}$ (18)

(1) Lin, Min and others, "Frequency Domain Analysis of Fixed On-Time With Bottom Detection Control for Buck Converter," IEEE IECON 2010, pp. 481–485.

4 References

- *LM5166 3-V to 65-V Input, 500-mA Output, Synchronous Buck Converter with Ultra-Low I_Q* (SNVSA67)
- *LM5166 Quickstart Design Tool*
- *AN-1481: Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs* (SNVA166)
- Lin, Min and others, "Frequency Domain Analysis of Fixed On-Time With Bottom Detection Control for Buck Converter," IEEE IECON 2010, pp. 481–485.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2017) to A Revision	Page
• Changed Equation 10	7
• Added Table 2	9

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