Application Report
SNVA835B–July 2018–Revised May 2019

Inverting Application for the LMZM33604/6

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ABSTRACT

The LMZM33606 is a 16 × 10 mm^2 6-A rated synchronous step-down power module that features a wide operating input range from 3.5 V to 36 V with adjustable output voltage range from 1 V to 20 V. The LMZM33606 can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted or negative with respect to input voltage. This application report shows how the conventional non-inverting evaluation board for the LMZM33606 can be configured for an inverting application. This application note also provides the additional level-shifter circuitry for EN and PGOOD pin if the feature is required. Note that the LMZM33604 is rated for 4A and pin-to-pin compatible with the LMZM33606.

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1 Inverting Buck-Boost Topology

1.1 Concept

In a standard buck configuration the positive connection (V_{OUT}) is connected to the internal inductor, and the return connection is connected to the device ground.

In the IBB configuration, SYS_GND is connected to device V_{OUT} and the device return is now the negative output voltage (nVOUT). This shift in topology allows the output voltage to be inverted with respect to the input voltage.

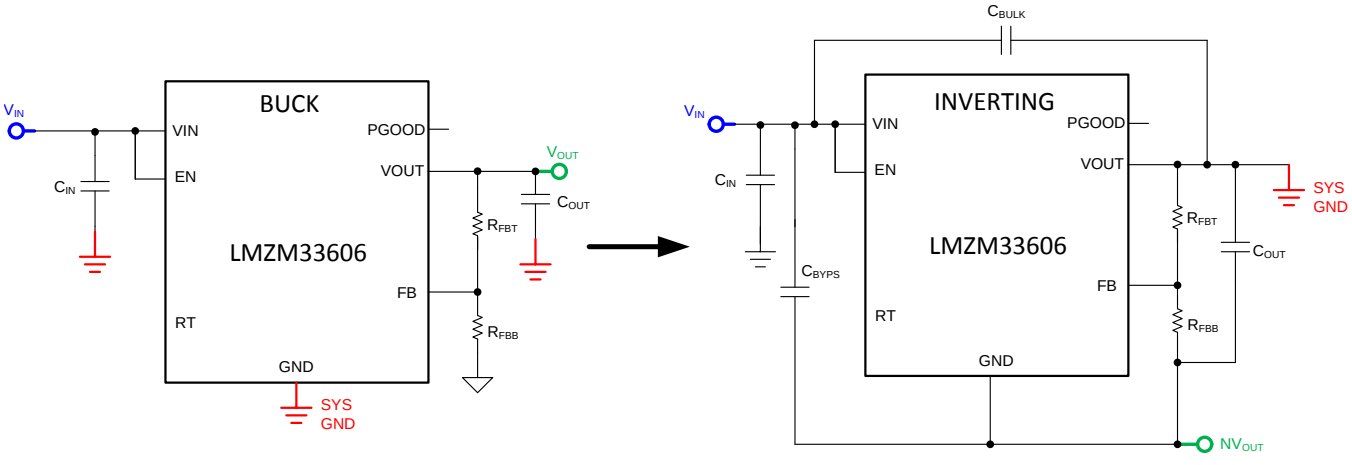


Figure 1. Converting From Buck to Inverting Buck Boost Topology

1.2 Output Current Calculations

By changing the buck configuration into an IBB configuration, the average inductor current is affected. The output current capability in the IBB topology is less than the buck configuration. The maximum achievable current is calculated by the following:

I_{OUT} (IBB) = I_{L_max} × (1 – D)

- I_{L_max} is the maximum rated inductor current
- D is the operating duty cycle

(1)

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2:

$$D = \frac{Vout}{Vout - Vin * \eta} \quad (2)$$

NOTE: V_{OUT} in Equation 2 is represented with a negative value.

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. Given that the IBB configuration yields an efficiency range of 70% to 85%, the conservative value of 70% is used for calculating the duty cycle. Use Equation 1 and Equation 2 to calculate the recommended maximum output current. For example a 24-V input voltage, –12-V output voltage system, the duty cycle is:

$$D = \frac{-12}{-12V - 24 * 0.7} = 0.4166 \quad (3)$$

The result of Equation 3 is then used to calculate the maximum achievable output current:

$$I_{OUT}\ (IBB) = 6 \times (1 - 0.4166) = 3.5A \quad (4)$$

Table 1 and Figure 2 provides a general idea of the maximum output current allowed from the modified LMZM33606.

Table 1. Maximum Output Current Calculation for LMZM33606

V_{OUT} (V)	V_{IN} (V)	IL_max (A)	η	D	I_{OUT} (A)
-1.2	24	6	0.7	0.066	5.6
-1.8	24	6	0.7	0.096	5.4
-2.5	24	6	0.7	0.130	5.2
-3.3	24	6	0.7	0.164	5.0
-5	24	6	0.7	0.230	4.6
-12	24	6	0.7	0.417	3.5

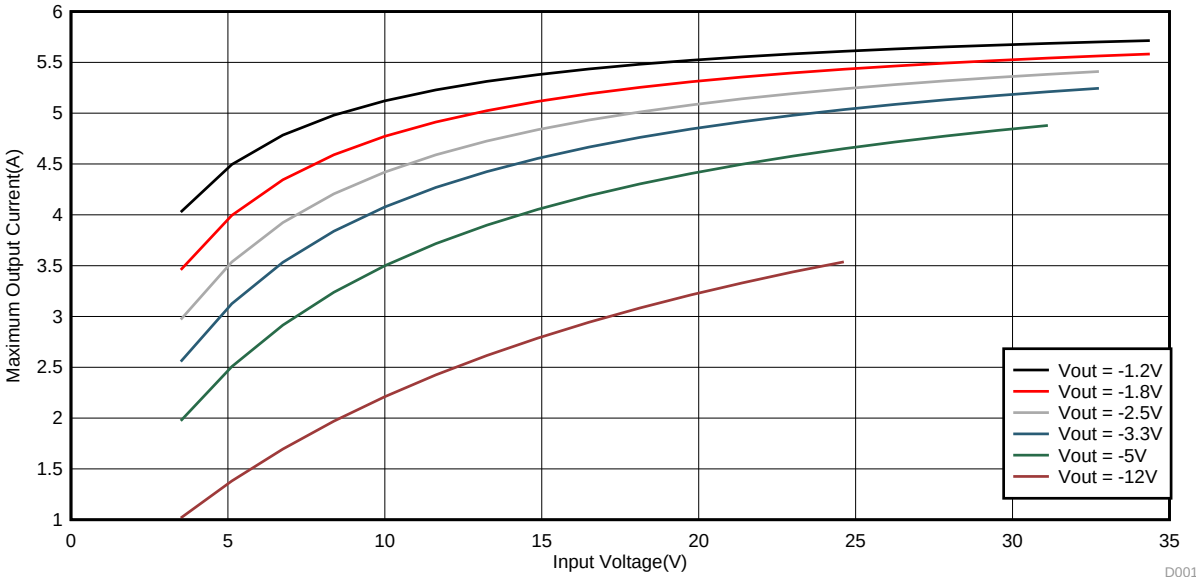


Figure 2. Recommended Maximum Output Current for LMZM33606

Table 2. Maximum Output Current Calculation for LMZM33604

V_{OUT} (V)	V_{IN} (V)	IL_max	η (%)	D	I_{OUT} (A)
-1.2	24	4	0.7	0.066	3.7
-1.8	24	4	0.7	0.096	3.6
-2.5	24	4	0.7	0.130	3.5
-3.3	24	4	0.7	0.164	3.3.3
-5	24	4	0.7	0.230	3.1
-12	24	4	0.7	0.417	2.3

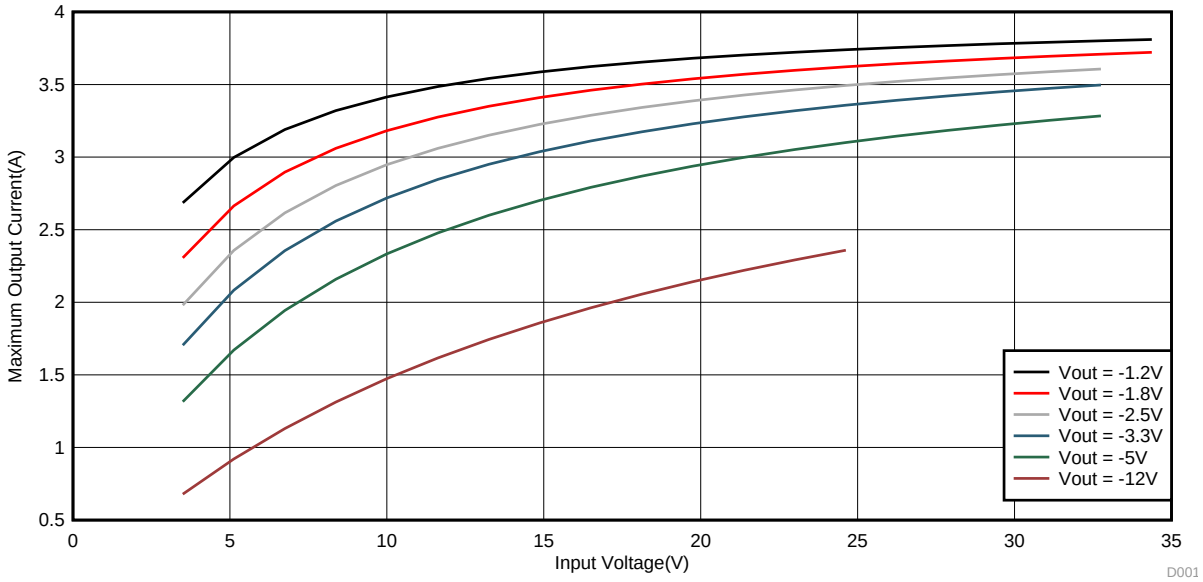


Figure 3. Recommended Maximum Output Current for LMZM33604

1.3 V_{IN} and V_{OUT} Range In Inverting Configuration

When configured in an IBB topology, the input voltage across the module is V_{IN} to V_{OUT} effectively limiting the input voltage range. The LMZM33606 has an input voltage range from 3.5 V to 36 + V_{OUT}, where V_{OUT} is a negative value. For example, for an output voltage of –12V the maximum input voltage is 24V. The output voltage range in this topology is –1 V to –20 V.

2 Design Considerations

2.1 Additional Bypass Capacitor and Schottky Diode

Use a ceramic bypass capacitor, C_{BYPS}, with a minimum capacitance of 10 µF. The voltage rating must be taken into consideration because this capacitor will experience stress equal to the full voltage range between V_{IN} and V_{OUT}.

In order for the sytem to be stable, there must be an input power supply capacitor to help dampen the high-frequency noise that can couple onto the circuit. An electrolytic capacitor with moderate ESR helps dampen any input supply ringing caused by long power leads. When using the LMZM33606EVM, C_{BULK} capacitor should be added across V_{IN} and SYS_GND.

Consider that the inclusion of the C_{BYP} capacitor introduces an AC path from V_{IN} to V_{OUT} and might worsen the transient response. When V_{IN} is applied to the circuit, this dV/dt across the bypass capacitor creates a current that must return to ground to complete the loop. This current might flow through the internal low-side body diode of the MOSFET and the inductor to return to ground. For this case, it is recommended to have a Schottky diode between NV_{OUT} and SYS GND. If large line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

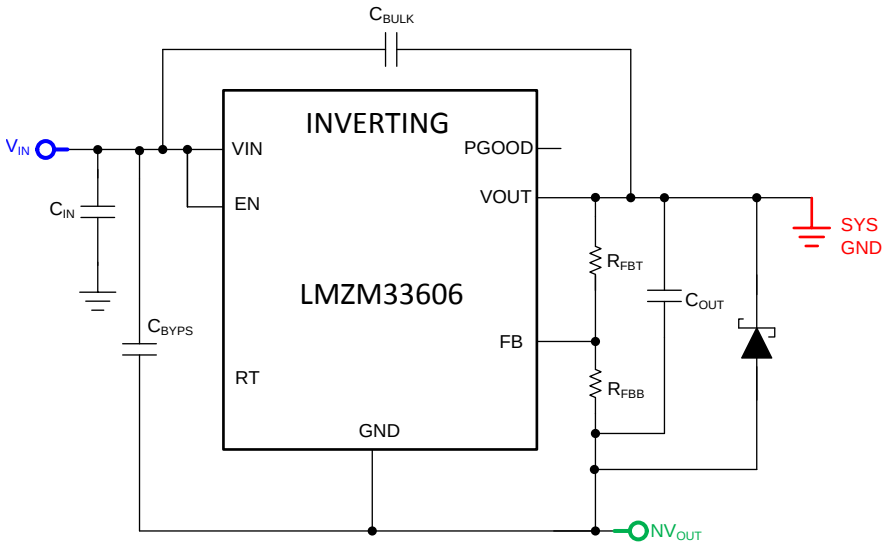


Figure 4. LMZM33606 Inverting Buck-Boost Schematic With Schottky Diode

2.2 Start-up Behavior and Switching Node Consideration

The voltage on the SW pin switches from V_{IN} to V_{OUT} in an inverting topology instead of from V_{IN} to GND in a buck topology. When the high-side MOSFET turns on, the SW node sees the input voltage. When the low-side MOSFET turns on, the SW node detects the device return, which is the output voltage. During start-up, V_{IN} rises to achieve the desired input voltage. V_{OUT} starts ramping down after the EN pin voltage exceeds its threshold level and V_{IN} exceeds its UVLO threshold. As V_{OUT} continues to ramp down, the SW node low level follows it down. Figure 5 shows the resulting normal and smooth start-up of the output voltage.

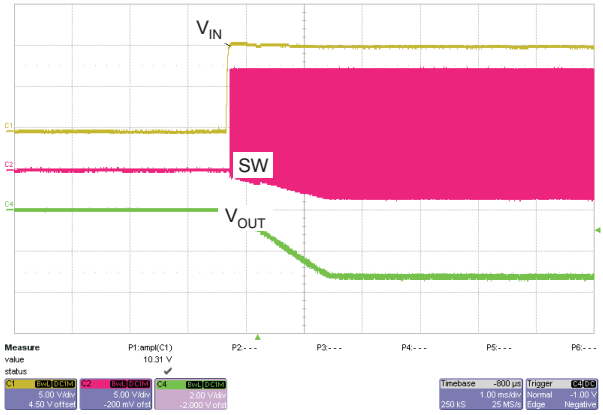


Figure 5. SW Node Voltage During Start-Up

3 External Components

The LMZM33606 power module integrates power MOSFETs and shielded inductor. As a result, this application only requires as few as four external components. Performing a load-transient test and frequency sweep is recommended to evaluate stability.

3.1 Capacitor Selection

Ceramic capacitors with low equivalent series resistance (ESR) are recommended to achieve low output voltage ripple. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. The higher the DC voltage applied to the capacitor, the less the effective capacitance. Use a minimum of 10-µF capacitance for both C_{BYP} and C_{IN}. Making this capacitor value too large can prevent proper start-up operations. Evaluating the Bode plot of the circuit under normal operation can provide insight on the stability of the system.

3.2 System Loop Stability

Stability is an important factor in the system when adding more output capacitance. The general rule of thumb for a stable design is a desired phase margin(PM) of at least 45° or greater. In extreme conditions too much output capacitance added to the system may result in a lowered bandwidth and slower transient response. The table below shows the PM for each output voltage selection measured from the modified default LMZM33606EVM with C_{FF} unpopulated and 388µF of ceramic-only C_{OUT}.

Table 3. Phase Margin of IBB LMZM33606

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	F_{cross}(kHz)	PM (º)
24	-1.2	3	32	37
24	-1.8	3	26	41
24	-2.5	3	20	43
24	-3.3	3	16	38
24	-5	3	15	44

Modifying the output capacitance and feed-forward capacitor will affect the PM measurement. The table below shows the PM for each output voltage selection that achieves a PM greater than 45º with the output capacitance and feed-forward capacitor used during testing. The Cff capacitor is meant to help improve phase margin and bandwidth when placed in parallel with the top feedback resistor. Note that the output capacitance is only ceramic. Non-ceramic capacitors will have high ESR that can impact the stability of the system. When modifying the output capacitance to improve PM, it is recommended to run a frequency response analysis to ensure proper operation and system stability.

Table 4. Phase Margin of Optimized IBB LMZM33606

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	F_{cross}(kHz)	PM (º)	C_{OUT} (µF)	C_{FF} (pF)
24	–1.2	2.5	33	48	435	100
24	–1.8	3	23.5	50	435	100
24	–2.5	3	18.4	52	435	100
24	–3.3	3	15.3	48	435	100
24	–5	3	13.7	62	435	100

Additionally too much output capacitance can falsely trigger hiccup mode in the LMZM33606. After start-up, hiccup mode is a feature in the LMZM33606 that protects the device against output short circuit conditions. In this mode the high-side and low-side MOSFETs power off and wait for a fixed hiccup time interval before restarting the device operation. Larger output capacitance results in longer charge time of the capacitors to the desired output voltage. The device can see this as a false short circuit condition and trigger hiccup mode.

4 Typical Performance

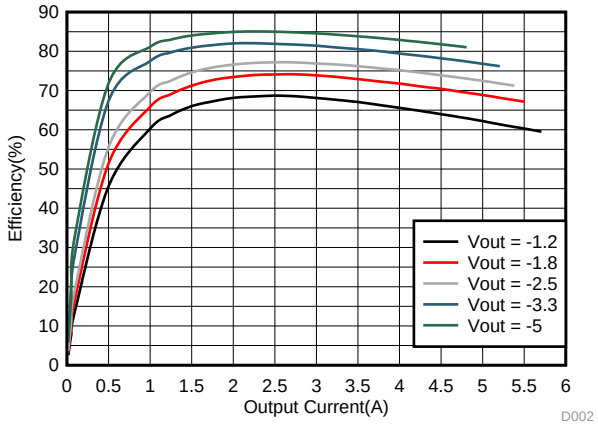


Figure 6. Efficiency at V_{IN} = 24 V

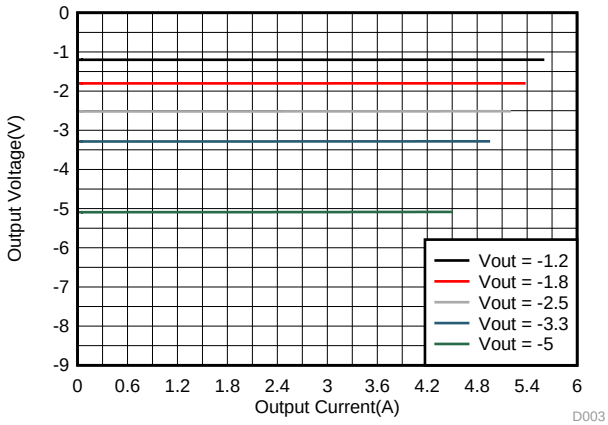


Figure 7. Load Regulation at V_{IN} = 24 V

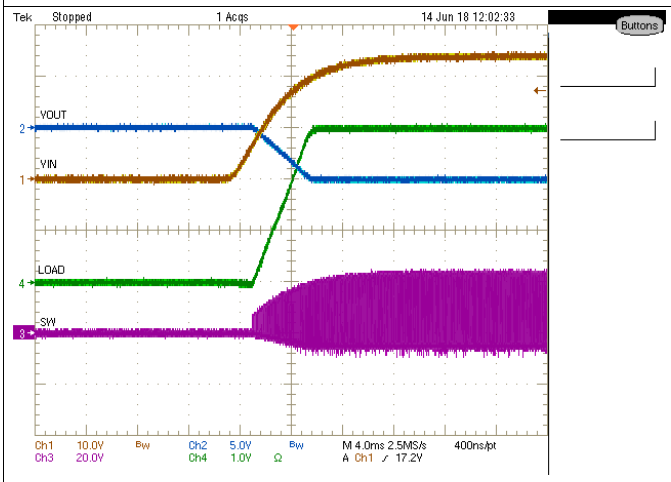


Figure 8. Start-up on V_{IN} = 24 V, V_{OUT} = –5 V With 3-A Load

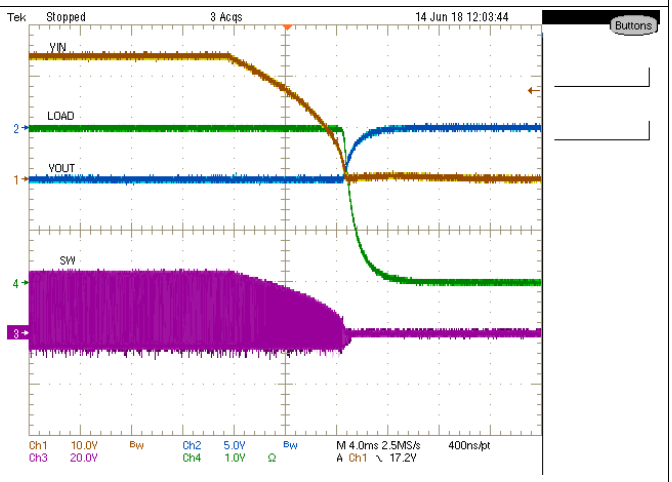


Figure 9. Shutdown on V_{IN} = 24 V, V_{OUT} = –5 V With 3-A Load

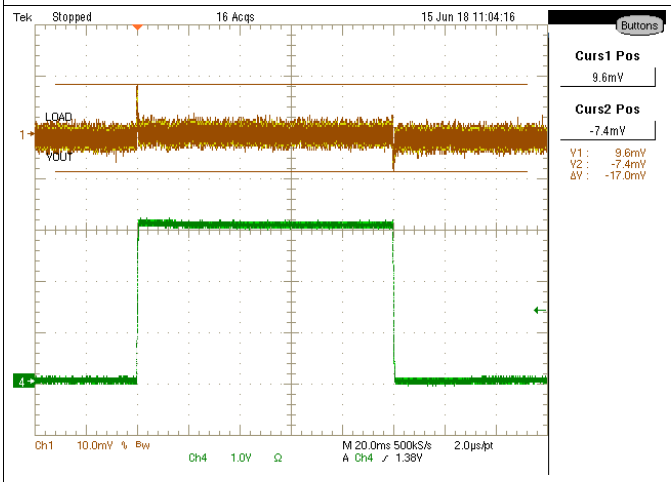


Figure 10. Load Transient Response, V_{IN} = 24 V, V_{OUT} = –5 V With 0-A to 3-A Load Step

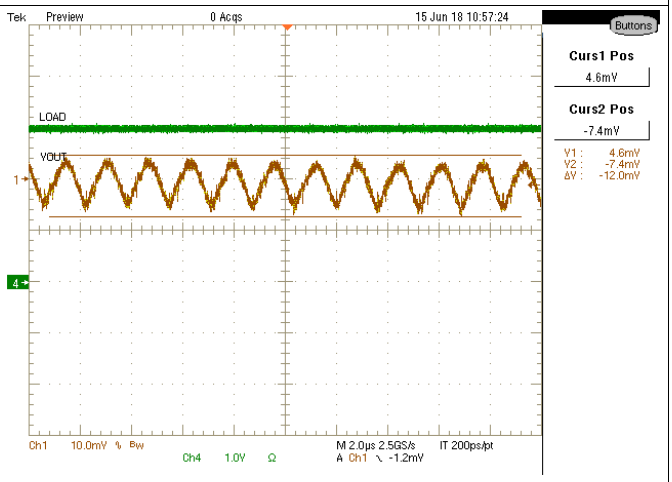


Figure 11. Output Voltage Ripple, V_{IN} = 24 V, V_{OUT} = –5 V With 3-A Load

5 Digital Pin Configurations

5.1 Digital Input Pin (EN)

Because the EN pin is referenced to V_{OUT} instead of 0 V, the EN voltage that turns the module on is affected. In a buck configuration, the specified typical threshold voltage for the EN pin with respect to IC return to be considered high is 1.2 V and 1.04 V is considered low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 1.2 V + V_{OUT}, and the low threshold is 1.04 V + V_{OUT}. For example, if V_{OUT} = –12 V, V_{EN} is considered a high for voltages above –10.8 V and a low for voltages below –10.96 V when V_{OUT} is up and running.

This behavior can cause difficulties enabling or disabling the part, because in some applications the IC providing the EN signal may not be able to produce negative voltages. The level shifter alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.

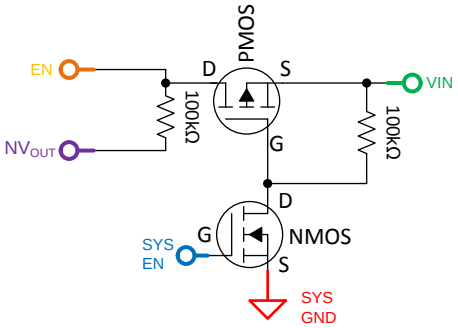


Figure 12. EN Pin Level Shifter

The positive signal (SYS_EN) that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 detects 0 V across its V_{GS} and also remains off. In this state, the EN pin detects V_{OUT}, which is below the low level threshold and disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (minimum V_{GS} as specified in the data sheet of the MOSFET), the gate of Q2 is pulled low through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. As a consequence, V_{IN} ties to EN through Q2, and the pin is above the high level threshold, causing the device to turn on. Ensure that the V_{GD} of Q2 remains within the ratings of the MOSFET ratings during both enabled and disabled states. Also ensure that V_{GS} and V_{DS} ratings are not exceeded. Failing to adhere to these constraint can result in damaged MOSFETs.

The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the output of the circuit and goes from VIN to –VOUT properly enabling and disabling the device.

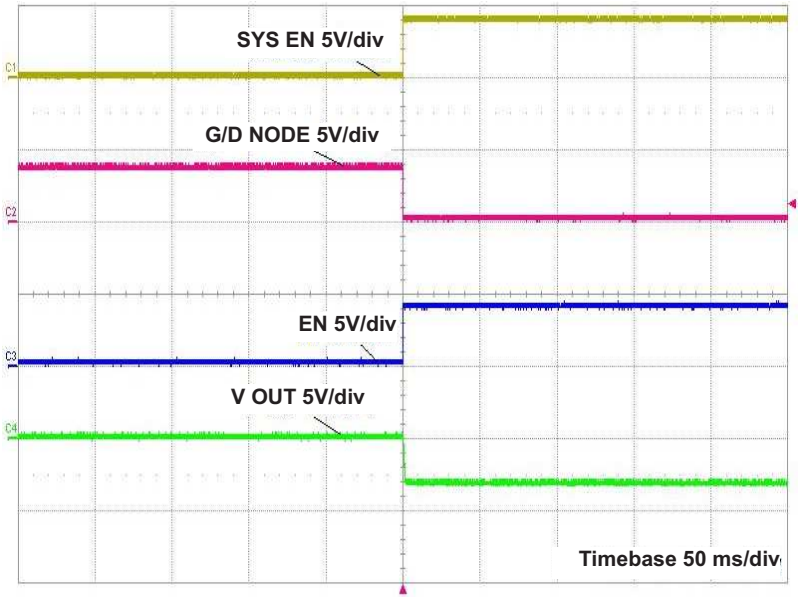


Figure 13. EN Pin Level Shifter on Start-Up

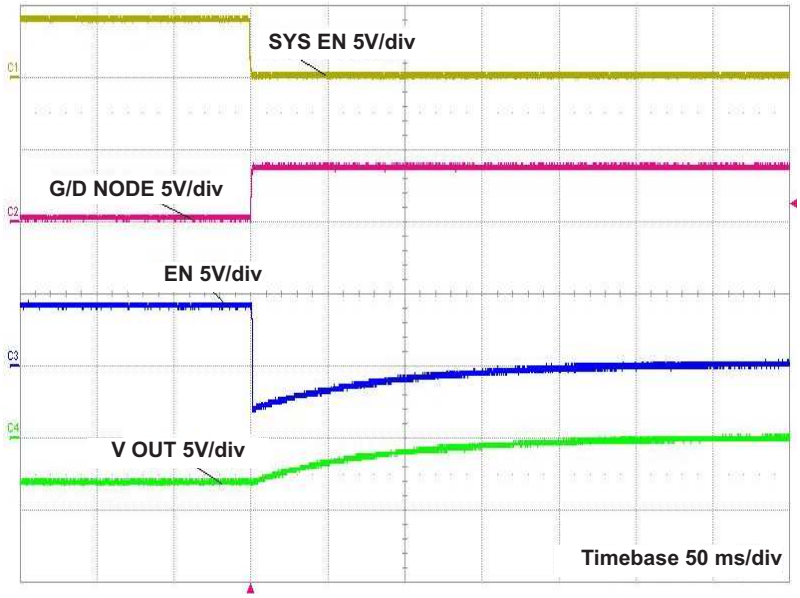


Figure 14. EN Pin Level Shifter on Shutdown

5.2 Power-Good Pin

The LMZM33606 has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC return in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the device pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin must not be driven more than 12 V above the negative output voltage (IC return).

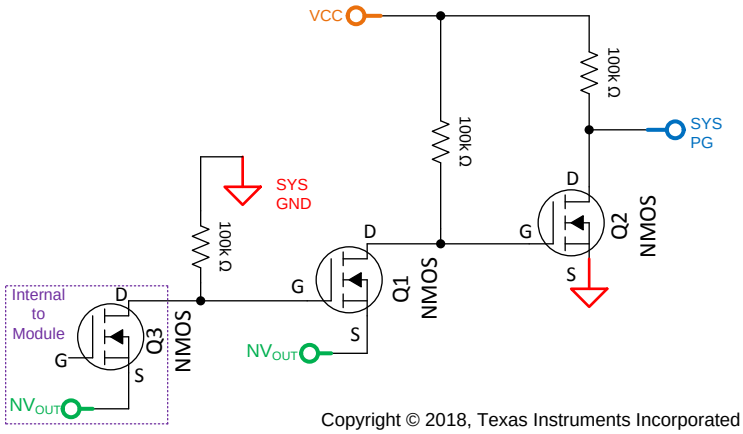
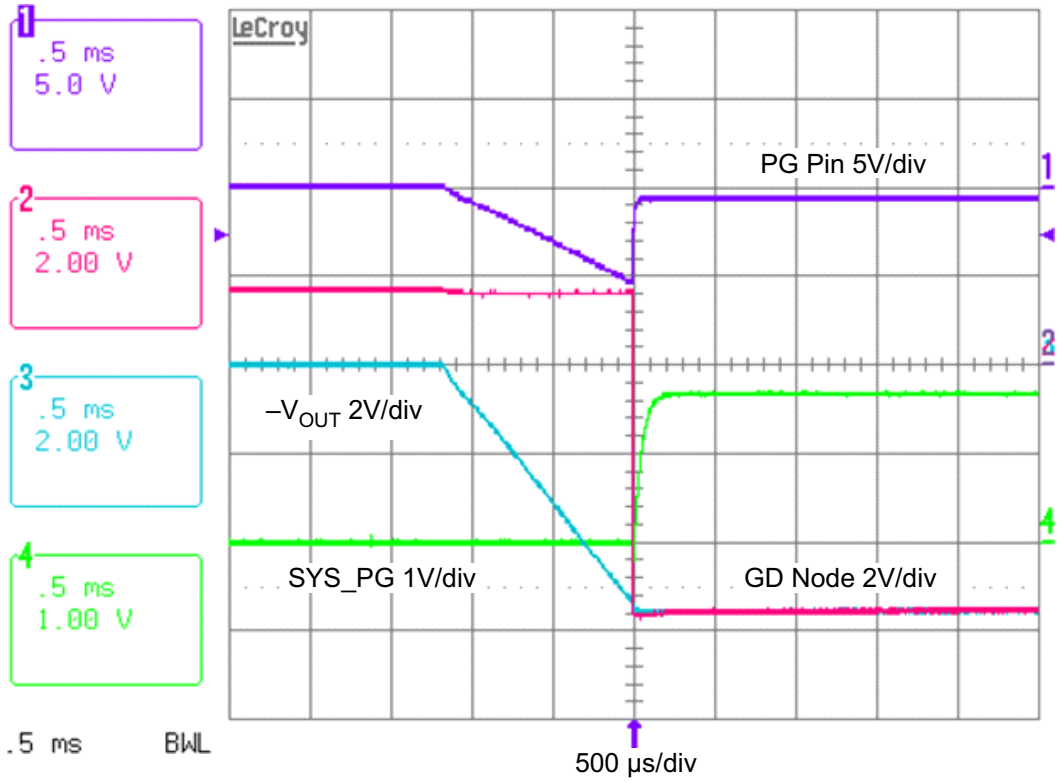


Figure 15. PG Pin Level Shifter

Inside these devices, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} detects V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 16 and Figure 17. The PG signal activates the PG pin level shifter circuit, and the GD Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V and FemtoFET CSD15830F3. The SYS_PG net is the output of the circuit that transitions between ground and 1.8 V and is easily read by a separate device.



Note that the PG pin is with respect to system return.

Figure 16. PG Pin Level Shifter on Start-Up

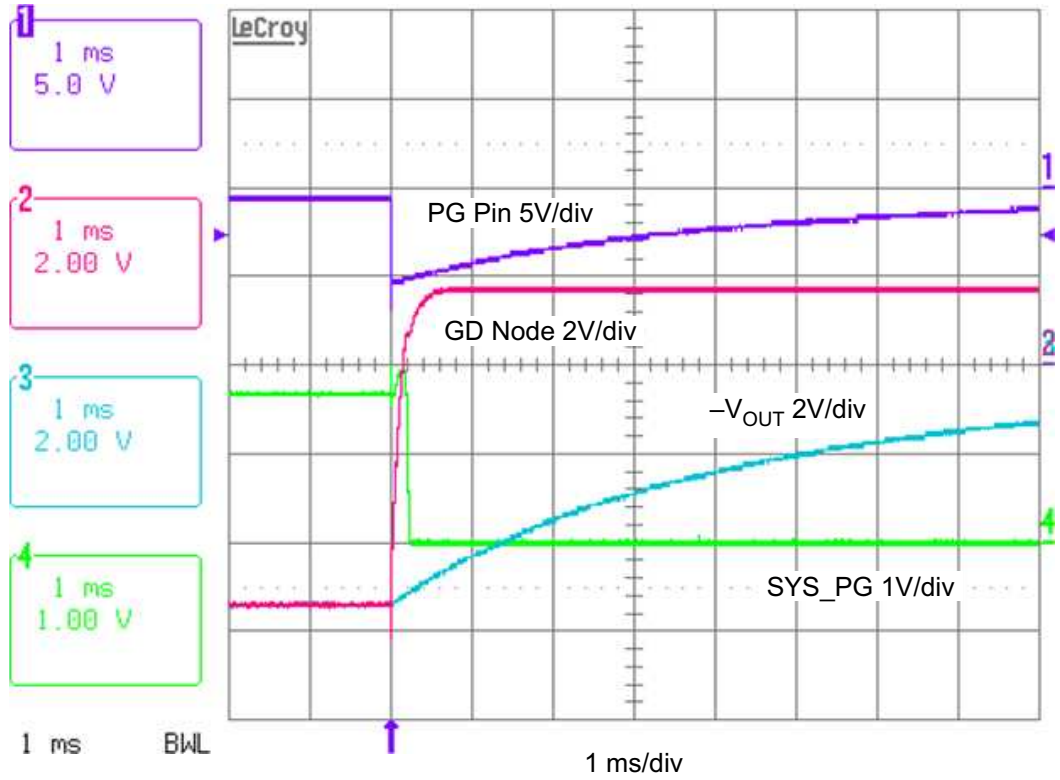


Figure 17. PG Pin Level Shifter on Shutdown

6 Conclusion

The LMZM33606 step-down power module can be configured in an IBB topology to generate a negative output voltage by switching the output and ground connection. The input voltage range is lowered because the device now has a reference point set to the negative output voltage rather than ground. Additionally, the inductor peak current is much higher effectively lowering the recommended maximum output current operating range. Converting an original buck topology into an IBB topology results in a lowered input voltage range and maximum output current. Additional level-shifting circuitry is required to invert the negative output signal if EN and PG pin usage is required.

7 References

The following documents are available for download from the TI web site:

1. D. G. Daniels, *Create an Inverting Power Supply From a Step-Down Regulator*.
2. J. Tucker, *Using a buck converter in an inverting buck-boost topology* .
3. J. Tucker, *Using the TPS5430 as an Inverting Buck-Boost Converter*.
4. T. Allag, C. Glaser, *Using the TPS6215x in an Inverting Buck-Boost Topology*.
5. Guibord, Matt, *Feedforward Capacitor to Improve Stability and Bandwidth With the TPS621-Family and TPS821-Family*.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (October 2018) to B Revision	Page
• Changed to "slower transient response" from "PM less than 45 deg"	6
• Changed the PM column in table 4.	6

Changes from Original (July 2018) to A Revision	Page
• Updated duty cycle equation	2
• Updated duty cycle calculation	2
• Updated Table 1	3
• Updated Table 2	3

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