Interfacing the TLC320AD57 Sigma-Delta Stereo ADC (in Master Mode) with the TMS320C5X DSP

APPLICATION REPORT: SPRA090

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Abstract

Most audio systems use either an analog-to-digital converter (ADC) or digital-to-analog converter (DAC) to interface with a digital signal processor (DSP). This application note describes how to interface the Texas Instruments (TI™) TLC320AD57 (’AD57) audio band sigma-delta stereo ADC with the TI TMS320C5x (’C5x) DSP via the serial port. The hardware interface solution is provided because the sigma-delta stereo ADC is hardware controlled.

Product Support

Related Documentation

The following list specifies product names, part numbers, and literature numbers of corresponding TI documentation.

- *TLC320AD57C Sigma-Delta Stereo Analog-to-Digital Converter Data Manual*, Literature number SLAS086A
- *TMS320C5x User's Guide*, Literature number SPRU056C

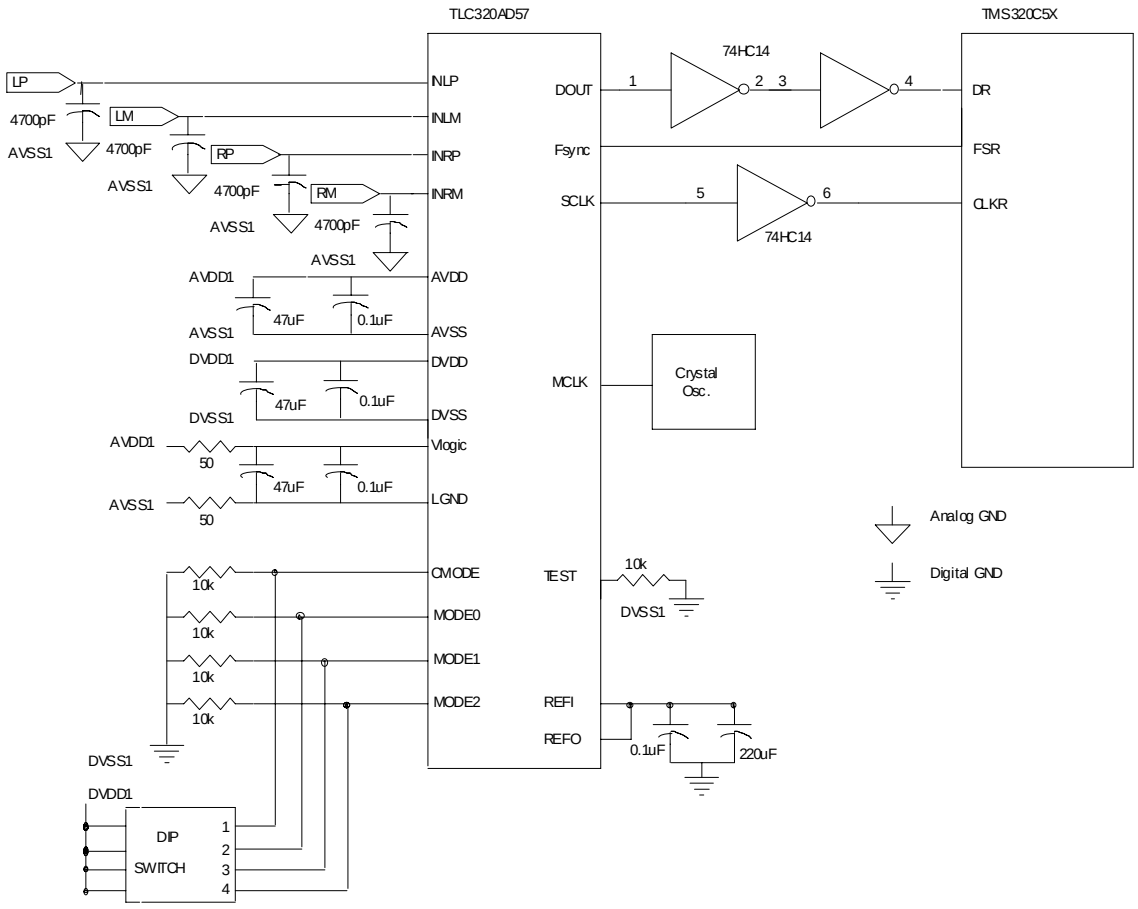
World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Hardware Solution

Figure 1 shows the hardware connection between the ’C5x DSP and the ’AD57 ADC in the master mode. (For details on master mode operation, see the TI *TLC320AD57C Sigma-Delta Stereo Analog-to-Digital Converter Data Manual*).

Figure 1. TMS320C5x and TLC320AD57 (in Master Mode) Hardware Connection



TLC320AD57 Operating Conditions

As a master, the TLC320AD57 generates the following signals to provide operational information to the DSP:

- LRClk (left/right clock) indicates whether serial data out is from the left or right channel of the ADC.
- Fsync (Frame synchronization pulse) designates valid data out from the ADC.
- SCLK (shift clock) clocks serial data out of the ADC.

These clocks are generated through an external crystal oscillator (frequencies range from 18.432 MHz to 256 kHz) connected to the MCLK input of the ADC. The relationship between MCLK, SCLK, and LRClk is shown in Table 1.

Table 1. Relationship of Master Clock to Shift Clock and Sampling Rate (Modes 6 and 7)

MCLK (MHz)	CMODE	SCLK (MHz)	LRClk (kHz)
12.2880	Low	1.536	48
18.4320	High	1.536	48
11.2896	Low	1.412	44.1
16.9344	High	1.412	44.1
8.1920	Low	1.024	32
12.2880	High	1.024	32
0.2560	Low	0.032	1
0.3840	High	0.032	1

Although the ADC can have either 16-bit or 18-bit resolution, this application report discusses only the 16-bit DSP Continuous Modes, mode 6 (110) and mode 7 (111). This is because the maximum word length for data transfer via the serial port receiver of the ’C5x DSP is 16 bits.

In addition, the relationship of SCLK to LRClk is 32X in modes 6 and 7. Fsync pulse, on its falling edge, initiates the first data bit out of the ADC.

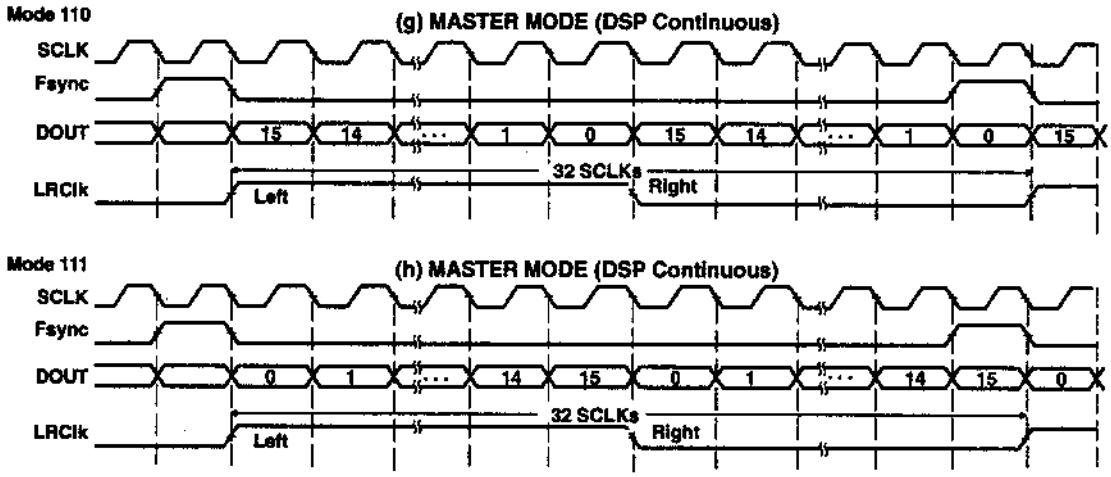
The sampling frequency or LRClk is related to MCLK based on the CMODE value as follows:

- LRClk = MCLK/256 (for CMODE low)
- LRClk = MCLK/384 (for CMODE high)

During the high period of LRClk, the 16-bit left channel data is shifted out. The 16-bit right channel is shifted out during the low period of LRClk.

For mode 6, the MSB (most significant bit) is shifted out first. For mode 7, the LSB (least significant bit) is shifted out first (see Figure 2). See the TI *TLC320AD57 Data Manual* timing diagrams (Figures 2-3(d) and 2-3(e).

Figure 2. TLC320AD57 Timing Diagram (Master Mode 110 and 111)

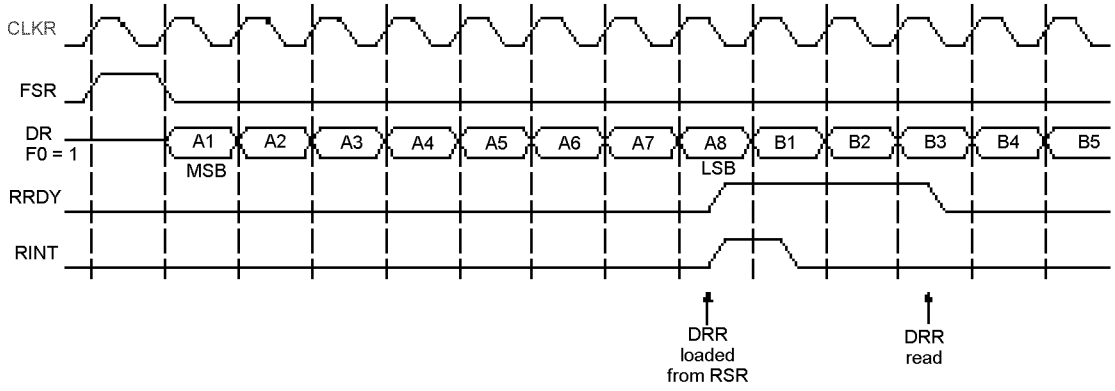


TMS320C5x Operating Conditions

The ’C5x DSP requires the F0 bit of the Serial Port Control (SPC) register to be set to 0 for 16-bit transfer. The FSM bit also must be set to 0 for continuous mode receives. No more sync pulse is needed after the initial frame sync pulse from the ADC. The DSP Receive Shift Register (RSR) receives data via its serial input DR.

For continuous mode, the Receive Interrupt (RINT) occurs after every 16-bit word received when RSR data is loaded to the Data Receive Register (DRR). Thus, the DSP firmware has to poll this interrupt to identify the appropriate data (whether serial data is from the left or right channel). See Figure 3 (taken from the TI *TMS320C5x DSP User’s Guide*).

Figure 3. TMS320C5x Timing Diagram (Continuous Receive Mode)



Summary

This application report explained how to connect the TI TLC320AD57 audio band sigma-delta stereo ADC to the TI TMS320C5x DSP for audio end-equipment application. You are advised to create your own DSP firmware to manipulate the ADC's left/right channel serial data based on the recommendations provided in this document.