Migrating from TMS320VC5402A to TMS320VC5502

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5402A to the TMS320VC5502. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the following data manuals and reference guides: *TMS320VC5402A Fixed-Point Digital Signal Processor Data Manual* (SPRS015), the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166), the *TMS320C54x DSP Reference Set, Volume1* (SPRU131), the *TMS320C54x DSP Reference Set, Volume 5* (SPRU302), the *TMS320C55x DSP CPU Reference Guide* (SPRU371), and the *TMS320C55x DSP Peripherals Reference Guide* (SPRU317).

Migration issues from the TMS320VC5402A to TMS320VC5502 are indicated with the following symbols:

[S] means software modification is required.

[H] means hardware modification is required.

[D] means the VC5402A and VC5502 are different but no modification is necessary for migration (i.e., different but compatible).

[N] means the VC5502 adds new features that are not available on the VC5402A

These symbols are included at the beginning of each section.

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1 Pin and Package Compatibility [H]

Table 1. Pin and Package Differences

Device	Package Type(s)	Pin Count
VC5402A	Microstar Ball Grid Array (GGU)	144
	Low Profile Quad Flatpack (PGE)	144
VC5502	Ball Grid Array (GZZ)	176
	Low Profile Quad Flatpack (PGF)	176

2 Power Supply [H]

Table 2. Power Supply Differences

	Core Supply Voltage (CV_{DD})			I/O Supply Voltage (DV_{DD})			PLL Supply Voltage (PV_{DD})		
Device	**MIN**	***NOM***	**MAX**	**MIN**	***NOM***	**MAX**	**MIN**	***NOM***	**MAX**
VC5402A	1.55V	1.6V	1.65V	2.7V	3.3V	3.6V	N/A	N/A	N/A
VC5502	1.20V	1.26V	1.32V	3.0V	3.3V	3.6V	3.0V	3.3V	3.6V

The VC5502 contains an additional supply voltage, PV_{DD}, dedicated for the PLL module only. On the VC5402A, the PLL runs on the core supply voltage (CV_{DD}).

NOTE: TI DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to insure that neither supply is powered-up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long-term reliability of the device. Please refer to TI application report SLVA073 for more information.

3 Phase-Locked Loop (PLL) and Clock Mode Settings at Reset

Table 3. PLL Differences

Device	PLL Type	On-Chip Oscillator	Clock Input Source
VC5402A	Analog PLL	Yes	External clock input, or On-chip oscillator with external crystal†
VC5502	Analog PLL	Yes	External clock input, or On-chip oscillator with external crystal

† On-chip oscillator functionality is only supported in silicon revision A. Please refer to SPRZ018 for more details.

The reference clock input of the VC5402A may be sourced from either a crystal resonator circuit or an external clock.

- The crystal resonator circuit is connected across the X1 and X2/CLKIN pins of the VC5402A to enable the internal oscillator.
- The external clock source is directly connected to the X2/CLKIN pin, and X1 is left unconnected.

The VC5402A clock generator circuitry takes the reference clock input and then either divides it by two or four (DIV mode) to generate clocks for the device. Alternatively, the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor (1 of 31 possible ratios), allowing use of a clock source with a lower frequency than that of the CPU. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The VC5402A CLKMD register is used to define the clock configuration of the PLL clock module. Upon reset, the CLKMD register is initialized with a predetermined value dependent only upon the state of the CLKMD1 – CLKMD3 pins. For more programming information, see the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (SPRU131).

The clock input of VC5502 may be sourced either from an externally generated 3.3-V clock input on the X2/CLKIN pin, or from the on-chip oscillator (OSCIN) if an external crystal circuit is attached to the device. The oscillator supports fundamental mode crystals up to 25 MHz. Please refer to the VC5502 data manual (SPRS166) for more details. The VC5502 does not support the clock mode select (CLKMD) input pin. At reset, pin GPIO4 sets the state of the CLKMD0 bit of the CLKMD register, which in turn determines the clock source for the DSP. The CLKMD0 bit selects either the internal oscillator output (OSCOUT) or the X2/CLKIN pin as the input clock source for the DSP. If GPIO4 is low at reset, the CLKMD0 bit will is set to ‘0’ and the internal oscillator and the external crystal generate the input clock to the DSP. If GPIO4 is high, the CLKMD0 bit will be set to ‘1’ and the input clock will be taken directly from the X2/CLKIN pin. Please note that after reset, the GPIO4 pin may become active depending on the boot mode selected through the GPIO[2:0] pins.

When the VC5502 is not in bypass mode (PLL mode-enabled) the frequency of the input clock can be divided-down by a programmable divider (D0) by any factor from 1 to 32. The output clock of the divider can be multiplied by any factor from 2 to 15 through a programmable multiplier (M1). Following reset, the clock generator is placed in bypass mode.

4 Memory

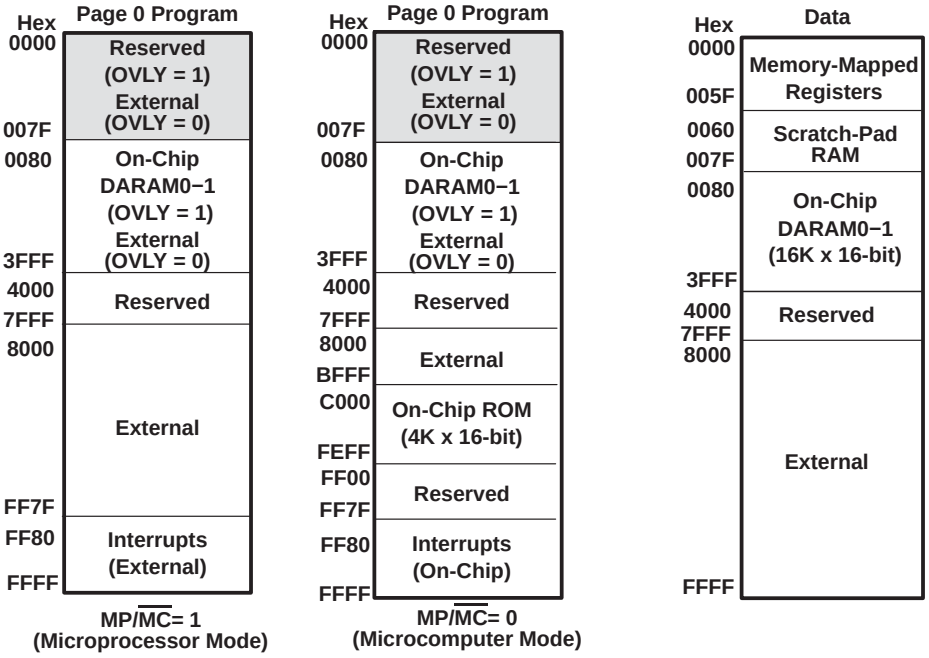
There are many differences in the memory architecture and organization between C54xx and C55xx devices. Table 4 shows a comparison of memory features on both devices. Refer to the device data sheets and migration document, SPRU429, for a complete description.

Table 4. Memory Differences

	Device	
Memory Type	**VC5402A**	**VC5502**
Total on-chip memory	32K words	56K words
Single-access random access memory (SARAM)	None	None
Dual-access random access memory (DARAM)	16K words	32K words
Read-only memory (ROM)	16K words	16K words
Instruction cache (I-Cache)	None	8K words (16K bytes)
Maximum addressable external memory	8M words	8M words

4.1 Memory Map

C55xx devices have a unified memory map – which means that code and data can be placed anywhere in memory. A unified memory architecture allows code and data to share the same address space so program and data accesses are made to the same physical space. This is in contrast to the C54xx devices which offer a modified Harvard architecture with separate code and data memory spaces. Figure 1, Figure 2, and Figure 3 show the memory maps for both devices.



NOTE: Address ranges for on−chip DARAM in data memory are: DARAM0: 0080h–1FFFh; DARAM1: 2000h–3FFFh

Figure 1. VC5402A Program and Data Memory Map

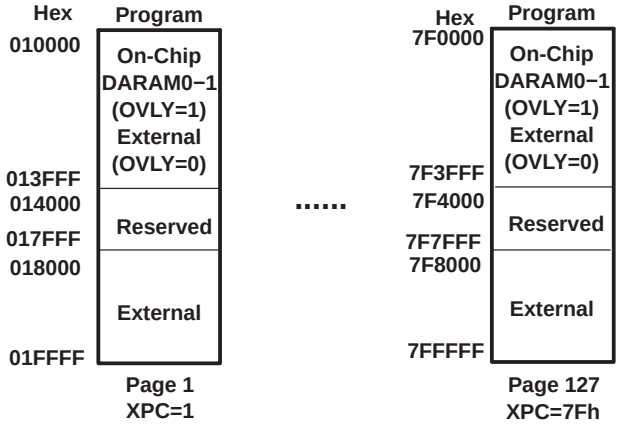


Figure 2. VC5402A Extended Program Memory Map

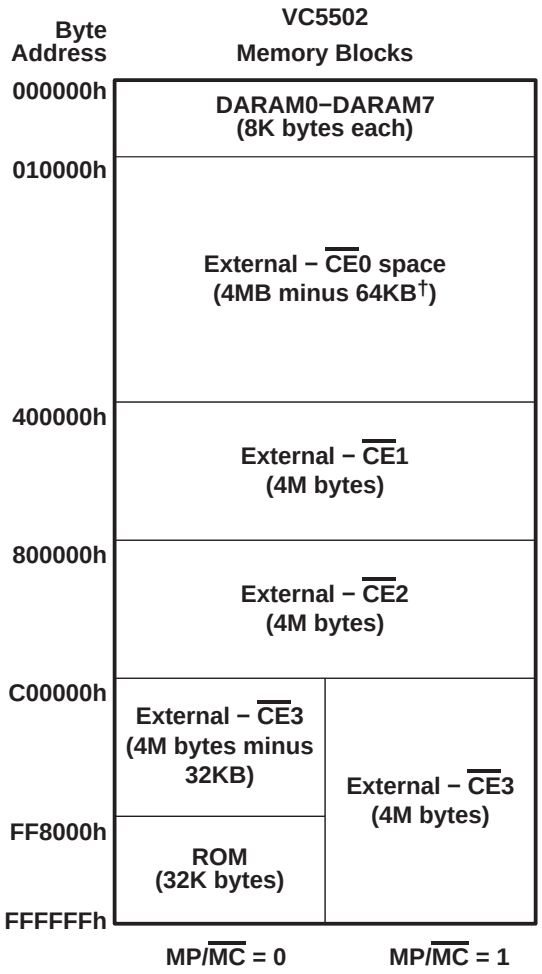


Figure 3. VC5502 Memory Map

As shown in Figure 2, the VC5402A uses a paged extended memory scheme in program space to allow access of up to 8192K of program memory. Because of the unified memory map architecture, such a scheme does not exist on the VC5502.

C55xx code and data are treated slightly differently regarding memory addresses. To be compatible with the C54xx family, C55xx data addresses always point to 16-bit boundaries. To decrease code size, C55xx program addresses are byte-accessible versus being word-addressable (16 bits) on the C54xx devices.

4.1.1 Coding Tips

Some tips for coding C55xx device instructions are provided here:

- Since C55xx addresses in program space are given in bytes, instructions that use hard-coded addresses/offsets (for example, #1000h) will not address the correct values, and therefore, are flagged as MASM55 errors. It is good programming practice to avoid using hard-coded addresses or offsets. If you are migrating your assembly code from the VC5402A to the VC5502 device, and hard-coded values have been used, replace them with labels so that the linker will resolve them at link time.

- Because C55x code is byte addressed, the interrupt vector table should be aligned on a 256-byte page (the 8 LSBs of the base address should be 0s).
- C54xx devices use 16-bit word addresses and lengths in the linker command file. A C55x linker command file uses byte addresses and byte lengths for both program and data sections. However, C55x map file lists program addresses in bytes and data addresses in 16-bit words.

4.2 On-Chip ROM

The standard on-chip ROM contains a bootloader which provides a variety of methods to load application code automatically after power-up or a hardware reset.

The VC5402A has an on-chip memory security feature supporting a maskable option to protect the contents of on-chip memories. When the ROM protect bit is set, no externally originating instruction can access the on-chip memory spaces; host port interface (HPI) accesses have no write restrictions, however, read accesses are restricted to the 4000h−5FFFh address range. Code execution begins at location FF80h of the on-chip ROM (if the MP/MC pin is sampled low during a hardware reset). This location contains a branch instruction to the start of the bootloader program. The standard VC5402A devices provide different ways to download the code to accommodate various system requirements, please refer to the bootloader section for more details. Refer to Table 5 for the VC5402A ROM layout.

Table 5. VC5402A Standard On-Chip ROM Layout

Address Range	Description
C000h−D4FFh	ROM tables for the GSM EFR speech codec
D500h−F7FFh	Reserved
F800h−FBFFh	Bootloader
FC00h−FCFFh	μ-Law expansion table
FD00h−FDFFh	A-Law expansion table
FE00h−FEFFh	Sine look-up table
FF00h−FF7Fh	Reserved†
FF80h−FFFFh	Interrupt vector table

† 128 words are reserved for factory device-testing purposes. Application code to be implemented in on-chip ROM must reserve these 128 words at addresses FF00h−FF7Fh in program space.

The VC5502 incorporates 16K x16-bit of on-chip, one-wait-state maskable ROM that can be mapped into program memory space. The on-chip ROM is located at the byte address range FF8000h–FFFFFFh when MP/MC = 0 at reset. The VC5502 does not have a hardware MP/MC pin. MP/MC in this case refers to a bit located in the ST3 status register, and its status is determined by the logic level on the BOOTM[2:0] pins at reset. These pins are not sampled again until the next hardware reset. The software reset instruction does not affect the MPNMC bit, however, software can be used to set or clear the MPNMC bit.

The VC5502 on-chip ROM is a two-cycle-per-word memory access, except for the first word access, which requires four cycles. The branch instruction to the start of the bootloader program is contained at FF8000h in ROM.

The standard on-chip ROM layout for the VC5502 is shown in Table 6. The bootmode branch table contains hard-coded jumps to the beginning of each boot mode code section in the bootloader. The sine look-up table contains 256 values (crossing 360 degrees) expressed in Q15 format.

Table 6. VC5502 On-Chip ROM Layout

Starting Byte Address	Contents
FF_8000h	Bootloader Program
FF_ECAEh	Bootloader Revision Number
FF_ECB0h	Boot Mode Branch Table
FF_ED00h	Sine Table
FF_EF00h	Reserved
FF_FF00h	Interrupt Vector Table

The VC5502 provides several options to download the code to accommodate varying system requirements. Refer to the *Bootloader* section of this document for details.

4.3 Instruction Cache (I-Cache)

The I-cache on the VC5502 consists of a single 2-way cache block. The 2-way cache uses 2-way associative mapping and holds up to 16K bytes: 512 sets, two lines per set, four 32-bit words per line. The cache supports the following features listed below.

- Line flush. A line flush will invalidate the line valid (LV) bit for a specific line in cache.
- Miss Counter Register (ICWMC) function. The ICWMC register is incremented by 1 for every miss in the 2-way cache.
- Freeze/lock feature: Writing ‘1’ to the cache freeze (CAFRZ) bit of ST3_55 causes the contents of the I-cache to be locked. Instruction words that were cached prior to the freeze are still accessible in the case of an I-cache hit, but the data arrays will not be updated in response to an I-cache miss. To re-enable updates, write ‘0’ to CAFRZ. A DSP reset forces CAFRZ = 0 (I-cache not frozen). Cache lock (or freeze) applies to the entire cache only. Freeze of select portions of the cache is not supported.

Control bits in the CPU status register, ST3_55, provide the ability to enable, freeze, and flush the cache. See section 2.3 of the *TMS320VC5501/5502 DSP Instruction Cache Reference Guide* (SPRU630), for more details.

The VC5402A device does not have an instruction cache.

4.4 Enhanced External Parallel Interface (XIO2) and External Memory Interface (EMIF)

The VC5402A device interfaces to external memory via the so-called XIO2 interface. Most external accesses require three cycles composed of a leading cycle, an active (read or write) cycle, and a trailing cycle. The leading and trailing cycles provide additional immunity against bus contention when switching between read operations and write operations. To maintain high-speed read access, a consecutive read mode that performs single-cycle reads as on previous 54x devices is available.

The VC5502 device accesses external memory via the EMIF interface. The EMIF provides General-Purpose Input/Output (GPIO) capabilities and glueless interface to SARAM, asynchronous EPROM, SDRAM, and SBRAM. The VC5502 EMIF has a specified maximum clock frequency of 100 MHz when interfacing to synchronous memory. The EMIF clock can be derived internally from the CPU clock or from an external clock source through the ECLKIN pin if a specific EMIF frequency is needed. The source for the EMIF clock is selected by the EMIFCLKS pin.

NOTE: When driven from an external clock source, additional internal synchronization logic is used. This results in EMIF data throughput performance degradation.

For more information about the VC5502 EMIF, please refer to the *TMS320VC5501/5502 DSP External Memory Interface (EMIF) Reference Guide* (SPRU621).

Table 7 outlines the main differences between the way each device interfaces to external memory .

Table 7. VC5402A, VC5502 External Memory Access Comparison

	Device	
Interface to External Memory	**VC5402A**	**VC5502**
Interface name	Enhanced External Parallel Interface (XIO2)	External Memory Interface (EMIF)
Type of memory possible	Asynchronous only	Asynchronous and wynchronous
Max interface speed	Depends on CPU clock rate and access type†	100MHz
Interface width	16 bits	8, 16, 32 bits
Interface clock source	Internal (CLKOUT)	Internal (SYSCLK3) or external (ECLKIN)‡

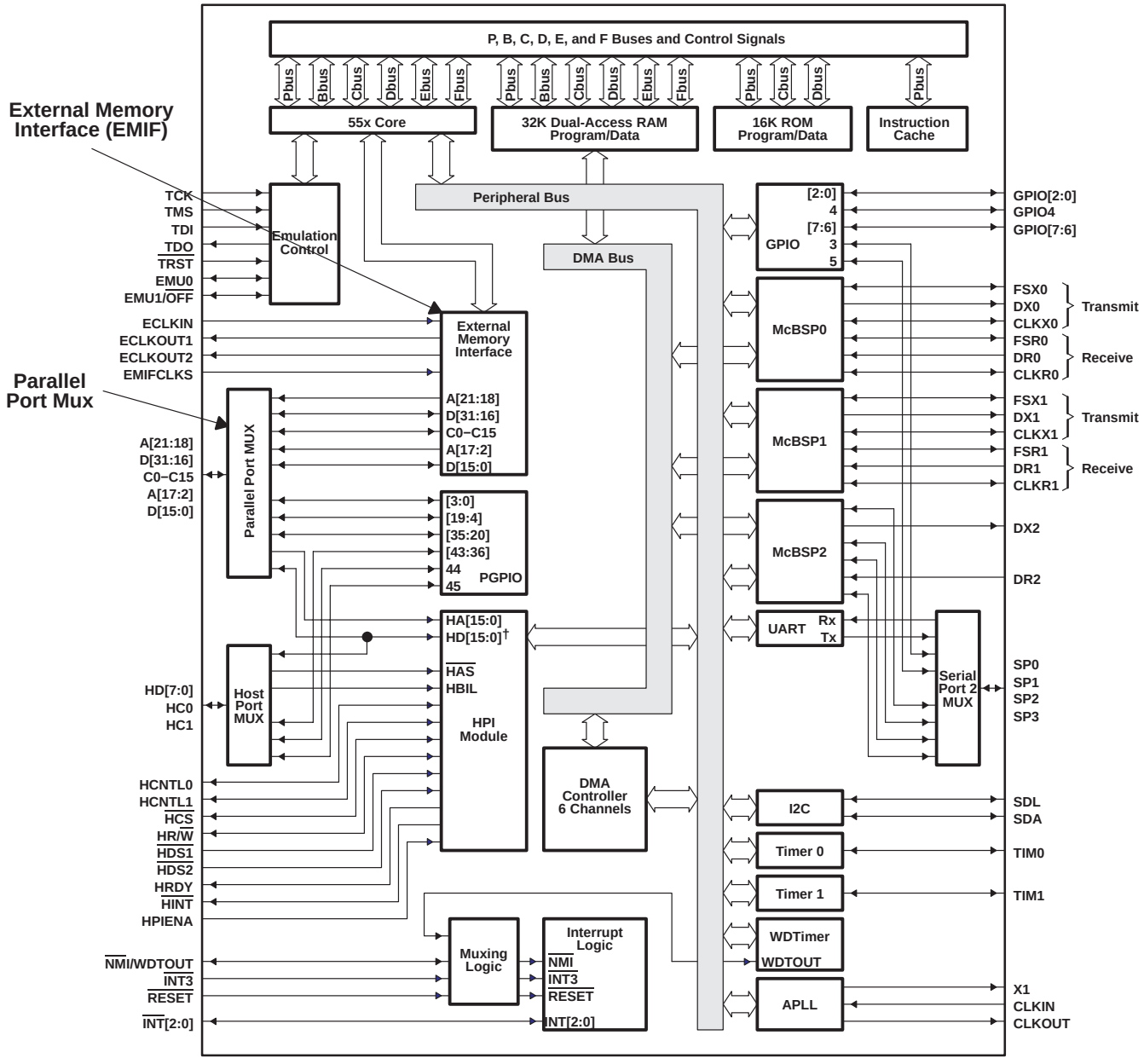
† Most external accesses require 3 cycles. However, a consecutive read mode that performs single-cycle reads is available. A cycle refers to one CLKOUT cycle. CLKOUT represents the CPU rate divided by 1, 2, 3, or 4 as configured in the bank-switching control register (BSCR).

‡ The EMIF may be clocked from an external asynchronous clock source through the ECLKIN pin if a specific EMIF frequency is needed. Data throughput performance is degraded due to synchronization issues when an external clock source is used.

NOTE: When the EMIF clock source is external (ECLKIN), the EMIF internal clock speed, SYSCLK3, is limited to the fast peripheral clock (SYSCLK1) maximum speed which is 150MHz. The fast peripherals clock group includes the DMA, HPI, and the timers. Please refer to section 3.9.1.4 in the *TMS320VC5502 Fixed-Point Digital Signal Processor Data Manual* (SPRS166), for more information.

Access to external memory on the VC5502 is done through the 32-bit external memory Interface (EMIF). As shown in Figure 4, the majority of EMIF signals are routed to external memory via the parallel-port mux. Only Four EMIF I/O signals (ECLKIN, ECLKOUT1, ECLKOUT2, and EMIFCLKS) are directly connected to the EMIF peripheral.

The parallel port mux controls the function of 20 address signals (pins A[21:2]), 32 data signals (pins D[31:0]), and 16 control signals (pins C0 through C15). The parallel port mux supports two modes: full EMIF mode and non-multiplexed HPI mode. Please refer to the *Pin Muxing* section of this document for more details.



† HD[15:8] are not used when the HPI is operated in multiplexed mode.

Figure 4. VC5502 Functional Block Diagram

4.5 Host Port Interface (HPI) Memory Access

The VC5502 HPI provides a parallel port through which an external host processor (host) can access memory internal to the VC5502 DSPs. Specifically, the host can access the first 32K words of internal memory except for addresses 000000h–00005Fh, which are reserved for the memory mapped registers of the CPU. The host must provide 15-bit addresses to the HPI, where each address points to a word (a 16-bit value) in memory. The host does not have direct access to memory that is external to the DSP. The host can access the following HPI registers on the device: HPIC, HPIAW, HPIAR, and HPID. Note that if the DSP and HPI contend for access to the same internal DARAM block, the DSP is always given priority. Refer to *TMS320VC5501/5502 DSP Host Port Interface (HPI) Reference Guide* (SPRU620), Table 1, for more information.

On the VC5402A, the HPI allows host access to the entire on-chip memory range of the DSP. Host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one cycle.

5 Multichannel Buffered Serial Port (McBSP) [H/S]

The McBSP internal block diagram of the VC5402A and VC5502 is shown in Figure 5. As evident from the diagrams, the register set of the VC5502 McBSP adds the following registers: one SPCR register, one PCR register, one XCR register, one MCR register, one SRGR register, seven RCER registers, and seven XCER registers

The VC5402A McBSP adds two special synchronization events to the DMA: REVTA and XEVTA.

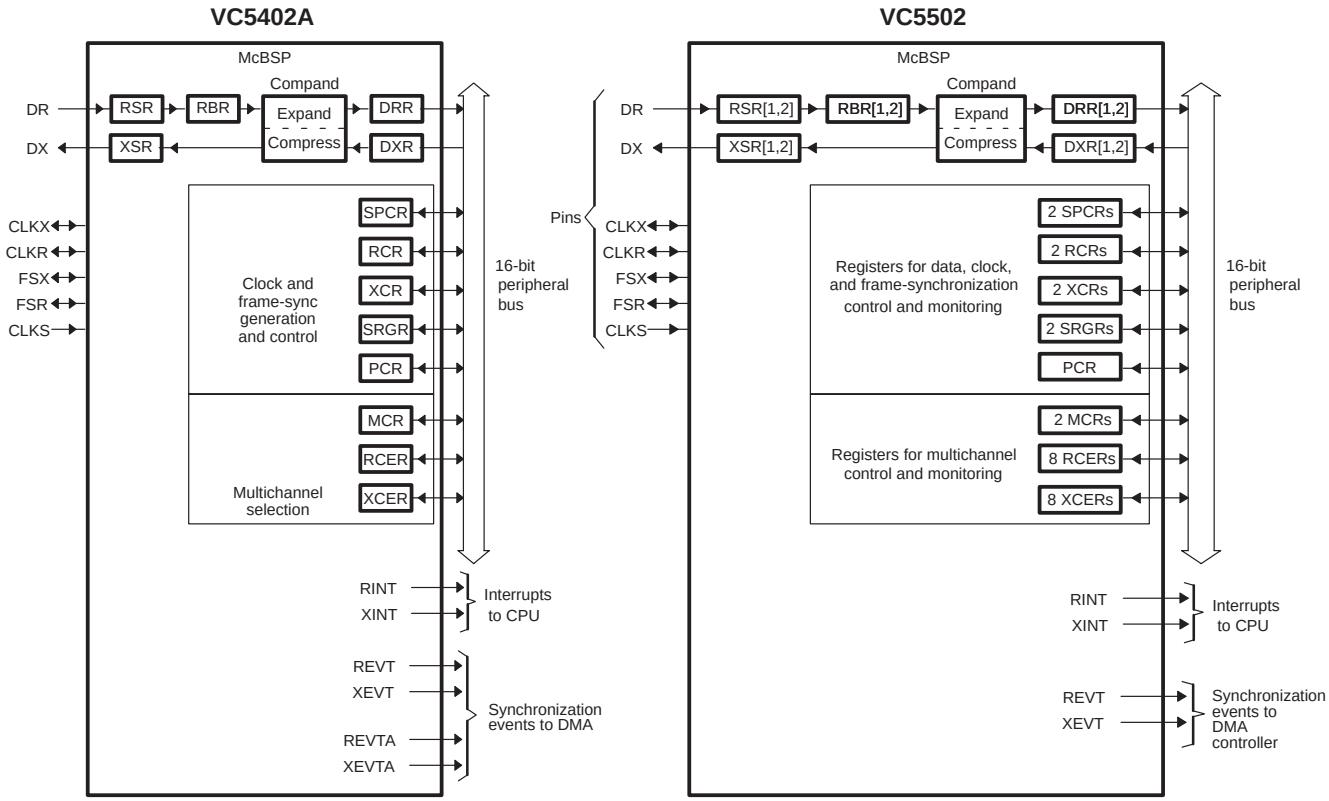


Figure 5. Conceptual Block Diagram of the McBSP

Major feature differences between the McBSPs on these devices include:

- VC5502 capability to use the McBSP pins as general-purpose I/O pins
- VC5502 inclusion of status bits for flagging exception/error conditions
- VC5402A control registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSA) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register.
- DMA synchronization events: refer to the DMA section of this document.
- Memory-mapped registers:
  - The VC5402A has 27 memory-mapped CPU registers, which are mapped in data memory space address 00h to 5Fh. Each VC5402A device also has a set of memory-mapped registers associated with peripherals. Each 5402A device also has a set of memory-mapped registers associated with peripherals. Unlike the C5502, all CPU and peripheral memory-mapped registers are part of the data memory (00h-5Fh)
  - The VC5502 has 78 memory-mapped CPU registers that are mapped in I/O memory space. Please note that all McBSP registers are I/O mapped, they are not part of the data memory as in the case of the VC5402A.

Table 8 and Table 9 show a comparison between the McBSP memory-mapped registers for McBSP Port#0 on both devices. The same differences also apply to the other McBSP ports.

Table 8. McBSP Port#0 Data Registers

	VC5402A		VC5502	
	(Data Memory Mapped Registers)		(I/O Mapped Registers†)	
McBSP Port#0 Data Register Description	Register Name	Word Address	Register Name	Word Address
Data Receive Register 1	DRR10	0021h	DRR1_0	2800h
Data Receive Register 2	DRR20	0020h	DRR2_0	2801h
Data Transmit Register 1	DXR10	0023h	DXR1_0	2802h
Data Transmit Register 2	DXR20	0022h	DXR2_0	2803h

† I/O mapped registers are accessible at addresses in I/O space

Table 9. McBSP Port#0 Control Registers

	VC5402A		VC5502	
	Data Memory Mapped Registers		I/O Mapped Registers†	
McBSP Port#0 Control Register Description	Register Name	Address: 0039h Sub-Address‡	Register Name	Word Address
Serial Port Control Register 1	SPCR10	00h	SPCR1_0	2804h
Serial Port Control Register 2	SPCR20	01h	SPCR2_0	2805h
Receive Control Register 1	RCR10	02h	RCR1_0	2806h
Receive Control Register 2	RCR20	03h	RCR2_0	2807h
Transmit Control Register 1	XCR10	04h	XCR1_0	2808h
Transmit Control Register 2	XCR20	05h	XCR2_0	2809h
Sample Rate Generator Register 1	SRGR10	06h	SRGR1_0	280Ah
Sample Rate Generator Register 1	SRGR20	07h	SRGR2_0	280Bh
Multichannel Control Register 1	MCR10	08h	MCR1_0	280Ch
Multichannel Control Register 2	MCR20	09h	MCR2_0	280Dh
Pin Control Register 0	PCR0	0Eh	PCR0	2812h
Receive Channel Enable Register Partition A	RCERA0	0Ah	RCERA_0	280Eh
Receive Channel Enable Register Partition B	RCERB0	0Bh	RCERB_0	280Fh
Transmit Channel Enable Register Partition A	XCERA0	0Ch	XCERA_0	2810h
Transmit Channel Enable Register Partition B	XCERB0	0Dh	XCERB_0	2811h
Receive Channel Enable Register Partition C§	RCERC0	10h	RCERC_0	2814h
Receive Channel Enable Register Partition D§	RCERD0	11h	RCERD_0	2815h
Transmit Channel Enable Register Partition C§	XCERC0	12h	XCERC_0	2816h

† I/O mapped registers are accessible at addresses in I/O space.
‡ Access done using the subbanked addressing scheme
§ VC5402A register description in the VC5402A data manual is: “Additional channel enable register for 128-channel selection”

Table 9. McBSP Port#0 Control Registers (Continued)

	VC5402A		VC5502	
	Data Memory Mapped Registers		I/O Mapped Registers†	
McBSP Port#0 Control Register Description	Register Name	Address: 0039h Sub-Address‡	Register Name	Word Address
Transmit Channel Enable Register Partition D§	XCERD0	13h	XCERD_0	2817h
Receive Channel Enable Register Partition E§	RCERE0	14h	RCERE_0	2818h
Receive Channel Enable Register Partition F§	RCERF0	15h	RCERF_0	2819h
Transmit Channel Enable Register Partition E§	XCERE0	16h	XCERE_0	281Ah
Transmit Channel Enable Register Partition F§	XCERF0	17h	XCERF_0	281Bh
Receive Channel Enable Register Partition G§	RCERG0	18h	RCERG_0	281Ch
Receive Channel Enable Register Partition H§	RCERH0	19h	RCERH_0	281Dh
Transmit Channel Enable Register Partition G§	XCERG0	1Ah	XCERG_0	281Eh
Transmit Channel Enable Register Partition H§	XCERH0	1Bh	XCERH_0	281Fh

† I/O mapped registers are accessible at addresses in I/O space.
‡ Access done using the subbanked addressing scheme
§ VC5402A register description in the VC5402A data manual is: “Additional channel enable register for 128-channel selection”

Both the VC5402A and the VC5502 support bootloading via the serial port. On the VC5502, the GPIO4 can be used as a handshaking signal when using the McBSP serial-slave boot mode. Please refer to the bootloader section of this document for more details.

The McBSP module behavior upon entering the idle state depends on the source of the clock and frame synchronization signals. Assuming the idle control bit is set, if these signals are provided by an external source, the McBSP will enter the idle state after the current McBSP activity is completed, or enter the idle state immediately if no data transfer activity exists. If these signals are internally generated by the DSP, the McBSP will enter the idle state immediately if both transmitter and receiver are in reset (XRST = ‘0’ and RRST = ‘0’). Otherwise, the IDLE state is not entered. The McBSP and the DMA can wake up from the idle state automatically if the McBSP gets a new data transfer.

6 Interrupts [S/H]

VC5502 vector-relative locations and priorities for all internal and external interrupts are shown in Table 10.

Table 10. VC5502 Interrupt Locations and Priorities

Name	Software (Trap) Equivalent	Location (Hex bytes)	Priority	Function
RESET	SINT0	0	0	Reset (hardware and software)
NMI	SINT1	8	1	Nonmaskable interrupt
INT0	SINT2	10	3	External interrupt #0
INT2	SINT3	18	5	External interrupt #2
TINT0	SINT4	20	6	Timer #0 interrupt
RINT0	SINT5	28	7	McBSP #0 receive interrupt
RINT1	SINT6	30	9	McBSP #1 receive interrupt
XINT1	SINT7	38	10	McBSP #1 transmit interrupt
LCKINT	SINT8	40	11	PLL lock interrupt
DMAC1	SINT9	48	13	DMA Channel #1 interrupt
DSPINT	SINT10	50	14	Interrupt from host
INT3/WDTINT†	SINT11	58	15	External interrupt #3 or Watchdog timer interrupt
RINT2	SINT12	60	17	McBSP #2 receive interrupt
XINT2	SINT13	68	18	McBSP #2 transmit interrupt
DMAC4	SINT14	70	21	DMA Channel #4 interrupt
DMAC5	SINT15	78	22	DMA Channel #5 interrupt
INT1	SINT16	80	4	External interrupt #1
XINT0	SINT17	88	8	McBSP #0 transmit interrupt
DMAC0	SINT18	90	12	DMA Channel #0 interrupt
–	SINT19	98	16	Software interrupt #19
DMAC2	SINT20	A0	19	DMA Channel #2 interrupt
DMAC3	SINT21	A8	20	DMA Channel #3 interrupt
TINT1	SINT22	B0	23	Timer #1 interrupt
IIC	SINT23	B8	24	I^2C interrupt
BERR	SINT24	C0	2	Bus Error interrupt
DLOG	SINT25	C8	25	Data Log interrupt

† WDTINT is only available when the Watchdog Timer is used as a general-purpose timer.

Table 10. VC5502 Interrupt Locations and Priorities (Continued)

Name	Software (Trap) Equivalent	Location (Hex bytes)	Priority	Function
RTOS	SINT26	D0	26	Real-time Operating System interrupt
–	SINT27	D8	27	Software interrupt #27
–	SINT28	E0	28	Software interrupt #28
–	SINT29	E8	29	Software interrupt #29
–	SINT30	F0	30	Software interrupt #30
	SINT31	F8	31	Software interrupt #31

† WDTINT is only available when the Watchdog Timer is used as a general-purpose timer.

VC5402A vector-relative locations and priorities for all internal and external interrupts are shown in Table 11.

Table 11. VC5402A Interrupt Locations and Priorities

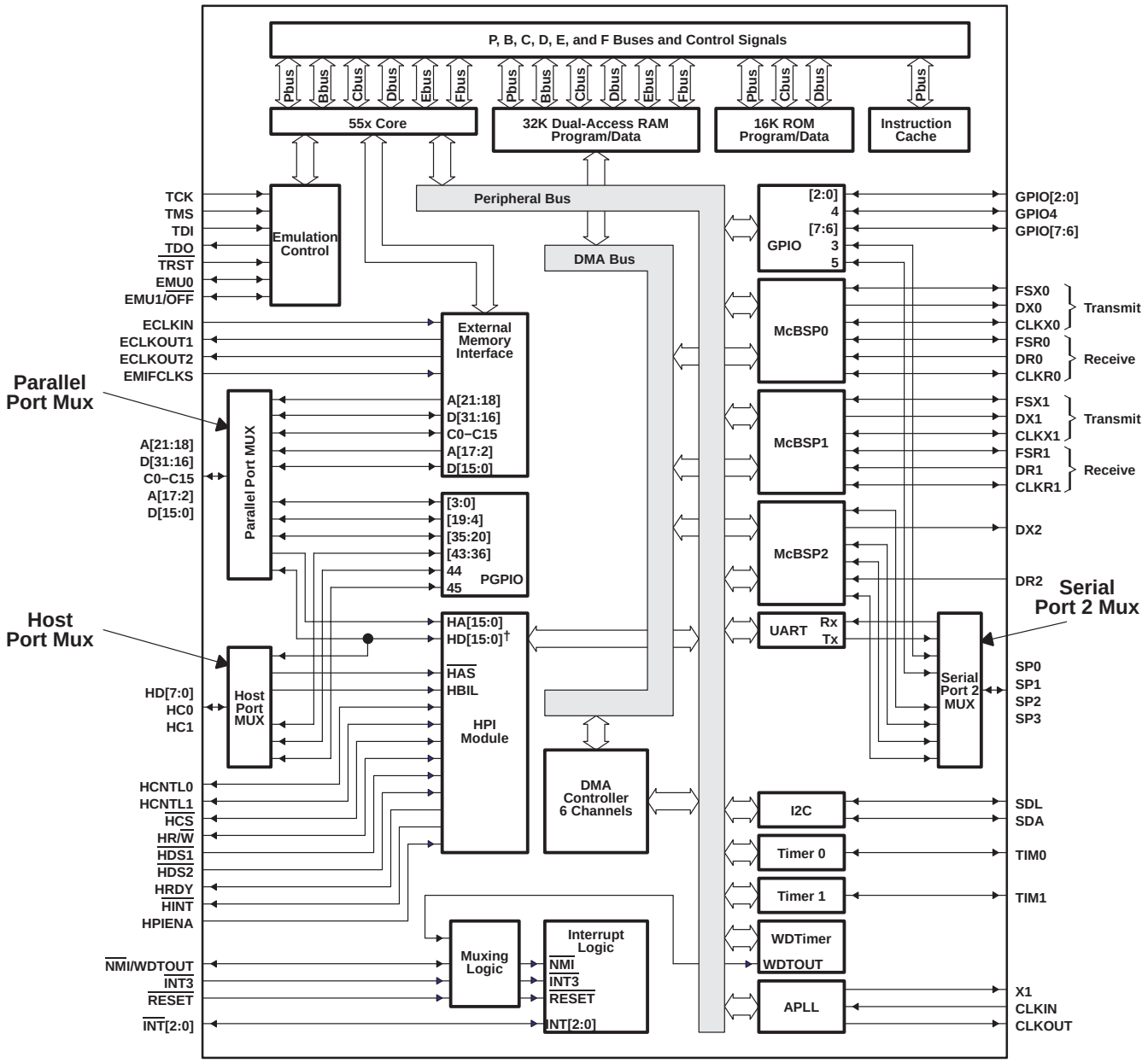
Name	Trap/INTR Number (K)	Location		Priority	Function
		Decimal	Hex		
$\overline{\text{RS}}$, SINTR	0	0	00	1	Reset (hardware and software reset
$\overline{\text{NMI}}$, SINT16	1	4	04	2	Nonmaskable interrupt
SINT17	2	8	08	–	Software interrupt #17
SINT18	3	12	0C	–	Software interrupt #18
SINT19	4	16	10	–	Software interrupt #19
SINT20	5	20	14	–	Software interrupt #20
SINT21	6	24	18	–	Software interrupt #21
SINT22	7	28	1C	–	Software interrupt #22
SINT23	8	32	20	–	Software interrupt #23
SINT24	9	36	24	–	Software interrupt #24
SINT25	10	40	28	–	Software interrupt #25
SINT26	11	44	2C	–	Software interrupt #26
SINT27	12	48	30	–	Software interrupt #27
SINT28	13	52	34	–	Software interrupt #28
SINT29	14	56	38	–	Software interrupt #29
SINT30	15	60	3C	–	Software interrupt #30

Table 11. VC5402A Interrupt Locations and Priorities (Continued)

Name	Trap/INTR Number (K)	Location		Priority	Function
		Decimal	Hex		
$\overline{\text{INT0}}$, SINT0	16	64	40	3	External user interrupt #0
$\overline{\text{INT1}}$, SINT1	17	68	44	4	External user interrupt #1
$\overline{\text{INT2}}$, SINT2	18	72	48	5	External user interrupt #2
TINT, SINT3	19	76	4C	6	Timer interrupt
RINT0, SINT4	20	80	50	7	McBSP #0 receive interrupt (default)
XINT0, SINT5	21	84	54	8	McBSP #0 transmit interrupt (default)
RINT2, SINT6	22	88	58	9	McBSP #2 receive interrupt (default)
XINT2, SINT7	23	92	5C	10	McBSP #2 transmit interrupt (default)
$\overline{\text{INT3}}$, SINT8	24	96	60	11	External user interrupt #3
$\overline{\text{HINT}}$, SINT9	25	100	64	12	HPI interrupt
RINT1, SINT10	26	104	68	13	McBSP #1 receive interrupt (default)
XINT1, SINT11	27	108	6C	14	McBSP #1 transmit interrupt (default)
DMAC4,SINT12	28	112	70	15	DMA channel 4 (default)
DMAC5,SINT13	29	116	74	16	DMA channel 5 (default)
Reserved	30−31	120−127	78−7F	−	Reserved

7 Pin Muxing [N]

To reduce pin count and therefore package footprint, the number of pins on the VC5502 have two functions. In order to achieve this dual functionality, internal multiplexers are utilized. Three muxes are included in the VC5502 (see Figure 2) to control the configuration of these dual-function pins: the parallel port mux, the host port mux, and the Serial Port 2 Mux. The state of these muxes is set at reset based on the state of the GPIO6 and GPIO7 pins. The external bus selection register (XBSR) shows the configuration of these muxes after the VC5502 comes out of reset. These muxes represent a significant change from the VC5402A architecture which does not have any muxing for these pins.



† HD[15:8] are not used when the HPI is operated in multiplexed mode.

Figure 6. VC5502 Functional Diagram

7.1 Parallel Port Mux

The parallel port mux of the VC5502 consists of 20 address signals, 32 data signals, and 16 control signals. The parallel bus supports two different modes (determined by the state of the GPIO6 pin at reset).

- Full EMIF mode: The EMIF's 20 address, 32 data, and 16 control signals are routed to the corresponding external parallel bus address, data, and control signals. The HPI 8-bit multiplexed mode can also be selected in parallel with the full-EMIF mode
- Non-multiplexed HPI mode: The HPI is enabled with its 16 address, 16 data, and 9 control signals routed to the corresponding address, data, and control signals of the external parallel bus. Moreover, 16 control signals, 4 address signals, and 16 data signals of the external parallel bus that are not needed for HPI operation are set to general-purpose I/O. EMIF is not available in this mode.

7.2 Host Port Mux

The VC5502 host port mux controls the function of eight data signals (pins HD[7:0]) and two control signals (pins HC0 and HC1). The host port mux supports two different modes (determined by the state of the GPIO6 pin at reset).

- 8-bit multiplexed mode: The HPI's 8 data and 2 control signals are routed to their corresponding pins on the host-port mux.
- Parallel general-purpose I/O mode: All pins on the host-port mux are routed to the PGPIO. The HPI is enabled to 16-bit (non-multiplexed) mode, but communicates through the parallel-port mux.

NOTE: The HPI does not have access to external memory or the peripheral I/O space. The HPI cannot access internal DARAM space when the device is in reset.

7.3 Serial Port 2 Mux

The VC5502 has three serial ports: McBSP0, McBSP1, and McBSP2, each of which has six signals. The signals for McBSP0 and McBSP1 are directly routed to pins on the VC5502. Four of the pins for McBSP2 are multiplexed with two pins of the on-chip UART and two pins of the GPIO.

The mode of the Serial Port 2 Mux, controlled by the state of the GPIO7 pin at reset, determines which signals are routed to the VC5502 pins. Refer to Table 12.

Table 12. VC5502 Routing of Serial Port 2 Mux Signals

Pin	Serial Port 2 Mux Mode = 0 (GPIO7 Setting at Reset = 0)	Serial Port 2 Mux Mode = 1 (GPIO7 Setting at Reset = 1)
SP0	GPIO3	CLKX2
SP1	UART.TX	CLKR2
SP2	GPIO5	FSX2
SP3	UART.RX	FSR2

When GPIO7 is low at reset, McBSP2 will be disabled and any writes or reads to/from its registers will result in a bus error if the PERITOEN bit of the time-out control register is set to 1. When GPIO7 is high at reset, the UART will be disabled and any writes or reads to/from its registers will result in a bus error if the PERITOEN bit of the time-out control register is set to 1. GPIO3 and GPIO5 will not be available during this mode of the Serial Port 2 Mux. Figure 7 shows the signal interface to the Serial Port 2 Mux.

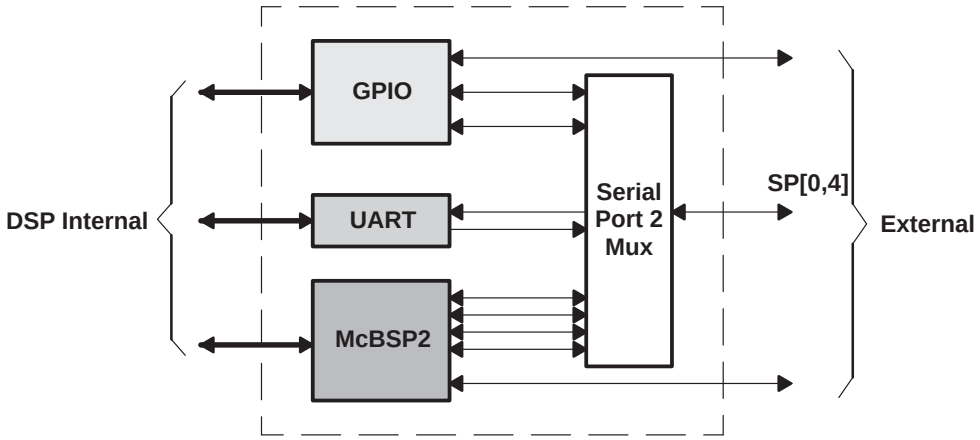


Figure 7. Serial Port 2 Mux Interface

8 Host Port Interface (HPI)

The HPI on the VC5502 and VC5402A provides a parallel port through which an external host processor (host) can access memory internal to the DSP. However, the host does not have direct access to memory that is external to the DSP. The DSP functions as a slave to the HPI. The HPI on both devices can be configured as an 8-bit or a 16-bit interface.

8.1 HPI Access to Internal DSP Memory

The VC5402A HPI allows the host access to the entire on-chip memory range of the DSP. The host and the DSP both have access to the on-chip RAM at all times and host accesses are always synchronized to the DSP clock. If the host and the DSP contend for access to the same location, the host has priority, and the DSP waits for one cycle. Note that since host accesses are always synchronized to the VC5402A clock, an active input clock (CLKIN) is required for HPI accesses during IDLE states, and host accesses are not allowed while the VC5402A reset pin is asserted.

On the VC5502, the host can access the first 32K words (64K Bytes) of internal memory except for addresses 00 0000h–00 005Fh, which are reserved for the memory mapped registers of the CPU. The host cannot access DSP peripheral registers or external memory through the HPI. The host must provide 15-bit addresses to the HPI, where each address points to a word (a 16-bit value) in memory. Host activity is asynchronous to the clock that drives the HPI, which is the fast peripherals clock (SYSCLK1) of the DSP. No host access should occur when the HPI is placed in IDLE. The host cannot wake up the DSP through the DSP_INT bit of the HPIC1 register when the DSP is in IDLE mode.

8.2 HPI Modes of Operation

The VC5402A HPI can be used to interface to an 8-bit or 16-bit host. When the address and data buses for external I/O is not used (to interface to external devices in program/data/IO spaces), the VC5402A HPI can be configured as an HPI16 to interface to a 16-bit host. This configuration can be accomplished by connecting the HPI16 pin to logic “1”. When the VC5402A HPI16 pin is connected to logic “0”, the HPI is configured as an HPI8. The HPI8 is an 8-bit parallel port for interprocessor communication. The host communicates with the HPI8 through three dedicated registers — the HPI address register (HPIA), the HPI data register (HPID), and the HPI control register (HPIC). The HPIA and HPID registers are only accessible by the host, and the HPIC register is accessible by both the host and the VC5402A.

The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface. In HPI16 mode only nonmultiplexed address/data modes are supported where 15-bit address bus are used to allow access to all internal memory (including internal extended address pages). The HPI16 acts as a slave to a 16-bit host processor and allows access to the on-chip memory of the DSP. Access to the entire on-chip RAM through the DMA bus is possible from a host via the HPI.

The C5402A 8-bit bidirectional data bus of the HPI can be used as general-purpose input/output (GPIO) pins when the HPI is disabled (HPIENA = 0) or when the HPI is used in HPI16 mode (HPI16 = 1).

The VC5502 HPI also supports interfaces to 8- and 16-bit hosts. The HPI is configured for 8-bit multiplexed mode when the GPIO6 pin of the DSP is sampled high at reset. The 16-bit mode is selected if the GPIO6 pin is sampled low at reset.

In the 8-bit multiplexed mode, an 8-bit data bus (HD[7:0]) carries both addresses and data. Each host cycle on the bus consists of two consecutive 8-bit transfers. Data flow between the host and the HPI uses a 16-bit temporary storage register called HPID. Data arriving from the host is held in HPID until the data can be stored elsewhere in the DSP. Data to be sent to the host is held in HPID until the HPI is ready to perform the transfer. Effectively, this register is a port through which the host accesses two first-in, first-out buffers (FIFOs). A read FIFO supports host read cycles, and a write FIFO supports host write cycles. Both read and write FIFOs are eight words deep (each word 16 bits). If the host is performing multiple reads or writes to consecutive memory addresses (autoincrement HPID cycles), the FIFOs are used for bursting. The HPI DMA logic performs reads or writes a burst of four words at a time when accessing one of the FIFOs. In this mode, when the HPI is enabled (HPIENA signal high) pins HD[7:0] can be used as GPIO pins. The HPI DMA logic requires no programming; it automatically stores or fetches data using the address provided by the host.

In the 16-bit non-multiplexed mode, the HPI provides separate address and data buses. Each host cycle on the data bus consists of one 16-bit transfer. In this nonmultiplexed mode, the FIFO memory acts as a single register (only one location is used) and bursting is not used. When the HPI is enabled (HPIENA signal high), the HPI data bus pins, HD[15:0] can be used for general-purpose I/O (GPIO).

The HPI can access the entire DARAM space of the VC5502 excluding memory-mapped CPU registers; however, it does not have access to external memory of the peripheral I/O space. The HPI cannot access internal DARAM space when the device is in reset.

8.3 HPI Memory Map

The HPI memory maps for the VC5502 and VC5402A are shown in Figure 8 and Figure 9, respectively.

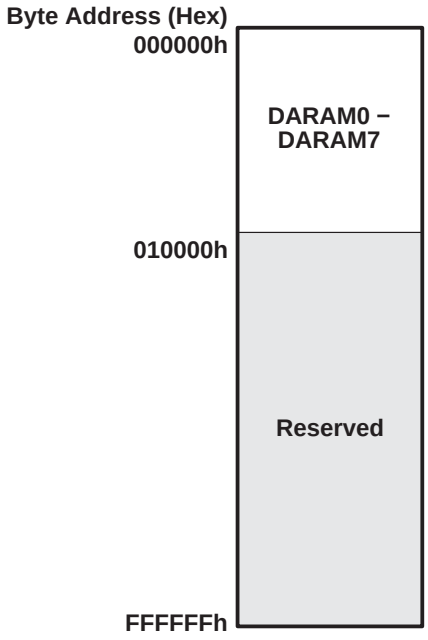


Figure 8. VC5502 HPI Memory Map

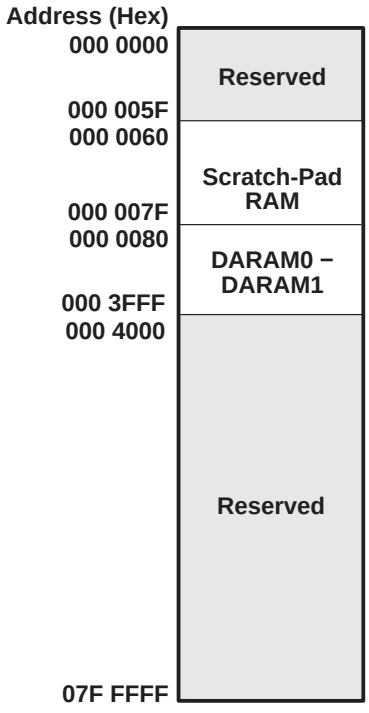


Figure 9. VC5402A HPI Memory Map

9 Timers [H/S]

Table 13. Timers Differences

Device	Total Number of Timers	Number of Bits	Type
VC5402A	1	16	General-Purpose (GP)
VC5502	4	64	2 General-Purpose, 1 watchdog, 1 DSP/BIOS counter

The VC5402A features a 16-bit timing circuit with a 4-bit prescaler. The timer counter is decremented by one every CLKOUT cycle. Each time the counter decrements to 0, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits.

The VC5502 has four 64-bit timers: Timer 0, Timer 1, Watchdog Timer (WDT), and Timer 3. The first two timers, Timer 0 and Timer 1, are mainly used as general-purpose timers. The Watchdog Timer can be used as either a general-purpose timer or a watchdog timer. The output pin of the Watchdog Timer, WDTOUT, is multiplexed with the NMI input pin. It can also be internally connected to the NMI, RESET, and INT3 signals of the VC5502. The fourth timer, Timer 3, is reserved as a DSP/BIOS counter; users have no access to this timer. No interrupts are needed from this timer; therefore, the timer output is not internally connected to the CPU interrupt logic.

The interrupt signal (TINT) of the Watchdog Timer can be internally connected to the NMI, RESET, and INT3. The interrupt signals of Timer 0 and Timer 1 are directly connected to the interrupt logic of the DSP. The interrupts for Timer 0 and Timer 1 are maskable and can be enabled or disabled.

10 DMA [S]

The DMA controllers of the VC5402A and VC5502 DSP have the following common features:

- Six channels, which allow the DMA controller to track the context of six independent block transfers. Each DMA channel has independently programmable priorities
- The source and destination address registers can have configurable indexes through memory on each read and write transfer, respectively.
- On completion of a half- or entire-block transfer, each DMA channel may send an interrupt to the CPU in response to the operational events.
- Full address range. The DMA can access the full extended address range implemented on the device. On the VC5502, the DMA controller can access all of the internal, external memory space and some of the IO memory spaces (which contains registers for the DSP peripherals such as McBSP, UART, GPIO, PGPIO, and I2C). On the VC5402A, the DMA access extends to the on-chip memory, on-chip peripherals, and external memory. For more information, refer to chapter 3, *Memory*, in the *TMS320C54x DSP, CPU and Peripherals, Reference Set Volume 1* (SPRU131).
- Event synchronization. DMA transfers in each channel can be dependent on the occurrence of selected events.

However, there are some distinct differences between the DMA controllers of each device:

- On the VC5402A, the DMA always has higher priority than the CPU for both internal and external accesses. On the VC5502, however, the CPU always has priority over the DMA controller for accesses to the same DARAM block in internal memory.

- The VC5502 DMA controller has a dedicated idle domain. You can configure the DMA controller into a low-power state by turning off this domain. Each multichannel buffered serial port (McBSP) on the VC5502 has the ability to temporarily take the DMA domain out of this idle state when the McBSP needs the DMA controller.
- The VC5502 supports16 separate synchronization events and each channel can be tied to separate synchronization event independent of the other channels. Synchronization events are selected by programming the SYNC field in the channel-specific DMA Channel Control Register (DMA_CCR). The VC5402A supports only 14 separate synchronization events. The DSYN bit field of the DMSEFCn register selects the synchronization event for a channel. Refer to Table 14.
- The VC5502 has an Auto-wakeup/Idle function for McBSP to DMA to on-chip memory data transfers when the DMA and the McBSP are both set to IDLE. In the case that the McBSP is set to external clock mode and the McBSP and the DMA are set to idle, the McBSP and the DMA can wake up from IDLE state automatically if the McBSP gets a new data transfer. The McBSP and the DMA enter the idle state automatically after data transfer is complete. [The clock generator (PLL) should be active and the PLL core should not be in power-down mode for the Auto-wakeup/Idle function to work.]
- The VC5402A DMA configuration and operation is achieved by a set of memory-mapped control registers. The DMA registers are memory-mapped using a register subaddressing scheme. Register subaddressing involves multiplexing a set of registers to a single location in the memory map. A subbank addressing register is used to control the multiplexer. A subbank data register is used to actually read or write data to the desired subaddressed register.
- The VC5502 DMA configuration registers do not use the subaddressing scheme. There are two registers that affect all channels: the global control register (DMAGCR) and the global time-out control register (DMAGTCR). In addition, for each of the DMA channels, there are 16 channel configuration registers. All the DMA configuration registers are mapped to I/O space. Please refer to the TMS320VC5502 data manual, SPRS166C, for the specific I/O address of each register.
- The VC5402A DMA supports external accesses to extended program, extended data, and extended I/O memory. A maximum of two DMA channels can be used for external memory accesses (One for external reads and one for external writes.) The control of the bus is arbitrated between the CPU and the DMA. While the DMA or CPU is in control of the external bus, the other will be held-off via wait states until the current transfer is complete. The DMA takes precedence over XIO requests. Single-word (16-bit) transfers are supported for external accesses. The VC5402A DMA does not support:
  - transfers from the peripherals to external memory
  - transfers from external memory to the peripherals
  - external-to-external transfers
  - synchronized external transfers

There are also differences in the operation of the indexing modes and the DMA interrupts between the two devices. Please refer to the DMA documentation for both devices for more information.

Table 14. Synchronization Events Differences

VC5402A		VC5502	
Synchronization Event	**DMSEFCn Register Setting (DSYN Field)**	**Synchronization Event**	**DMA_CCR (Sync Field)**
No synchronization event	0000	No synchronization event	00000b
McBSP0 receive event (REVT0)	0001	McBSP0 receive event (REVT0)	00001b
McBSP0 transmit event (XEVT0)	0010	McBSP0 transmit event (XEVT0)	00010b
McBSP1 receive event (REVT1)	0101	McBSP1 receive event (REVT1)	00101b
McBSP1 transmit event (XEVT1)	0110	McBSP1 transmit event (XEVT1)	00110b
McBSP2 receive event (REVT2)	0011	Timer 0 event	01101b
McBSP2 transmit event (XEVT2)	0100	Timer 1 event	01110b
McBSP0 receive event − ABIS mode	0111	External Interrupt 0	01111b
McBSP0 transmit event − ABIS mode	1000	External Interrupt 1	10000b
McBSP1 receive event − ABIS mode	1011	External Interrupt 2	10001b
McBSP1 transmit event − ABIS mode	1100	External Interrupt 3	10010b
McBSP2 receive event − ABIS mode	1001	I^2C Receive Event	10011b
McBSP2 transmit event − ABIS mode	1010	I^2C Transmit Event	10100b
Timer interrupt event	1101	Reserved/UART Event Serial Port 2 Mux Mode= 0: UART Rcv. Event (UARTREVT) Serial Port 2 Mux Mode= 1: Reserved	01011b
External Interrupt 3	1110	Reserved/UART Event Serial Port 2 Mux Mode= 0: UART Xmt. Event (UARTXEVT) Serial Port 2 Mux Mode= 1: Reserved	01100b
Reserved (do not use this value)	1111	Reserved/McBSP Event Serial Port 2 Mux Mode= 0: Reserved Serial Port 2 Mux Mode= 1: McBSP2 Rcv. Event (REVT2)	01001b

Table 14. Synchronization Events Differences (Continued)

VC5402A		VC5502	
Synchronization Event	**DMSEFCn Register Setting (DSYN Field)**	**Synchronization Event**	**DMA_CCR (Sync Field)**
		Reserved/McBSP Event Serial Port 2 Mux Mode= 0: Reserved Serial Port 2 Mux Mode= 1: McBSP2 Xmt. Event (XEVT2)	01010b
		Reserved (do not use these values)	other

11 Bootloader [H]

Both the VC5402A and VC5502 offer several options to download code into the DSP on-chip RAM. Refer to Table 15.

On the VC5502 bootloader, GPIO4 is configured as an output and used for multiple functions depending on the boot mode selected. Refer to TI application report *Using the TMS320VC5502 Bootloader* (SPRA911), for more details.

External pins BOOTM2, BOOTM1, and BOOTM0 select the boot configuration. The values of BOOTM[2:0] are latched with the rising edge of the RESET input. BOOTM2 is shared with GPIO2, BOOTM1 is shared with GPIO1, and BOOTM0 is shared with GPIO0. Such BOOTM pins do not exist on the VC5402A.

Table 15. Boot Modes Differences

	VC5402A		VC5502	
Boot Mode Source	**Support**	**Condition**	**Support**	**Condition**
Standard serial boot from McBSP0 (16-bit)	Yes	BRINT0 = 1	Yes	BOOTM[2:0]= 010
Standard serial boot from McBSP0 (8-bit)	Yes	BRINT1 = 1	No	–
SPI EEPROM boot (8-bit address EEPROM) using McBSP1	Yes	INT3 Flag set	No	–
SPI EEPROM boot (24-bit address EEPROM) using McBSP0	No	–	Yes	BOOTM[2:0]= 001
HPI boot, multiplexed mode	No	–	Yes	BOOTM[2:0]= 101
HPI boot, non-multiplexed mode	Yes	INT2 Flag set	Yes	BOOTM[2:0]= 101
Parallel EMIF boot from 16-bit external asynchronous memory	No	–	Yes	BOOTM[2:0]= 011
Parallel boot modes (8-bit and 16-bit supported)	Yes	Valid keyword in boot table‡	No	–
Direct execution (no boot) from 32-bit external asynchronous memory	No	–	Yes	BOOTM[2:0]= 100
Direct execution (no boot) from 16-bit external asynchronous memory	No	–	Yes	BOOTM[2:0]= 000
I^2C EPROM† boot	No	–	Yes	BOOTM[2:0]= 110
UART boot	No	–	Yes	BOOTM[2:0]= 111
I/O boot modes (8-bit and 16-bits supported)	Yes	BIO pin low and Valid keyword in boot table‡	No	–

† Supporting EPROMs up to 512K bits
‡ Refer to SPRA618 for more details

12 Power Saving Modes [H/S]

The VC5502 is divided into six clock domains to power-off the main clock to the portions of the device that are not being used. The six domains are:

- CPU Domain
- Master Port Domain (includes DMA and HPI modules)
- I-Cache
- Peripherals Domain
- Clock Generator Domain
- EMIF Domain

The current state of all domains is collectively called the idle configuration. The user can choose which domains are active and which are idle at any given time. The Idle function is implemented for low power consumption; it achieves low power consumption by gating the clock to unused parts of the chip, and/or setting the clock generator (PLL) and the internal oscillator to a power-down mode.

The VC5502 has three idle modes it may be configured to operate in:

- Idle2 mode: In this mode all modules except the CLOCK module are set to idle state.
- Idle3 mode: In this mode all modules (including the CLOCK module) are set to idle state.
- Idle3 mode with Internal oscillator disabled: In this state, all modules (including the CLOCK module) are set to the idle state and the internal oscillator is set to the power-down mode. This is the lowest power-consuming state that VC5502 can be placed under.

On the VC5502, the McBSP module behavior upon entering the idle state depends on the source of the clock and frame synchronization signals. Assuming the idle control bit is set, if these signals are provided by an external source, the McBSP will enter the idle state after the current McBSP activity is completed, or enter the idle state immediately if no data transfer activity exists. If these signals are internally generated by the DSP, the McBSP will enter the idle state immediately if both transmitter and receiver are in reset (XRST = ‘0’ and RRST = ‘0’). Otherwise, the IDLE state is not entered. The McBSP and the DMA can wake up from the idle state automatically if the McBSP gets a new data transfer.

NOTES:

- Each module in the peripherals domain (with the exception of the HPI) will immediately go into idle if it has no data transfer activity. If the module being set to idle has activity, it will wait until the activity completes before going into idle. The HPI will go into idle regardless of whether or not there is data transfer taking place. In this case, software must confirm that the HPI has no activity before setting it to idle.
- The internal memory blocks and external memory are shared by two domains (CPU and DMA). When both domains are idled, memory accesses are disabled.

The VC5402A device, however, does not have idle domains. Instead, the VC5402A has power-down modes in which it enters a dormant state and dissipates less power than normal operation while maintaining the CPU contents. This allows operations to continue unaltered when the power-down mode is terminated. Power-down modes are invoked either by executing the IDLE 1, IDLE 2 or IDLE 3 instructions, or by driving the HOLD signal low with the HM status bit set to 1. Please refer to section 6.11 of the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (SPRU131), for mode details.

13 Inter-Integrated Circuit (I^2C) [N]

The VC5502 adds an inter-integrated circuit (I^2C) multi-master and slave interface. The I2C serial port offers compatibility with Philips. I2C-Bus. Specification, Version 2.1 (January 2000). Some features of this port include:

- Up to 400 Kbps (no fail-safe I/O buffers)
- 7-bit and 10-bit device addressing modes
- Master (transmit/receive) and slave (transmit/receive) functionality

I^2C boot load in master mode is supported on the VC5502.

14 UART [N]

The VC5502 adds a universal asynchronous receiver/transmitter (UART) on-chip peripheral. The UART performs serial-to-parallel conversions on data received from a peripheral device or modem and parallel-to-serial conversion on data received from the CPU. The CPU can read the UART status at any time. The UART includes control capability and a processor interrupt system that can be configured to minimize software management of the communications link. It also includes a programmable baud rate generator capable of dividing the CPU clock by divisors from 1 to 65535 and producing a 16y-reference clock for the internal transmitter and receiver logic.

UART bootload is also supported on the VC5502. The boot load mode selection is determined by the logic level on the GPIO[2:0] pins when sampled at reset.

The UART pins are multiplexed with the pins of McBSP2. Depending on the state of GPIO7, the Serial Port 2 Mux determines which pins are connected to the SP0, SP1, SP2, and SP3.

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