Application Report
SPRAAM4–May 2007

TMS320TCI6488 RAC Internal Precisions

Madeleine Saikaly

ABSTRACT

This document provides processing decisions for the RAC internal sub-modules contained in the TCI6488 DSP device.

Contents

List of Figures

1 RAC Overview

The receive accelerator (RAC) module in TCI6488 consists of three sub-modules:

- Front-end interface (FEI) that receives antenna data, repackages and delivers to GCCP0 and GCCP1
- Two generic correlator coprocessors (GCCP) that receive chip-rate antenna streams and provide the DSP with de-spread symbols and correlation energy results.
- Back-end interface (BEI) with direct access to enhanced direct memory access (EDMA) switch fabric. The results are put directly into memory for DSP use.

RAC block diagram is shown in Figure 1.

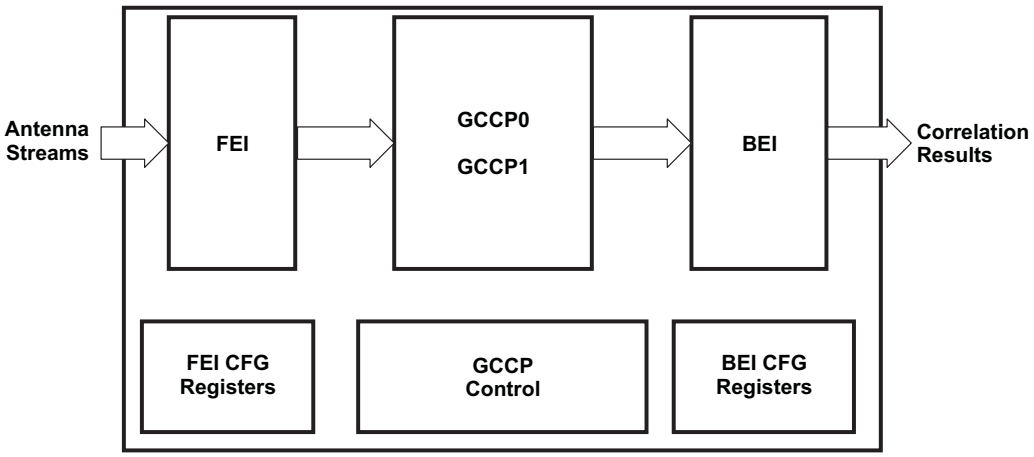

Figure 1. RAC Overview

2 Front-End Interface

The RAC front-end interface receives packets of antenna samples and the corresponding time stamp and enables GCCP processing. Typically, packets come from the antenna interface through the EDMA. The FEI has one input 64-bit data interface with the EDMA and two 128-bit output data interfaces, one with each GCCP. In addition, the FEI supports access to data memories in each GCCP through one 64-bit read/write bus.

Each FEI input sample packet contains eight chip periods worth of data. So with every 32-chip iteration period, the RAC front-end receives at least four packets. The first packet carries samples from chip period #0 to chip period #7, the second carries samples from chip period #8 to #15, the third carries samples from chip period #16 to #23 and the last carries samples from chip period #24 to #31.

The antenna samples have an over-sampling factor of 2. The packet format is shown in Figure 2:

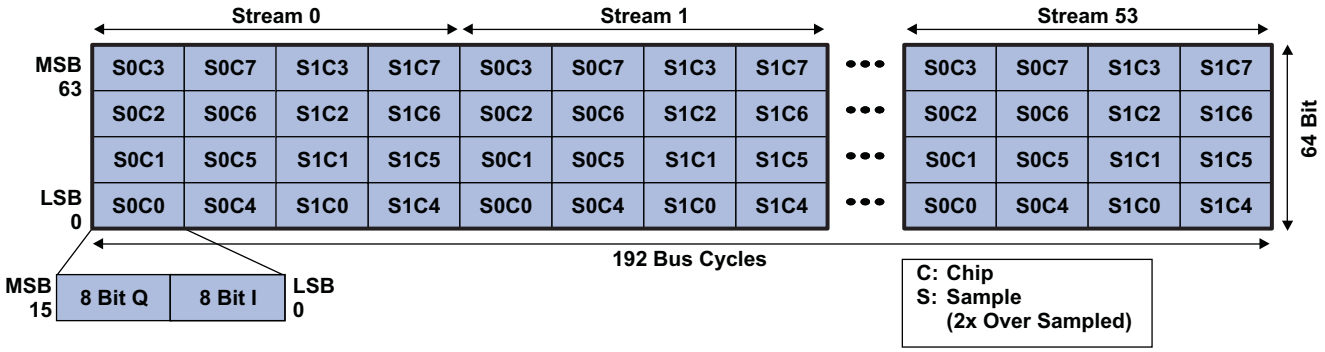

Figure 2. FEI Sample Packet Input Format

The FEI buffers the antenna samples, reformats them, and transfers them to the two GCCPs. Data output from the FEI to the GCCP is still at an over-sampling factor of 2.

3 Generic Correlation Co-Processors

The GCCP data path contains:

- Correlator and adder trees
- Code generator
- Interpolators
- Amplitude and phase adjustors (also know as rotators)
- Coherent accumulators
- Energy translators (generating complex amplitude $|x|$ or power $|x|^2$)
- Non-coherent accumulators

GCCP is built around a task-based correlation engine. A task can be either:

- A finger symbol de-spreading task (FD-SYM)
- A finger delay tracking task (FD-FT)
- A finger power estimation task (FD-FPE)
- A path monitor task (PM)
- A preamble detection task (PD)
- A stream power estimation task (SPE)

Each type of task has specific parameters and uses the data-path differently.

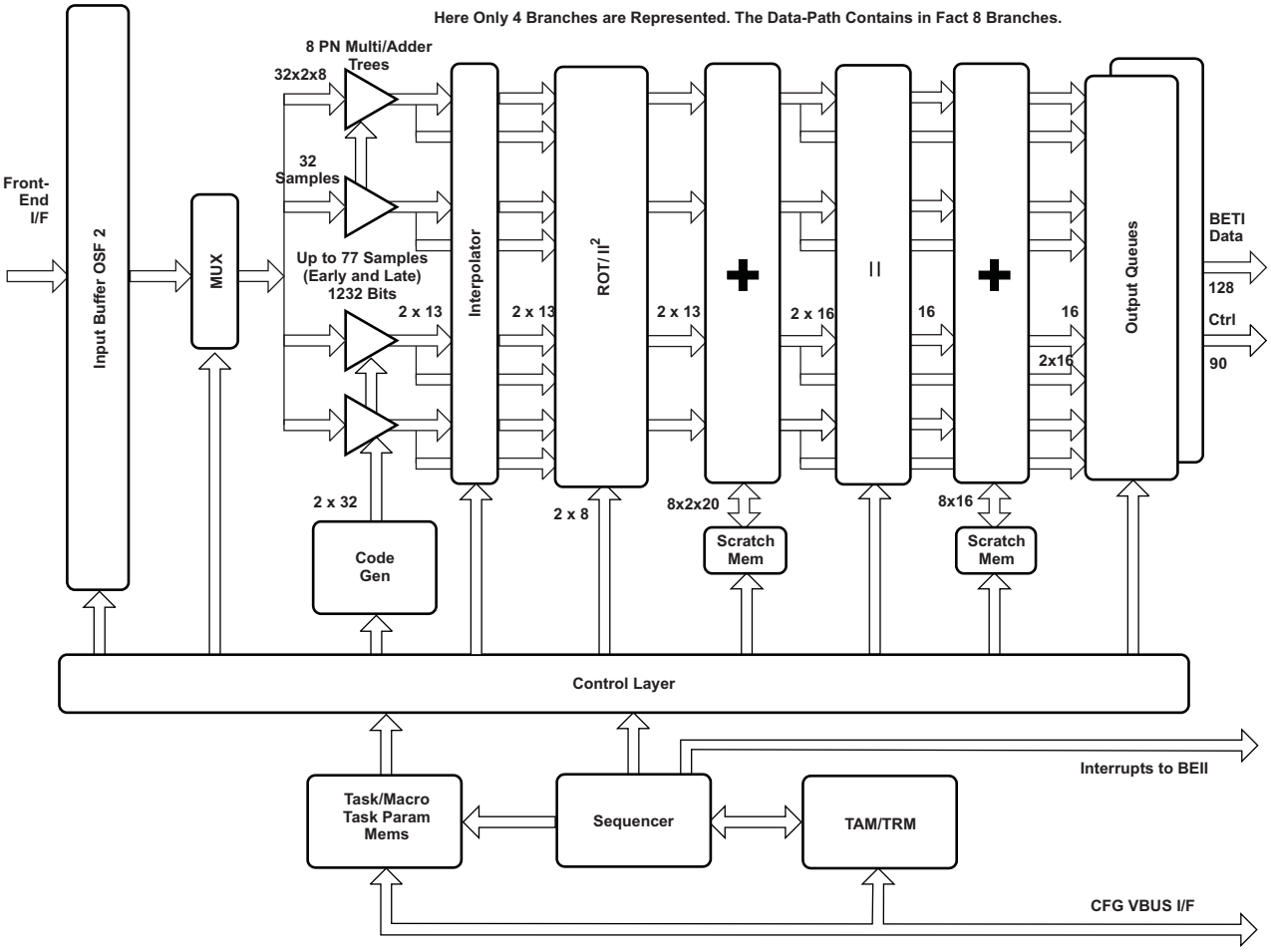

Figure 3. GCCP Architecture Overview

3.1 Preamble Detector

In PD mode, the GCCP is used to generate four coherent or eight non-coherent results per cycle. There are three search modes:

- Full-chip search
- Half-chip search
- Quarter-chip search

Each search mode can be performed in two ways:

- Non-coherent stage active
- Non-coherent stage inactive

3.1.1 Input buffer

During each iteration period, the front-end interface writes up to 54 [streams] ×32 [chip periods] × 2 [samples per chip period] = 3456 samples to the GCCP input buffer. Each sample is a 16-bit complex signed integer (I part takes the lowest eight bits and Q part takes the highest eight bits).

As shown in Figure 1 input buffer data width is 64-bit.

3.1.2 Multiplexer

The multiplexer takes the 96-samples (each is 16-bit complex) from the IQ input buffer and generates the 77 samples (each is 16-bit complex IQ) needed for the adder trees.

3.1.3 Code Generator

The code generator in PD mode is different from the common block used in other modes; the short code generator, OVSF code generator, and pilot bits demodulation are omitted. The long code generator is also different to meet the RACH preamble/CPCH preamble long code specification.

Data going from the code generator to the adder trees is 32×2 bits wide.

3.1.4 Adder Tree/Correlator

The correlation engine consists of eight parallel independent correlators. During each cycle, each correlator receives one input iteration packet and one code iteration packet. The input iteration packet consists of 32 input chips. Each input chip is a complex signed integer (2×8 bits). The code iteration packet consists of 32 code chips. Each code chip is a complex Boolean (2×1 bits) computed on-line by the code generator.

The adder tree input consists of: 77 antenna samples (each is 16-bit complex IQ) from the multiplexer, and a 32-bit I code and a 32-bit Q code from the code generator.

The output of the adder trees consists of 16 I symbols 13-bit wide and 16 Q symbols 13-bit wide going to the interpolator.

3.1.5 Interpolator

In PD mode, the interpolation is not used for full-chip search or half-chip search; it is only used for quarter-chip search.

Four branches of 4-tap complex (I, Q) interpolators are each used in parallel, in order to generate four interpolated results per cycle. Two of these branches can be summed to create an 8-tap interpolator.

Each interpolator receives a packet of correlation results data input from the adder trees, and four sets of filter coefficients, scalar signed 8-bit integer (4×4×8-bits) coefficients array. Each correlation result is a complex (I, Q) signed integer (2×13 bits).

Each interpolator generates one interpolated result which is a complex (I, Q) signed integer (2×13 bits). In total, they output eight complex 13-bit signed integers (8×2×13-bits) to the rotator when non-coherent memory is enabled; otherwise they output four complex 13-bit signed integers (4×2×13-bits) to the rotator when non-coherent memory is not active.

3.1.6 Rotator

In PD mode, the rotator is not used for full-chip search or half-chip search; it is only used for quarter-chip search.

The rotator has eight branches of complex multipliers. Each branch data input consists of a 2×13-bit complex (I, Q) signed integer from the interpolator and a 2×8-bit complex (I, Q) signed integer from the phaser.

The output of each branch rotator is a 2×13-bit complex (I, Q) signed integer data going to coherent memory.

3.1.7 Power Computation

Power computation is not used in the PD mode.

3.1.8 Coherent Accumulation

In PD mode, all eight components of the coherent accumulation are active and up to eight results are generated. These are dumped in parallel directly to the output queues if non-coherent accumulation is not active, or to the amplitude sub-module if non-coherent accumulation is active.

The coherent accumulator receives a packet of rotated results from the rotator. The packet contains up to eight rotated results. Each rotated result is a 2×13-bit complex (I, Q) signed integer.

The coherent accumulator generates a packet of accumulated results. The packet contains up to eight accumulated results. Each accumulated result is a 2×16-bit complex (I, Q) signed integer. It can also be reduced to a 2×8-bit complex (I, Q) signed integer when written into the output queues.

3.1.9 Amplitude Computation

The amplitude sub-module is bypassed when non-coherent accumulation is not-active.

When non-coherent accumulation is active, input to the amplitude sub-module is the eight results from the coherent accumulation. Each accumulated result is a 2×16-bit complex (I, Q) signed integer.

Output from the amplitude sub-module is the eight amplitude results that are fed to the non-coherent accumulator. Each amplitude result is a 16-bit scalar unsigned integer.

3.1.10 Non-coherent Accumulation

Up to eight 16-bit scalar unsigned integer amplitude results from the amplitude computation sub-module are fed to the non-coherent accumulator.

When a non-coherent duration is finished, final results are dumped into the output queues. Each output non-coherent accumulation result is a 16-bit scalar unsigned integer.

3.1.11 Output Queues

Correlation results, either from coherent accumulation (2×8-bit complex (I, Q) signed integer) or non-coherent accumulation (16-bit scalar unsigned integer) stages are fed into the output queues.

The output data bus from the queues to the BEI is 128-bit wide.

3.1.12 Mean Value in Post-Processing

This sub-module is in the RAC back-end interface. The mean value is performing the sum of outgoing offsets results for PD task.

Input is the amplitude 16-bit scalar unsigned integer array.

The output mean value is a 32-bit scalar unsigned integer.

3.2 Path Monitor

In PM mode, the GCCP is used to generate four coherent or eight non-coherent results per cycle. There are three search modes:

- Full-chip search
- Half-chip search
- Quarter-chip search

Each search mode can be performed in two ways:

- Non-coherent stage active
- Non-coherent stage inactive

3.2.1 Input Buffer

During each iteration period, the FEI writes up to 54 [streams] × 32 [chip periods] × 2 [samples per chip period] = 3456 samples to the GCCP input buffer. Each sample is a 16-bit complex signed integer (the I part takes the lowest eight bits and the Q part takes the highest eight bits).

The input buffer data width is 64-bit, as shown in Figure 1.

3.2.2 Multiplexer

The multiplexer takes the 96 samples (each is 16-bit complex) from the IQ input buffer and generates the 77 samples (each is 16-bit complex IQ) needed for the adder trees.

3.2.3 Code Generator

In PM mode, the following code generator sub-blocks are active:

- Long code generator generates gold code scrambling codes
- Short code generator generates gold code scrambling codes
- OVSF code generator generates OVSF channelisation codes
- Pilot bits demodulation uncovers the pilot bit modulation on DPCC

Data going from the code generator to the adder trees is 32×2 bits wide.

3.2.4 Adder Tree/Correlator

The correlation engine consists of eight parallel independent correlators. During each cycle, each correlator receives one input iteration packet and one code iteration packet. The input iteration packet consists of 32 input chips. Each input chip is a complex signed integer (2×8 bits). The code iteration packet consists of 32 code chips. Each code chip is a complex Boolean (2×1 bits) computed on-line by the code generator.

The adder tree input consists of: 77 antenna samples (each is 16-bit complex IQ) from the multiplexer, and a 32-bit I code and a 32-bit Q code from the code generator.

The output of the adder trees consists of 16 I symbols 13-bit wide and 16 Q symbols 13-bit wide going to the interpolator.

3.2.5 Interpolator

In PM mode, the interpolation is not used for full-chip search or half-chip search; it is only used for quarter-chip search.

Four branches of 4-tap complex (I, Q) interpolators are each used in parallel in order to generate four interpolated results per cycle. Two of these branches can be summed to create an 8-tap interpolator.

Each interpolator receives a packet of correlation results. The packet contains four results. Each correlation results is a complex (I, Q) signed integer (2×13 bits).

Each interpolator generates one interpolated result. It is a complex (I, Q) signed integer (2x13 bits).

In total, the Interpolators receive 16×2×13-bits data input from the adder trees and four sets of filter coefficients scalar signed 8-bit integer (4×4×8-bits) coefficients array. They output eight complex 13-bit signed integers (8×2×13-bits) to the rotator when non-coherent memory is enabled, otherwise they output four complex 13-bit signed integers (4×2×13-bits) to the rotator when non-coherent memory is not-active.

3.2.6 Rotator

In PM mode all eight rotators are active.

The rotator has eight branches of complex multipliers. Each branch data input consists of 2×13-bit complex (I, Q) signed integer from Interpolation and 2×8-bit complex (I, Q) signed integer from the phaser.

The output of each branch rotator is 2×13-bit complex (I, Q) signed integer data going to coherent memory.

3.2.7 Power Computation

Power computation is not used in PM mode.

3.2.8 Coherent Accumulation

In PM mode, all eight components of the coherent accumulation are active and up to eight results are generated. These are dumped in parallel directly to the output queues if non-coherent accumulation is not-active or to the amplitude sub-module if non-coherent accumulation is active.

The coherent accumulator receives a packet of rotated results from the rotator. The packet contains up to eight rotated results. Each rotated result is a 2×13-bit complex (I, Q) signed integer.

The coherent accumulator generates a packet of accumulated results. The packet contains up to eight accumulated results. Each accumulated result is a 2×16-bit complex (I, Q) signed integer. It can also be reduced to a 2×8-bit complex (I, Q) signed integer when written into the output queues.

3.2.9 Amplitude Computation

The amplitude sub-module is bypassed when non-coherent accumulation is not-active.

When non-coherent accumulation is active, input to the amplitude sub-module is the eight results from the coherent accumulation. Each accumulated result is a 2×16-bit complex (I, Q) signed integer.

Output from the amplitude sub-module consists of eight amplitude results that are fed to the non-coherent accumulator. Each amplitude result is a 16-bit scalar unsigned integer.

3.2.10 Non-Coherent Accumulation

Up to eight 16-bit scalar unsigned integer amplitude results from the amplitude computation sub-module are fed to the non-coherent accumulator.

When a non-coherent duration is finished, final results are dumped into the output queues. Each output non-coherent accumulation result is a 16-bit scalar unsigned integer.

3.2.11 Output Queues

Correlation results either from coherent accumulation (2×8-bit complex (I, Q) signed integer) or non-coherent accumulation (16-bit scalar unsigned integer) stages are fed into the output queues.

The output data bus from the queues to the BEI is 128-bit wide.

3.2.12 Mean Value in Post-Processing

This sub-module is in the RAC back-end interface. The mean value is performing the sum of outgoing offsets results for the PM task.

Input is the amplitude 16-bit scalar unsigned integer array.

The output mean value is a 32-bit scalar unsigned integer.

3.3 Finger Despreader

The finger despreader (FD) can use the GCCP in two ways, depending on the spreading factor of the channel:

- For a spreading factor ≥ 32, only up to one symbol is generated per cycle and per iteration period
- For a spreading factor ≤ 16, up to four symbols are generated per cycle

3.3.1 Input Buffer

During each iteration period, the FEI writes up to 54 [streams] × 32 [chip periods] × 2 [samples per chip period] = 3456 samples to the GCCP input buffer. Each sample is a 16-bit complex signed integer (I part takes the lowest eight bits and Q part takes the highest eight bits).

As shown in Figure 1 Input buffer data width is 64-bit.

3.3.2 Multiplexer

The muliplexer takes the 96 samples (each is 16-bit complex) from the IQ input buffer and generates the 77 samples (each is 16-bit complex IQ) needed for the adder trees.

3.3.3 Code Generator

In FD mode, the following code generator sub-blocks are active:

- Long code generator generates gold code scrambling codes
- Short code generator generates gold code scrambling codes
- OVSF code generator generates OVSF channelisation codes
- Pilot bits demodulation uncovers the pilot bit modulation on DPCCH

Data going from the code generator to the adder trees is 32×2 bits wide.

3.3.4 Adder Tree/Correlator

The correlation engine consists of eight parallel independent correlators. During each cycle, the correlators receive one input iteration packet and one code iteration packet. The input iteration packet consists of 32 input chips. Each input chip is a complex signed integer (2×8 bits). The code iteration packet consists of 32 code chips. Each code chip is a complex Boolean (2×1 bits) computed on-line by the code generator.

The adder tree input consists of: 77 antenna samples (each is 16-bit complex IQ) from the multiplexer, a 32-bit I code and a 32-bit Q code from the code generator.

The output of the adder trees consists of 16 I symbols 13-bit wide and 16 Q symbols 13-bit wide going to the interpolator.

3.3.5 Interpolator

In FD mode, for a spreading factor ≥ 32, only one of the 4-tap interpolators is used. For a spreading factor ≤ 16, the four interpolators are active.

Up to four branches of 4-tap complex (I, Q) interpolators each are used in parallel in order to generate up to four interpolated results per cycle. Two of these branches can be summed to create an 8-tap interpolator. Each of these interpolators can be bypassed.

Each interpolator receives a packet of correlation results. The packet contains four results. Each correlation results is a complex (I, Q) signed integer (2×13 bits).

Each interpolator generates one interpolated result. It is a complex (I, Q) signed integer (2×13 bits).

In total, the interpolators receive 16×2×13-bits data input from the adder trees and four sets of filter coefficients (for 4x oversampling case in FD mode) scalar signed 8-bit integer (4×4×8-bit range) coefficients array. They output eight complex 13-bit signed integers (8×2×13-bits range) to the rotator.

3.3.6 Rotator

In FD mode, for a spreading factor ≥ 32, only one rotator is active. For a spreading factor ≤ 16, the four interpolators are connected to four active rotators.

Each rotator branch data input consists of 2×13-bit complex (I, Q) signed integer from the interpolator and 2×8-bit complex (I, Q) signed integer from the phasor.

The output of each branch rotator is a 2×13-bit complex (I, Q) signed integer data going to coherent memory.

3.3.7 Power Computation

The power computation sub-module in SPE, FPE16, and FPE32 shares its multipliers with the rotator. The power computation sub-module receives a packet of correlation results. Correlation results are computed by the interpolators or by the adder trees.

The input packet contains up to four correlation results. Each correlation result is a 2×13-bit complex (I, Q) signed integer.

The power computation sub-module generates one power result. A power result is a scalar 16-bit unsigned integer.

3.3.8 Coherent Accumulation

In FD mode, the coherent accumulation component is used only when the spreading factor ≥ 64.

The coherent accumulator receives a packet of rotated results from the rotator. The packet contains up to eight rotated results. Each rotated result is a 2×13-bit complex (I, Q) signed integer.

The coherent accumulator generates a packet of accumulated results. The packet contains up to eight accumulated results. Each accumulated result is a 2×16-bit complex (I, Q) signed integer. It can also be reduced to a 2×8-bit complex (I, Q) signed integer when written into the output queues.

In FD mode, the symbols are generated at a very high rate and the payload in bytes is minimal. In order to optimize the transfers, symbols are pre-packed in the coherent scratch. This packing mechanism is done for data symbols only. FD control symbols (with SF=256) are not pre-packed, so they are written into the output queues as soon as they are produced.

The packed FD data symbols are filled in the coherent scratch memory to look like a 128-bit word at the output queue input. In 8-bit mode, the 128-bit word contains eight symbols. In 16-bit mode, it contains four symbols.

3.3.9 Amplitude Computation

Amplitude computation is not used in FD mode.

3.3.10 Non-Coherent Accumulation

Non-coherent accumulation is not used in FD mode.

3.3.11 Output Queues

Correlation results from coherent accumulation (2×8-bit complex (I, Q) signed integer) stage are fed into the output queues.

Output data bus from the queues to the back-end interface (BEI) is 128-bit wide.

3.4 Finger Tracking

In finger tracking (FT) mode, the GCCP is used to generate amplitude results on DPCCH fingers. The spreading factor is set to 256. FT can use GCCP in two ways: non-coherent stage is active or not.

3.4.1 Input Buffer

During each iteration period, the front-end interface writes up to 54 [streams] × 32 [chip periods] × 2 [samples per chip period] = 3456 samples to the GCCP input buffer. Each sample is a 16-bit complex signed integer (I part takes the lowest eight bits and Q part takes the highest eight bits).

As shown in Figure 1 Input buffer data width is 64-bit.

3.4.2 Multiplexer

It takes the 96 samples (each is 16-bit complex) from the IQ input buffer and generates the 77 samples (each is 16-bit complex IQ) needed for the adder trees.

3.4.3 Code Generator

In FT mode, only the long code generator sub-block is active. The short code generator, OVSF code generator, and pilot bits demodulation are omitted.

Data going from the code generator to the adder trees is 32-bit I code and 32-bit Q code.

3.4.4 Adder Tree/Correlator

In FT mode, up to all eight correlators are used to feed three 4-tap interpolators. The correlation engine consists of eight parallel independent correlators. During each cycle, each correlator receives one input iteration packet and one code iteration packet. The input iteration packet consists of 32 input chips. Each input chip is a complex signed integer (2×8 bits). The code iteration packet consists of 32 code chips. Each code chip is a complex Boolean (2×1 bits) computed on-line by the code generator.

The adder tree input consists of: 77 antenna samples (each is 16-bit complex IQ) from the multiplexer, a 32-bit I code and a 32-bit Q code from the code generator.

The output of the adder trees consists of 16 I symbols 13-bit wide and 16 Q symbols 13-bit wide going to the interpolator.

3.4.5 Interpolator

In FT mode, three branches of 4-tap complex (I, Q) interpolators each are used in parallel in order to generate three interpolated results per cycle.

Each interpolator receives a packet of correlation results. The packet contains four results. Each correlation results is a complex (I, Q) signed integer (2×13 bits). It also receives three sets of filter coefficients scalar signed 4×8-bit integers.

Each interpolator generates one interpolated result to the rotator. It is a complex (I, Q) signed integer (2×13 bits).

3.4.6 Rotator

In FT mode, three rotators are active in order to generate early-on time-late (EOL) measurements on parallel.

Each rotator branch data input consists of 2×13-bit complex (I, Q) signed integer from interpolator and 2×8-bit complex (I, Q) signed integer from the phasor.

The output of each branch rotator is 2×13-bit complex (I, Q) signed integer data going to coherent memory.

3.4.7 Power Computation

Power computation is not used in FT mode.

3.4.8 Coherent Accumulation

In FT mode, only three coherent accumulators are used to accumulate over several symbols.

The coherent accumulator receives a packet of rotated results from the rotator. The packet contains three rotated results. Each rotated result is a 2×13-bit complex (I, Q) signed integer.

The coherent accumulator generates a packet of accumulated results. The packet contains three accumulated results. Each accumulated result is a 2×16-bit complex (I, Q) signed integer. It can also be reduced to a 2×8-bit complex (I, Q) signed integer when written into the output queues.

If the non-coherent step is not used, once the coherent accumulation is finished, it dumps results directly to the output queues.

3.4.9 Amplitude Computation

The amplitude sub-module is bypassed when non-coherent accumulation is not-active. When the non-coherent stage is used in FT mode, results from coherent accumulation stage are dumped to three components of the amplitude sub-module and converted to amplitude.

Input to the amplitude sub-module is the three results from the coherent accumulation. Each accumulated result is a 2×16-bit complex (I, Q) signed integer.

Output from the amplitude sub-module is three amplitude results that are fed to the non-coherent accumulator. Each amplitude result is a 16-bit scalar unsigned integer.

3.4.10 Non-Coherent Accumulation

If the non-coherent stage is used in FT mode, the amplitude results are accumulated in three of the non-coherent accumulators.

Three 16-bit scalar unsigned integer amplitude results from the amplitude computation sub-module are fed to the non-coherent accumulator.

When a non-coherent duration is finished, three final results are dumped into the output queues. Each output non-coherent accumulation result is a 16-bit scalar unsigned integer.

3.4.11 Output Queues

Correlation results either from coherent accumulation (2×8-bit complex (I, Q) signed integer) or non-coherent accumulation (16-bit scalar unsigned integer) stages are fed into the output queues.

The output data bus from the queues to the BEI is 128-bit wide.

4 Back-End Interface

The primary mission of the back-end sub-module is to push correlation results coming from GCCP data queues to any memory destination inside/outside the DSP.

The BEI is connected to both GCCPs through the output queues. It receives new correlation results with information needed to compute their destination address.

The BEI transfers data by using its own 128-bit master VBUS interface. This interface is connected to memory through the EDMA switch fabric.

4.1 Mean Value in Post-Processing

This sub-module is in the RAC back-end. The mean value is performing the sum of the outgoing offsets results for PM and PD tasks.

Input is the amplitude 16-bit scalar unsigned integer array.

The output mean value is a 32-bit scalar unsigned integer.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265