Application Report
SPRABU0—December 2013

Ethernet Packet Transfer Via Fast C&M Over AIF2

Communications Infrastructure

Abstract

This application report discusses the implementation of Ethernet packet transfer through Fast Control and Management (Fast C&M) over AIF2. Errata documentation describes some restrictions on the hardware design required for Fast C&M over AIF2 and this application report addresses those restrictions.

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1 Introduction

AIF2 specifies two different mechanisms in the CPRI control word portion of the link

- Slow C&M (HDLC): Not supported by AIF2
- Fast C&M (Fast Ethernet): Supported and extended by AIF2 hardware

Fast Ethernet:
Fast Ethernet is Ethernet that is 4B/5B encoded. 4B/5B encoding is the encoding on top of the SerDes 8B/10B encoding. In essence, AIF2 deals with 8B/10B encoding at the PHY layer and 4B/5B encoding at the protocol layer.

Figure 1 Ethernet Frame Structure

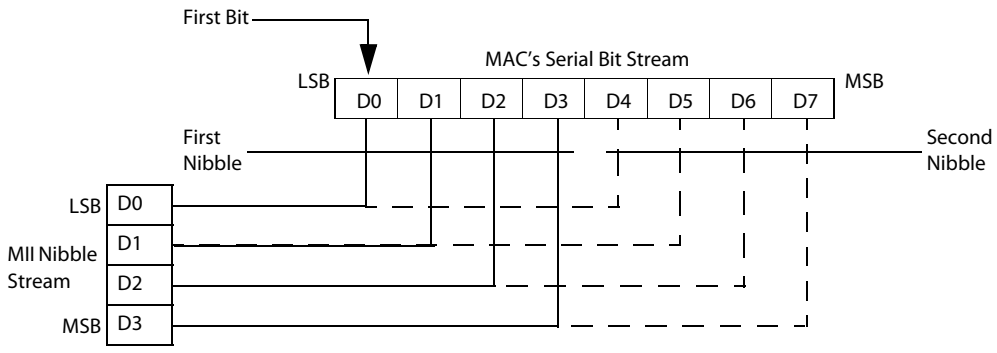
Preamble	Start of Frame	Destination Address	Source Address	Length	Payload	CRC
7 bytes	1 byte	6 bytes	6 bytes	2 bytes	1-1500 bytes	4 bytes

- Preamble: Constant value: 8'b1010_1010
  - Ingress: Stripped off by AIF2
  - Egress: Added by AIF2
- Start of Frame: Constant value: 8'b1010_1011
  - Ingress: Stripped off by AIF2
  - Egress: Added by AIF2
- Length Field: AIF2 does not use or check the length field of Ethernet.
  - Ingress: Ethernet frame is defined by 4B/5B encoding
  - Egress: Packet length is controlled by Multicore Navigator header
- Other Fields: Simply passed by AIF2

The Frame structure above is the Ethernet Frame Structure, this is 4B/5B encoded by the AIF2 and over which the SSD(JK) and ESD(TR) is appended by AIF2 hardware. There are some violations found in the way AIF2 transmits the Control Packet. See the following description for each issue:

1. As per the IEEE 802.3, data has to be transmitted in the following format

Figure 2 Octet/Nibble Transmit and Receive Order



The figure above only shows the 4-bit nibble case (before 4B5B encoding) but AIF2 hardware will convert it to 5-bit nibble by doing 4B/5B encoding but the basic transfer mechanism should be the same. LSB bit within the nibble goes first and LSB nibble (LSB 5 bits) should go as a first nibble. AIF2 hardware natively supports big endian data order and it supports bit level swap within byte before 4B5B encoding or after 4B5B encoding (in the latest revisions of supported devices), but it doesn't support 5-bit nibble level swap for 4B5B encoded data (AIF2 transfers MSB 5-bit nibble first and LSB 5-bit nibble last). This is a violation of the IEEE 802.3 specification.

2. IEEE 802.3 Fast Ethernet spec Start-of-Stream Delimiter chapter states: A Start-of-Stream Delimiter (SSD) is used to delineate the boundary of a data transmission sequence and to authenticate carrier events. On transmission, the first 8 bits of the MAC preamble are replaced by the SSD, a replacement that is reversed on reception. TI AIF2 Protocol encoder does not overwrite the first 8 bits of the MAC preamble. Instead, it appends an 8-bit SSD at the end of preamble and this is a violation of 802.3 spec.

TI proposes the following solutions to overcome this limitation of the AIF2 hardware

1. To make the changes in the FPGA at the RRH so that the FPGA expects the data to be received in the reverse sequence and scans for a 9-Octet preamble, instead of 8-Octet preamble.
2. To implement the 4B5B encoder and decoder in DSP core, i.e. the software implementation of Fast C&M and transmits the data over AIF2 in a Null Delimiter mode.
3. With this approach, the CRC generation/checking feature in AIF2 must also be disabled since there is no way to prevent the CRC calculation over the Ethernet header. SW would need to implement this CRC in addition to the Ethernet header. This should be applied to both Egress and Ingress configuration.

2 Software Implementation

The following section describes the software implementation of the 4B5B encoder and decoder. Consider the following preamble of the following stream at MAC level:

Figure 3 Ethernet Preamble

EtherFrame		4B (LSB First)
Preamble	55h	5
		5
	55h	5
		5
	55h	5
		5
	55h	5
		5
	55h	5
		5
	55h	5
		5
	55h	5
		5
SFD	D5h	5
		D

Data that is been expected to be transmitted is as follows:-

$$\ldots \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{10001}_{K}\ \underbrace{11000}_{J} \rightarrow \text{LSB of J, has to be transmitted first.}$$

The AIF2 hardware in 4B5B mode transfers the data in the following format:

$$\text{MSB of K} \leftarrow \underbrace{11000}_{K}\ \underbrace{10001}_{J}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}\ \underbrace{01011}_{5}$$

To rectify this, we propose the software solution where in DSP core is used to for the 4B to 5B encoding on the egress side, and 5B to 4B decoding on the Ingress side.

2.1 AIF2 Configurations

AIF2 is configured to work in null delimiter mode, with 0xFF as the null delimiter. The reason for selecting the character “0xFF” as the null delimiter is, because the 5B character “11111” is the idle character (CPRI spec).

Hence on the transmit side once the SSD(TR) characters inserted into the Ethernet stream, AIF2 hardware appends the Null delimiter out side of the packet and transmits the packet. Essentially forming a packet like:

Figure 4 AIF2 output frame Structure

NULL Delimiter	Preamble	Start of Frame	Destination Mac Address	Source Mac Address	Length	Payload	CRC	ESD	NULL Delimiter
0xFF	10 Bits SSD(JK) 60 Bits Preamble	1*10 Bits	6*10 Bits	6*10 Bits	20 Bits	(1-1500)*10 Bits	4*10 Bits	10 Bits (TR)	0xFF

To configure AIF2 in Null Delimiter mode the PdLinkSetup and PeLinkSetup configurations has to be as follows

```
PdLinkSetup.bEnablePdLink = TRUE;
      PdLinkSetup.CpriEnetStrip = 0x0;//Disable ethernet strip
      PdLinkSetup.Crc8Poly = CRC8_POLY;
      PdLinkSetup.Crc8Seed = CRC8_SEED;
      PdLinkSetup.CpriCwNullDelimitor = 0xFF;
      PdLinkSetup.CpriCwPktDelimitor[0] = CSL_AIF2_CW_DELIM_NULLDELM;
      PdLinkSetup.PdCpriCrcType[0] = CSL_AIF2_CRC_32BIT;
      PdLinkSetup.bEnableCpriCrc[0] = FALSE;//disable CPRI CRC
PdLinkSetup.PdPackDmaCh[0] = 124;//Set DB channel 124 as a dma ch for control channel
0. it doesn't need to be 124
PdLinkSetup.bEnablePack[0] = TRUE;//disable CPRI control channel 0 packing
PeLinkSetup.CpriCwNullDelimitor = 0xFF;//Idle character
      PeLinkSetup.CpriCwPktDelimitor[0] = CSL_AIF2_CW_DELIM_NULLDELM;
      PeLinkSetup.PePackDmaCh[0] = 124;
PeLinkSetup.bEnablePack[0] = TRUE;
```

2.2 TX 4B 5B Encoder

On the egress side before the ethernet data is being pushed to the Transmit queue, a 4B to 5B encoder function should be called. The 4B5B encoder kernel expects the data, in the following format:-

Figure 5 Ethernet frame Structure

Preamble	Start of Frame	Destination Address	Source Address	Length	Payload	CRC
7 bytes	1 byte	6 bytes	6 bytes	2 bytes	1-1500 bytes	4 bytes

Generally used preamble for the Ethernet frame: 0x55, 0x55, 0x55, 0x55, 0x55, 0x55, 0x55, 0x55 and the Start of Frame is 0xD5.

The 4B5B encoder does the following data manipulation to the input stream sent to it:-

- Each 4Bit Nibble is converted into a 5Bit Nibble.
- Insert SSD i.e JK into the first symbol location of the Preamble
- Append the ESD(TR) at the END of the stream after the CRC.

To form a packet as per the Fast C&M specification.

Figure 6 4B5B output frame Structure

Preamble	Start of Frame	Destination Mac Address	Source Mac Address	Length	Payload	CRC	ESD
10 Bits SSD(JK) 60 Bits Preamble	1*10 Bits	6*10 Bits	6*10 Bits	20 Bits	(1-1500)*10 Bits	4*10 Bits	10 Bits (TR)

The 4B5B encoder function kernel is implemented using the lookup table approach, each 4Bit Nibble is used as an Index in the Lookup table and corresponding 5-bit-encoded value is loaded using the following table.

Table 1 Fast Ethernet 4B/5B Encoding

Name	4b	5b	Description
0	0000	11110	hex data 0
1	0001	01001	hex data 1
2	0010	10100	hex data 2
3	0011	10101	hex data 3
4	0100	01010	hex data 4
5	0101	01011	hex data 5
6	0110	01110	hex data 6
7	0111	01111	hex data 7
8	1000	10010	hex data 8
9	1001	10011	hex data 9
A	1010	10110	hex data A
B	1011	10111	hex data B
C	1100	11010	hex data C
D	1101	11011	hex data D
E	1110	11100	hex data E
F	1111	11101	hex data F
I	-NONE-	11111	Idle
J	-NONE-	11000	SSD part1
K	-NONE-	10001	SSD part2
T	-NONE-	01101	ESD part1
R	-NONE-	00111	ESD part2
H	-NONE-	00100	Halt
End of Table 1			

2.3 RX 5B 4B Decoder

On the Ingress side, when the packets are received software needs to scan for the Start of Frame SSD and the end of frame ESD and then send the received packet to the decoder.

On the Rx side, there could be multiple fragmented packets received for the single packet sent from the Remote Radio head. This situation arises of whenever there a byte “0xFF” in the 5B encoded data on the Rx side.

Since AIF2 is configured to work in Null Delimiter mode with “0xFF” as the Null Delimiter, the AIF2 hardware fragments the incoming packet into multiple packets at each 0xFF boundary. The application software provided part of the example with this application report, scans for such scenarios and reforms the original packet by merging the multiple packets into a single packet and sends it to the decoder for further processing.

Consider the hypothetical case, of data being transmitted from the RRH to the Baseband board:

SSD	0x1	0x2	0x3	0x4	..	..	..	0xFF	0x10	0x11	..	..	..	..	0xFF	0x20	0x21	..	ESD

When such a packet is received at the AIF2, AIF2 segments it into 3 fragments as shown below:

SSD	0x1	0x2	0x3	0x4	..	..	..

0x10	0x11	..	..	..	..

0x20	0x21	..	ESD

The application must scan for the SSD and stitches all the packets into a single packet till it finds ESD. Once the SSD and ESD are detected and validated the packet is further sent to a 5B to 4B decoder which decodes the RX packet and forms a Ethernet packet for further processing at the MAC Layer.

3 Abbreviation

Abbreviation	Description
AIF2	Antenna Interface 2
C&M	Control and Management
CPRI	Common Public Radio Interface
ESD	End of Stream Delimiter
FPGA	Field Programmable Gate Array
LSB	Least Significant Bit
MAC	Media Access Control
MSB	Most Significant Bit
OBSAI	Open Base Station Architecture Initiative
RP3	RP3 Reference point 3 (OBSAI)
RRH	remote Radio Head
SSD	Start-of-Stream Delimiter, from IEEE 802.3 Fast Ethernet spec

4 References

- AIF2 users guide :
  http://www.ti.com/lit/pdf/sprugv7
- CPRI specification 4.0
- Device-specific errata document

5 Revision History

The following table lists changes for each revision.

Revision	Date	Description
SPRABU0	December 2013	Initial Publication

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