Product Bulletin

H.263 Encoder and Decoder Software for TMS320C64x™ DSP-Based Processors

Key Benefits

- Provides optimal flexibility and performance on C64x™ DSP-based processors
- Includes complete easy-to-use algorithm documentation for quick time-to-market
- Reduces cost-of-creation, optimization, testing and implementation associated with developing your own software
- Allows customer resources to be spent on differentiating video solutions

Overview

Texas Instruments' H.263 Encoder and Decoder software provides developers with tried and tested algorithms designed exclusively for TI's C64x DSP-based processors. These algorithms are easily integrated into designs and alleviate the need to write and debug software, reducing time-to-market.

TI's C64x DSPs and TMS320DM64x™ DSP-based digital media processors combined with H.263 Encoder and Decoder software provide a complete solution. This solution enables flexible video encoding compression by removing spatial redundancies that exist within the frames and the temporal redundancies that exist between successive frames. The finished product is high-quality pictures at low-bit rates.

The H.263 Standard

Thanks to its superior quality, H.263 is the dominant coding standard in video communication and has been adopted in several network transport standards such as ITU-T H.324 (PSTN), H.320 (ISDN), H.310 (BISDN), H.323 and 3GPP.

Key Features

Encoder

- D1 encoding at approximately 50% CPU loading
- Supports SQCIF, QCIF, CIF and 4CIF formats
- Configurable minimum and maximum quantization values for P frames
- Satisfies the minimal requirement defined in the ITU-T H.263 specification
- Complies with H.263 baseline profile
- No implementation of annexes
- Code tested extensively on C64x DSP-based processors
- Hooks allowing use of Real-time Transfer Protocol are partially in place. Structure to store necessary information is defined and can be allocated with appropriate flags at build-time, but no code has been implemented
- Structured to provide as much flexibility as possible, so software can run under different system configurations

Decoder

- D1 decoding at approximately 16% CPU loading
- Configurable rate control
- 4:2:0 coded video format
- Support for custom resolution is possible by minor code modification (generated bit stream will not be compliant with the H.263 simple profile standard)
- Number of macroblocks to be processed in a loop is configurable–optimize performance with available memory resources
- Operates in Little Endian mode
- 4CIF and D1 resolution encoding can be done with appropriate configuration
- Every VLD function is equipped with error detection capabilities; when an error code in a

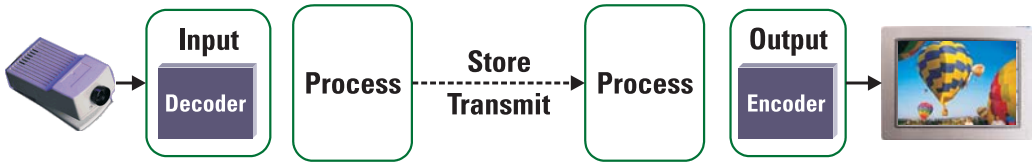

Figure 1. Decoder and Encoder Process

bitstream is detected, the decoder will exit with an appropriate error code to indicate the error location

Get Started Today

- Free 60-day evaluation period with four hours support provided by TI Third Party Authorized Software Providers. For more information, contact your local TI sales representative
- Purchase a Digital Media Development Kit (DMDK) at the DSP eStore – **www.dspestore.com**

Summary of Performance

Configuration ID Table (Encoder and Decoder)

Usage Conditions	Configuration ID
704×576, 25 fps, YUV420, bit rate = 4 Mbps	4CIF
720×480, 30 fps, YUV420, bit rate = 4 Mbps	D1 (Custom resolution)
352×288, 30 fps, YUV420, bit rate = 4 Mbps	CIF
176×144, 30 fps, YUV420, bit rate = 4 Mbps	QCIF
128×96, 30 fps, YUV420, bit rate = 512 kbps	SQCIF

Cycle Performance in Megacycles per Second for TMS320DM642 Digital Media Processors for Specified H.263 Test Parameters

Configuration ID	Encoder Test File Parameters	Performance Statistics (In Megacycles/Second)
		Average
4CIF	Calendar and train sequence	339
D1	Fire sequence	294
D1	Gi sequence	342
CIF	Foreman sequence	96
QCIF	Foreman sequence	24
QCIF	Akiyo sequence	20
Configuration ID	**Decoder Test File Parameters**	**Performance Statistics (In Megacycles/Second)**
		Average
4CIF	Coastguard sequence, 9669 kbps	107.5
D1	Fire sequence, 5618 kbps	95.5
CIF	Silent sequence, 238 kbps	12.7
CIF	Foreman sequence, 652 kbps	22.3
QCIF	Foreman sequence, 190 kbps	5.5
QCIF	News sequence, 110 kbps	3.4
QCIF	Coastguard sequence, 187 kbps	5.5

Profiled on the TMS320DM642 EVM using silicon revision 1.1 running at 600 MHz using Code Composer Studio™ IDE version 2.2.18

Memory Statistics – Generated with Code Generation Tools included in Code Composer Studio™ IDE 2.2

Configuration	Encoder Memory Statistics[1]				Decoder Memory Statistics[4]			
	Program Memory	Data Memory			Program Memory	Data Memory		
		Internal	External	Stack		Internal	External	Stack
4CIF	76	29	1200[2]	20	29	92	1200	1.2
D1	76	35[3]	1200	20	29	94[5]	1200	1.2
CIF	76	26	300	20	29	47	300	1.2
QCIF	76	26	300	20	29	47	300	1.2
SQCIF	76	26	300	20	29	47	300	1.2

[1] *All memory requirements are expressed in KB (1 KB = 1024 Bytes, 1 Byte = 8 bits). All are memory requirements for nmb2proc = 11.*
[2] *Does not include buffer to store generated bit stream.*
[3] *This is with nmb2proc = 15, hence memory requirements are higher.*
[4] *All memory requirements are expressed in KB. All are memory requirements for processing one row of macroblocks in a loop.*
[5] *Higher requirements due to 45 macroblocks in a row.*
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