Technical Brief
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A Technical Introduction to the TMS320F28004x Microcontroller

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ABSTRACT

While many real-time control systems require a high-performance microcontroller (MCU), the tradeoffs of balancing performance and cost can be challenging. To this end, Texas Instruments developed the Piccolo™ TMS320F28004x MCU device series. This document discusses the technical details of the TMS320F28004x architecture and highlights the new improvements to various key peripherals, such as an enhanced Type-2 CLA capable of running a background task, and the inclusion of a set of high-speed programmable gain amplifiers. Also, a completely new boot mode flow enables expanded booting options. Where applicable, a comparison to the Piccolo TMS320F2807x MCU device series is used, and some knowledge about the previous device architectures is helpful in understanding the topics discussed in this document.

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1 Introduction

Many real-time control systems require a high-performance microcontroller (MCU) for cost-sensitive applications. However, it can be a challenge to optimize these two parameters – performance and cost. To meet this challenge, the Texas Instruments Piccolo™ TMS320F28004x MCU device series, referred to as the F28004x in this document, was developed. This MCU incorporates critical control peripherals, analog components, communications peripherals, and nonvolatile memory in a single device. This level of integration provides a cohesive real-time control solution; increasing system performance and reliability while simplifying the board layout which reduces the overall system cost. The purpose of this document is to highlight the various key enhancements to the architecture and peripherals which are new to the F28004x. Where appropriate, a comparison to the Piccolo TMS320F2807x MCU device series, referred to as the F2807x in this document, is used. Therefore, some working knowledge about the previous C2000™ MCU device architectures are helpful in understanding the topics presented in this document.

2 Processor and Accelerators

The F28004x CPU is based on the TI 32-bit C28x fixed-point accumulator-based architecture and it is capable of operating at a clock frequency of up to 100 MHz. The CPU is tightly coupled with a Floating-Point Unit (FPU) which enables support for hardware IEEE-754 single-precision floating-point format operations. Also, a tightly coupled Trigonometric Math Unit (TMU) extends the capability of the CPU to efficiently execute trigonometric and arithmetic operations commonly found in control system applications. Similar to the FPU, the TMU provides hardware support for IEEE-754 single-precision floating-point operations which accelerate trigonometric math functions. A Viterbi, Complex Math, and CRC Unit (VCU) further extends the capabilities of the CPU for supporting various communication-based algorithms and is very useful for general-purpose signal processing applications, such as filtering and spectral analysis. The F28004x utilizes a VCU-I (Type 1) rather than the VCU-II (Type 2) since the additional instructions on the VCU-II are not necessary to support the functions needed for the F28004x class applications. (A “Type” change represents a major functional feature difference in a peripheral module).

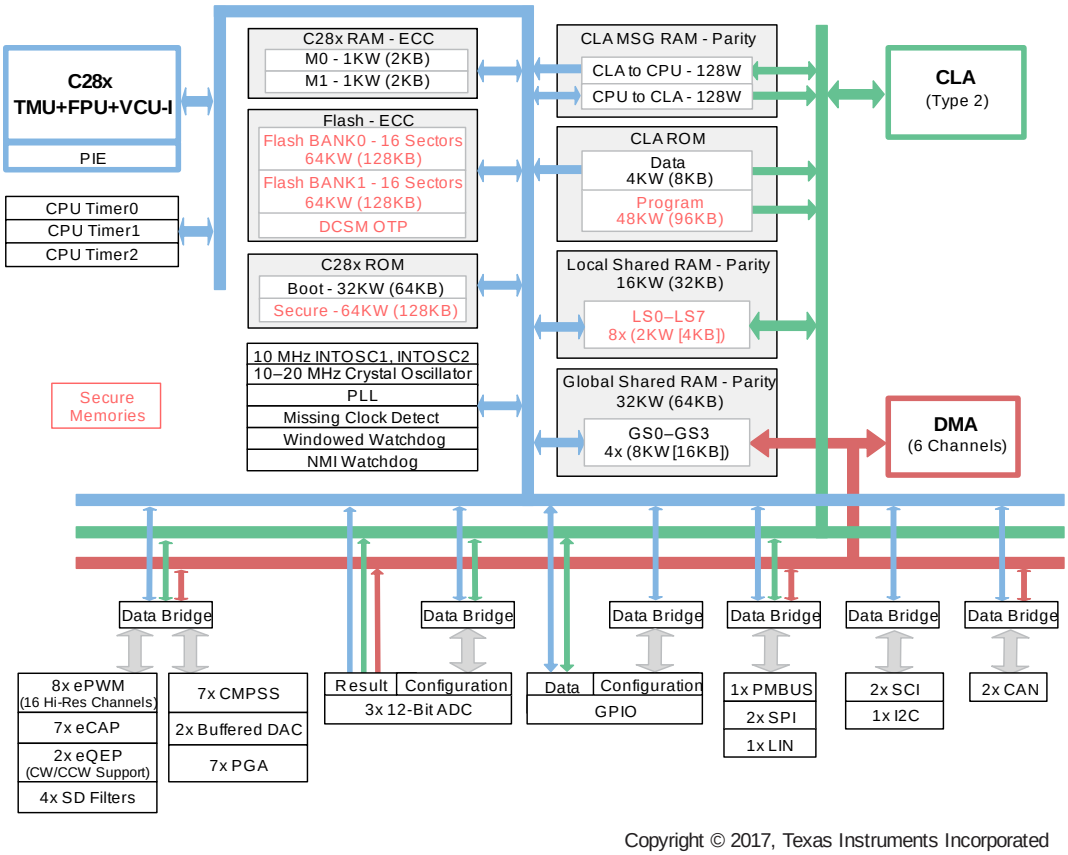

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Figure 1. F28004x Functional Block Diagram

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The Control Law Accelerator (CLA) is an independent 32-bit floating-point math hardware accelerator which executes real-time control algorithms in parallel with the main C28x CPU, effectively doubling the computational performance. With direct access to the various control and communication peripherals, the CLA minimizes latency, enables a fast trigger response, and avoids CPU overhead. Also, with direct access to the ADC results registers, the CLA is able to read the result on the same cycle that the ADC sample conversion is completed, providing “just-in-time” reading, which reduces the sample to output delay.

The F28004x features a new Type 2 CLA which has the option of running the lowest priority task (Task 8) as a background task. Once triggered, it runs continuously until it is terminated or reset by the CLA or MCU. The remaining tasks (Task 1 through Task 7, in priority order) can interrupt the background task when they are triggered. If needed, portions of the background task can be made uninterruptible. Some uses of the background task include running continuous functions, such as communications and clean-up routines. The background task is enabled by setting the BGEN bit in the MCTRLBGRND register. The Task 8 interrupt vector is then loaded from the MVECTBGRND register rather than the MVECT8 register. When the background task is interrupted, the branch return address is saved to the MVECTBGRNDACTIVE register, and the address is then loaded back to the MPC when execution continues.

3 Memory

The F28004x utilizes a memory map where the unified memory blocks can be accessed in either program space, data space, or both spaces. This type of memory map lends itself well for supporting high-level programming languages. The memory map structure consists of RAM blocks dedicated to the CPU, RAM blocks accessible by the CPU and CLA, RAM blocks accessible by the DMA module, message RAM blocks between the CPU and CLA, CAN message RAM blocks, Flash, and one-time programmable (OTP) memory. The F28004x memory map is similar to the F2807x with some minor modifications, as described below.

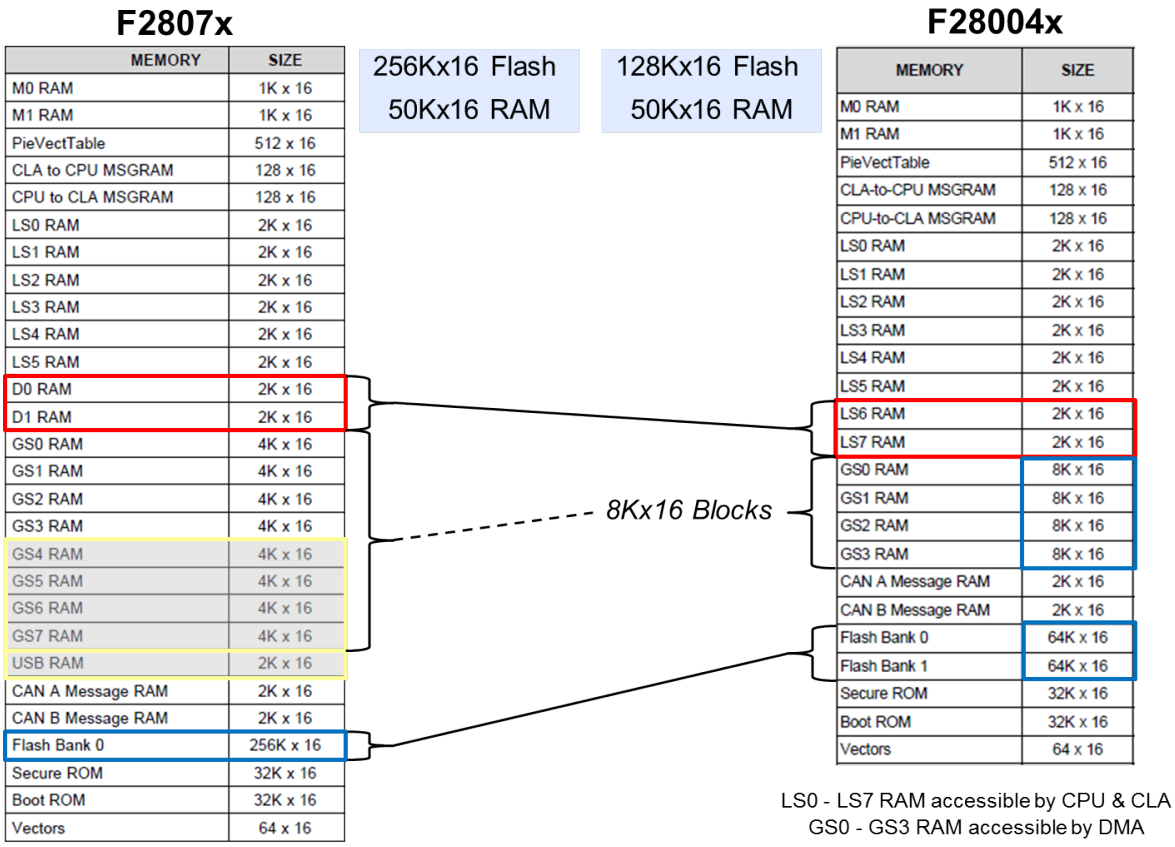

Figure 2. F28004x and F2807x Memory Map Comparison

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Memory blocks M0 and M1 have a size of 2KB (1Kx16) each, and include Error-Correcting Code (ECC) protection. These memory blocks are tightly coupled with the CPU, where only the CPU has access to them.

The F28004x eight local shared RAM blocks named LS0 through LS7 have a size of 4KB (2Kx16) each, and are accessible by the CPU and CLA. The LSx RAM blocks have parity and access protection, and can be secured. By default, the LSx RAM blocks are assigned to the CPU only, however each block can be allocated to the CPU and CLA by configuring the appropriate bit in the LSx Memory Selection register. When allocated to the CLA, each LSx RAM block can then be configured as either CLA program memory or CLA data memory. Compared with the F2807x memory map, the D0 and D1 RAM blocks are classified as LS6 and LS7 RAM blocks, and are located at the same memory addresses. This provides additional memory which can be allocated to the CLA.

The F28004x four global shared RAM blocks named GS0 through GS3 have a size of 16KB (8Kx16) each, and are accessible by the DMA module. The GSx RAM blocks have parity and access protection. Compared with the F2807x memory map, the eight GSx RAM blocks are combined into four GSx RAM blocks, occupying the same memory size and starting at the same memory address.

The CLA message RAM blocks are used to share data between the CPU and CLA. There is a dedicated CLA message RAM block for “CPU to CLA” and another dedicated CLA message RAM block for “CLA to CPU”. By using one-way message RAMs the CLA can read the “CPU to CLA” message RAM while the CPU is writing to it with no arbitration or stalls, and vice versa. The CLA message RAM blocks have a size of 256B (128x16) each, and have parity and access protection. The CLA has write access to the “CLA to CPU” message RAM block, and the CPU has write access to the “CPU to CLA” message RAM block. The CPU and CLA have read access to both CLA message RAM blocks.

The F28004x contains 256KB (128Kx16) of flash divided equally into two banks (bank 0 and bank 1). By using two banks, the user can program one bank while operating out of the other bank. Then as needed, the application can switch to the newly programmed bank. The flash is primarily used to store program code, but can also be used to store static data. The flash sectors have ECC protection providing Single-Error Correction and Double-Error Detection (SECDED), and each sector can be secured. Compared to the F2807x with 512KB (256Kx16) of flash operating with 2 wait-states at a maximum frequency of 120 MHz, the F28004x has 256KB (128Kx16) and operates at 4 wait-states at a maximum frequency of 100 MHz. However, by utilizing a 128-bit code pre-fetch mechanism and data cache, optimal system performance can be achieved. The F28004x has an average flash performance efficiency of about 84% compared to about 92% for the F2807x. The F28004x flash is optimized for lower cost and lower power consumption.

The F28004x contains two types of OTP memory blocks: TI-OTP and USER-OTP. The TI-OTP contains device specific calibration data for the ADCs, internal oscillators, programmable gain amplifiers, and buffered DACs, in addition to settings used by the flash state machine for erase and program operations. The USER-OTP contains locations for programming security settings, such as passwords for selectively securing memory blocks, configuring the standalone boot process, as well as selecting the boot-mode pins. This information is programmed into the dual code security module (DCSM).

The DCSM offers protection for two zones (zone-1 and zone-2), and is intended to block access and visibility to the various on-chip memory resources with the purpose of preventing duplication and reverse engineering of proprietary code. The options for both zones are identical, and each memory resource can be assigned to either zone. Either zone can protect each sector of flash individually, and each LSx memory block individually.

Each zone is secured by its own 128-bit (four 32-bit words) user defined CSM password, which is stored in its dedicated OTP location based on a zone-specific link pointer. The user accessible CSMKEY registers are used to secure and unsecure the device, and a new or un-programmed device will be unlocked by default. Each zone’s dedicated OTP block contains its security configuration settings, such as the CSM passwords, and the allocations for securing the LSx RAM blocks and flash sectors. Since the OTP cannot be erased, flexibility is provided by using a link pointer to select the location of the active zone region within the OTP block, allowing the user to make multiple modifications to the configuration up to thirty times. This is accomplished by exploiting the fact that each bit in the OTP can be programmed one bit at a time, and a “1” can be programmed to a “0”, but not erased back to a “1”. The most significant bit position in the link pointer that is programmed to a “0” defines the valid offset base address for the active zone region within the OTP block.

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4 Boot Modes

When the MCU is powered-on, and each time the MCU is reset, the internal bootloader software located in the boot ROM is executed. The boot ROM contains bootloading routines and execution entry points into specific on-chip memory blocks. This initial software program is used to load an application to the device RAM through the various bootable peripherals, or it can be configured to start an application located in flash. The F28004x is extremely flexible in its ability to use alternate, reduce, or completely eliminate boot mode selection pins by programming a BOOTPIN_CONFIG register.

After the MCU is powered-up or reset, the peripheral interrupt expansion block, also known as the PIE block, and the master interrupt switch INTM are disabled. This prevents any interrupts during the boot process. The program counter is set to 0x3FFFC0, where the reset vector is fetched. Execution then continues in the boot ROM at the code section named InitBoot. If the emulator is connected, then the boot process follows the Emulation Boot mode flow. In Emulation Boot mode, the boot is determined by the EMU-BOOTPIN-CONFIG and EMU-BOOTDEF-LOW/HIGH registers located in the PIE RAM. If the emulator is not connected, the boot process follows the Stand-alone Boot mode flow. In Stand-alone Boot mode, the boot is determined by two GPIO pins or the Z1-OTP-BOOTPIN-CONFIG and Z1-OTP-BOOTDEF-HIGH/LOW registers located in the DCSM OTP.

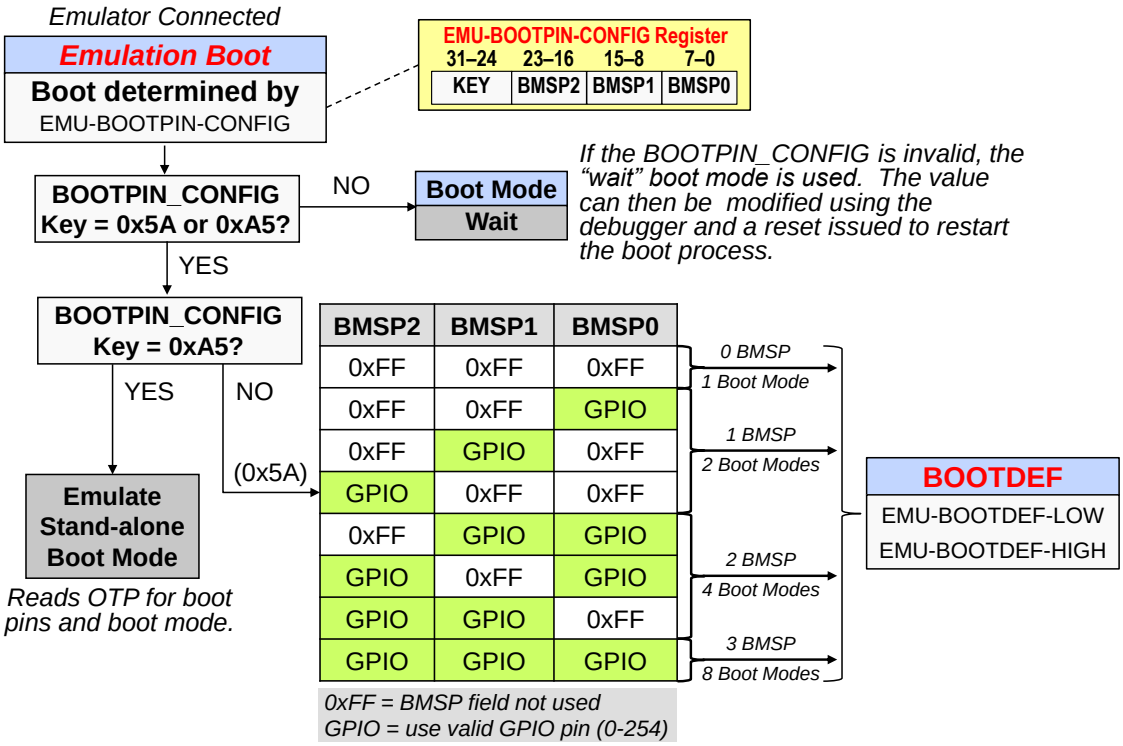

Figure 3. Emulation Boot Mode

In Emulation Boot mode, first the KEY value located in the EMU-BOOTPIN-CONFIG register (bit fields 31-24) is checked for a value of 0x5A or 0xA5. If the KEY value is not 0x5A or 0xA5, the "wait" boot mode is entered. The KEY value and the Boot Mode Selection Pin values (BMSP2-0, bit fields 23-0) can then be modified using the debugger and a reset is issued to restart the boot process. This is the typical sequence followed during device power-up with the emulator connected, allowing the user to control the boot process using the debugger.

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Once the EMU-BOOTPIN-CONFIG register is configured and a reset is issued, the KEY value is checked again. If the KEY value is set to 0xA5 the Stand-alone Boot mode is emulated and the Z1-OTP-BOOTPIN-CONFIG register is read for the boot pins and boot mode. Otherwise, the KEY value is set to 0x5A and the boot mode is determined by the BMSP bit field values in the EMU-BOOTPIN-CONFIG register and the EMU-BOOTDEF-LOW/HIGH registers. The EMU-BOOTPIN-CONFIG register contains three BMSP bit fields. If the BMSP bit field is set to 0xFF, then the bit field is not used. Therefore, the boot modes can be set by zero, one, two, or three BMSP bit fields. This provides one, two, four, or eight boot mode options, respectively. Details about the BOOTDEF options will be discussed after the Stand-alone Boot mode is covered.

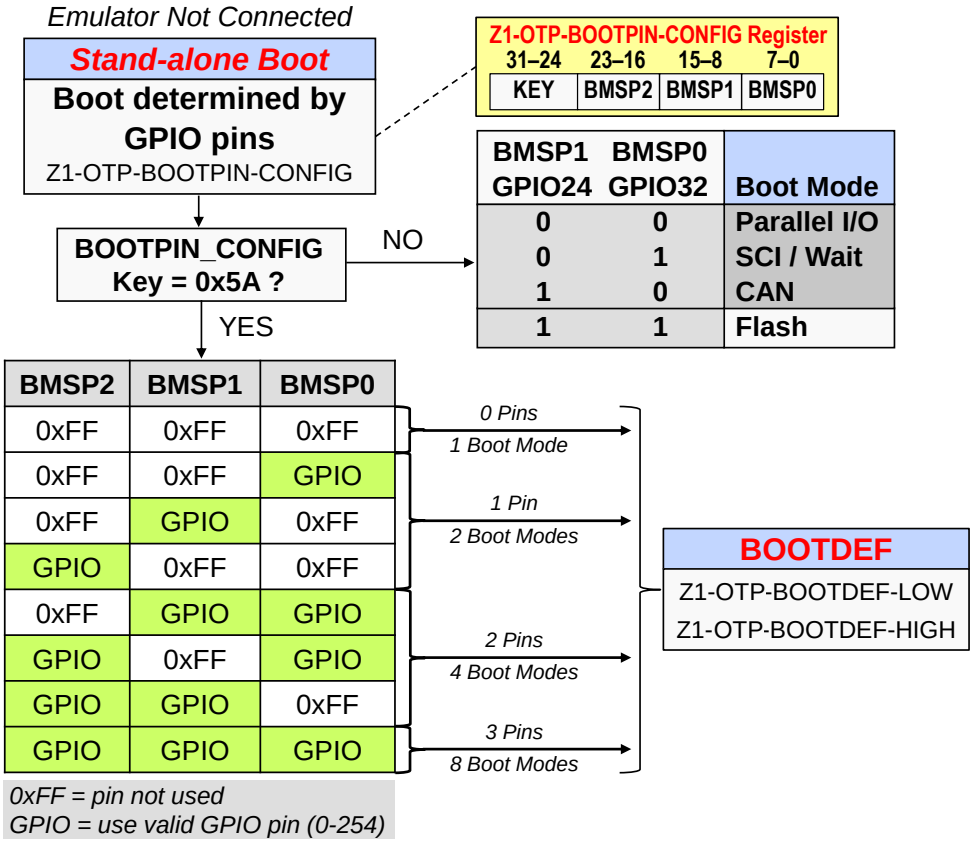

Figure 4. Stand-Alone Boot Mode

In Stand-Alone Boot mode, if the KEY value located in the Z1-OTP-BOOTPIN-CONFIG register (bit fields 31-24) is not 0x5A, the boot mode is determined by the default GPIO24 and GPIO32 pins. These two pins provide four boot options – Parallel I/O, SCI/Wait, CAN or Flash. If the KEY value is 0x5A the boot mode is determined by the BMSP bit field values in the Z1-OTP-BOOTPIN-CONFIG and the OTP-BOOTDEF-LOW/HIGH registers. The Z1-OTP-BOOTPIN-CONFIG register contains three BMSP bit fields. If the BMSP bit field is set to 0xFF, then the GPIO pin is not used. Therefore, the boot modes can be set by zero, one, two, or three GPIO pins. This provides one, two, four, or eight boot mode options, respectively.

The BOOTDEF options described here applies to both the EMU-BOOTDEF-LOW/HIGH registers used in Emulation Boot mode and the Z1-OTP-BOOTDEF-LOW/HIGH registers used in Stand-alone Boot mode. The BOOTDEF-LOW/HIGH registers consist of eight separate bit fields named BOOT_DEF0 through BOOT-DEF7. These bit fields correspond to the one, two, four, or eight boot mode options that are selected by the zero, one, two, or three BMSP bit fields/GPIO pins, respectively in the BOOTPIN_CONFIG register. Therefore, if zero BMSP bit fields/GPIO pins are selected, then only the BOOT_DEF0 bit field in the BOOTDEF-LOW/HIGH registers is used. Likewise, if three BMSP bit fields/GPIO pins are selected, then BOOT_DEF0 through BOOT_DEF7 in the BOOTDEF-LOW/HIGH registers is used.

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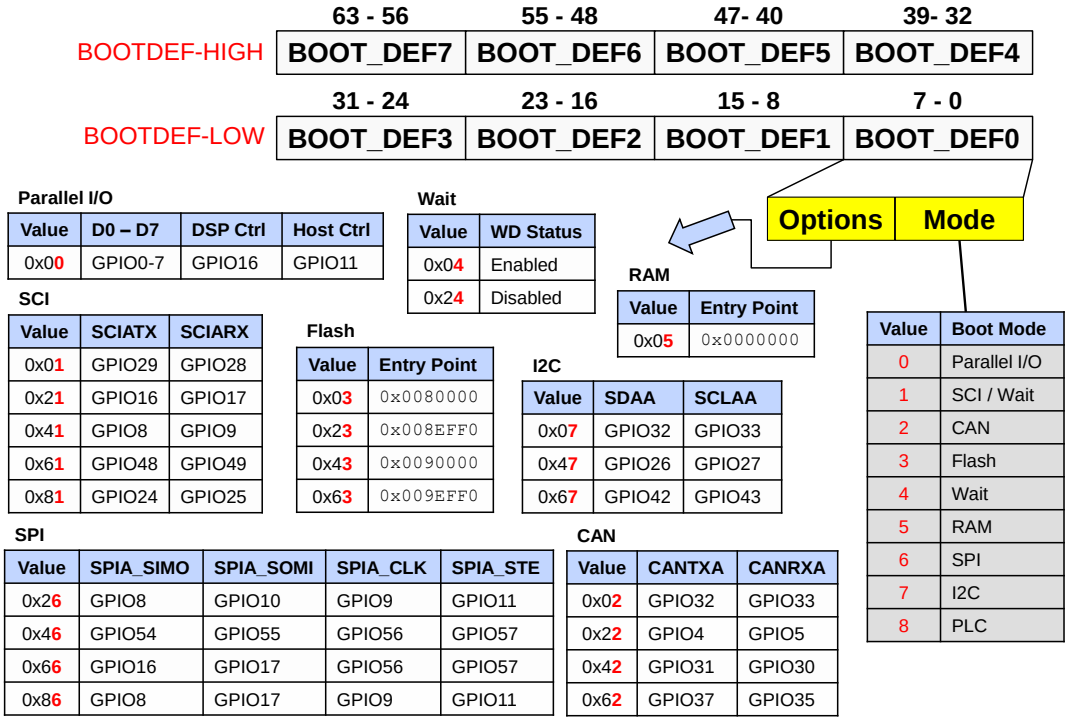

Figure 5. Boot Mode Definitions

The value in the BOOT_DEF bit fields determines which peripheral is used for bootloading or the entry point that is used for code execution. In the BOOT_DEF bit field the lower bits define the boot mode used and the upper bits define the options for that bit mode. Utilizing this type of booting technique provides flexibility for selecting multiple boot modes, as well as reducing the number of boot mode pins.

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5 System

The watchdog timer module on the F28004x now includes a WDCLK divider in addition to the watchdog prescaler. Using the WDCLK divider, the WDCLK derived from INTOSC1 can be divided by 2 to 4096 in powers of 2. This, along with the watchdog prescaler, provides a very wide range of timeout values for safety-critical applications. The WDCLK divider defaults to divide by 512 for backwards compatibility. Previously on the F2807x and earlier devices the WDCLK divider was fixed at divide by 512.

The F28004x has three options for supplying the required 1.2 V to the core (VDD): an external supply, the internal 1.2 V low dropout (LDO) voltage regulator (VREG), or the internal 1.2 V switching regulator (DC-DC). The internal DC-DC regulator provides increased efficiency over the LDO for converting 3.3 V to 1.2 V, however using the internal DC-DC regulator requires additional external components. By default the DC-DC regulator is disabled. To use this supply, the MCU must power up initially with the internal LDO VREG and then transition to the internal DC-DC regulator using the application software.

The architecture makes use of three crossbars (X-BARs) to provide a flexible means for interconnecting multiple inputs, outputs, and internal resources in various configurations. The Input X-BAR is used to route external GPIO signals into the device. With access to every GPIO pin, each signal can be routed to any or multiple destinations which include the ADCs, eCAPs, ePWMs, Output X-BAR, and external interrupts. Enhancements to the F28004x Input X-BAR include the addition of two more inputs (INPUT15 and INPUT16) and any of the sixteen inputs can be selected as an input to each eCAP module. On the F2807x INPUT7 through INPUT12 are fixed as inputs to eCAP1 through eCAP6, respectively. Also, the F28004x Input X-BAR has a default reset value of “1” for each input which is driven to the destinations, whereas the F2807x uses the state of the GPIO0 pin for the value. The Output X-BAR is used to route various internal signals out of the device through the GPIO pins, and the ePWM X-BAR is used to route signals to each ePWM Digital Compare submodule for actions such as trip zones and synchronizing. For the F28004x, both the Output X-BAR and ePWM X-BAR now include a CLAHALT signal. The ePWM X-BAR also has the addition of signals INPUT7 through INPUT14 from the Input X-BAR.

The F28004x supports three clock-gating low-power modes – Idle, Standby, and Halt. The Hibernate low-power mode found on the F2807x is not supported. New on the F28004x is the ability to power-down the external clock source XTAL by software at any time.

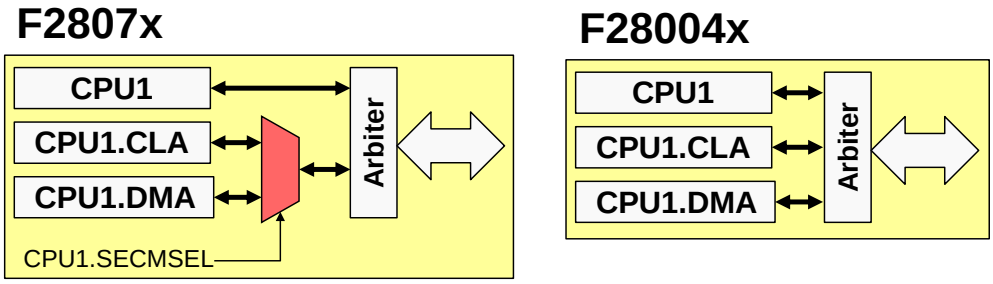

Figure 6. CPU/CLA/DMA Peripheral Access

An enhancement to the F28004x peripheral architecture is the capability for the CLA and DMA to have simultaneous access with arbitration. This allows the CPU, CLA, and DMA to have access without interference, which enables the CLA to utilize DMA transfers. The F2807x uses a common peripheral architecture and the SECMSEL register is used to select whether the dual ported bridge is connected with the CLA or DMA as the secondary master (the CPU is always connected as the primary master).

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6 Analog Peripherals

Analog peripherals are a critical component in many real-time control systems. They are used to sense signals for the feedback control loops, as well as for hardware protection. By integrating the analog peripherals on-chip, cost and design efforts can be reduced. For this reason, the F28004x incorporates on-chip analog-to-digital converters (ADCs), buffered digital-to-analog converters (DACs), programmable gain amplifiers (PGAs), and comparator subsystems (CMPSS). Newly introduced on the F28004x is an analog subsystem interconnect which enables a very flexible pin usage, allowing for smaller device packages. The DAC outputs, CMPSS inputs, PGA functions, and digital inputs are multiplexed with the ADC inputs. This type of interconnect permits a single pin to route a signal to multiple analog modules. The analog pins are organized into analog groups around a PGA and CMPSS module, and the routing is defined in an analog pin and internal connections table.

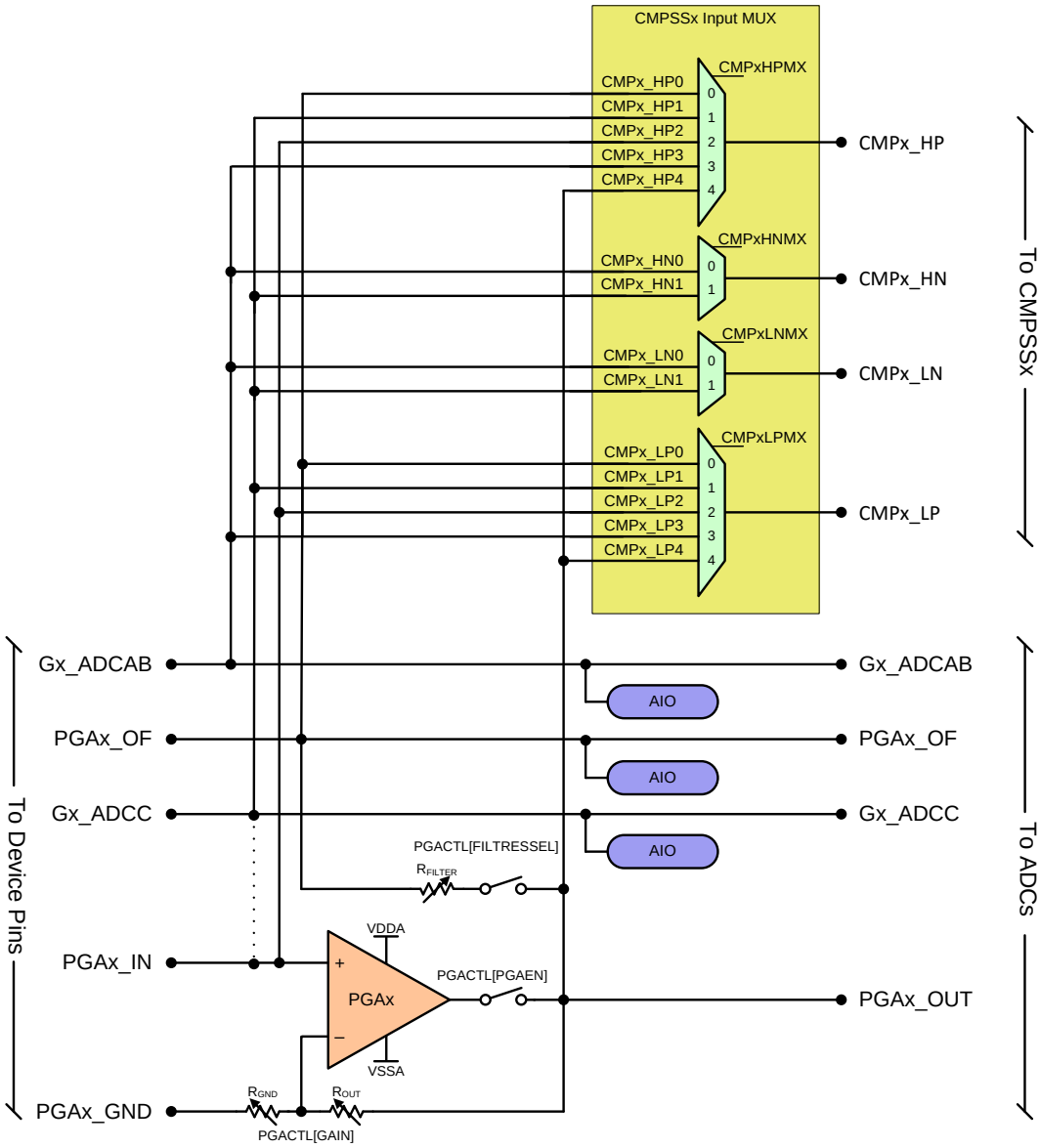

Figure 7. Analog Group Connections

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The PGA amplifies small input signals to increase the dynamic range for the downstream ADC and CMPSS modules. The PGA has four programmable gain modes (3x, 6x, 12x, and 24x) and support for low-pass filtering using an external capacitor, making it adaptable to various performance needs. The filtered signal is available for sampling and monitoring by the ADC and CMPSS modules. The F28004x has up to seven PGA modules.

The CMPSS modules are useful for supporting applications such as peak current mode control, switched-mode power, power factor correction, and voltage trip monitoring. The module is designed around a pair of analog comparators which generates a digital output indicating if the voltage on the positive input is greater than the voltage on the negative input. The positive input to the comparator is always driven from an external pin. The negative input can be driven by either an external pin or an internal programmable 12-bit digital-to-analog (DAC) as a reference voltage. Values written to the DAC can take effect immediately or be synchronized with ePWM events. A falling-ramp generator is available to control the internal DAC reference value for one comparator in the module, which enables peak current mode control in digital power applications. Each comparator output is fed through a programmable digital filter to prevent electrical switching noise from causing spurious trip signals. The output of the CMPSS generates trip signals to the ePWM event trigger submodule and GPIO structure.

The F28004x has up to seven Type 1 CMPSS modules. The Type 1 CMPSS enhancements, over Type 0 found on the F2807x, includes PWM blanking capability to clear-and-reset existing or imminent trip conditions near the EPWM cycle boundaries. Also, the CMPSS comparator positive and negative input signals are independently selectable by using the analog subsystem interconnect scheme. Previously the positive and negative pin input options were tightly coupled on the F2807x between the high and low comparators.

Three independent high-performance ADC modules are available on the F28004x. Each ADC module has a single sample-and-hold circuit and using multiple ADC modules enables simultaneous sampling or independent operation. The ADC module is implemented using a successive approximation type ADC with a resolution of 12-bits and it provides performance of 3.45 MSPS, yielding 10.35 MSPS for the device.

The buffered 12-bit DAC module can be used to provide a programmable reference output voltage and it includes an analog output buffer that is capable of driving an external load. The F28004x has two Type 1 DAC modules. The Type 1 DAC enhancements, over Type 0 found on the F2807x, includes 1x and 2x gain mode options along with increased load support. The pull-down output resistor is removed, and the DAC internal reference supports 2.5 volt and 3.3 volt options.

7 Control Peripherals

The enhanced Pulse Width Modulator (ePWM) module is a fundamental building block for most digital control systems. Power switching devices can be difficult to control when operating in the proportional region, but are easy to control in the saturation and cutoff regions. Since PWM is a digital signal by nature and easy for an MCU to generate, it is ideal for use with power switching devices. Essentially, PWM performs a DAC function, where the duty cycle is equivalent to the DAC analog amplitude value. Both the F28004x and the F2807x use the same Type 4 ePWM modules, however additional lock registers (HRLOCK, GLLOCK, TZCFGLOCK, TZCLRLOCK, and DCLOCK) have been added to the F28004x. Eight ePWM modules are available on the F28004x. The ePWM modules are highly programmable, extremely flexible, and easy to use, while being capable of generating complex pulse width waveforms with minimal CPU overhead or intervention.

The enhanced Capture (eCAP) module is used to accurately time external events by timestamping transitions on the capture input pin. It can be used to measure the speed of a rotating machine, determine the elapsed time between pulses, calculate the period and duty cycle of a pulse train signal, and decode current/voltage measurements derived from duty cycle encoded current/voltage sensors. The F28004x has seven Type 1 eCAP modules. This new eCAP module features high-resolution capture capability which is now an extension to the module, rather than being a separate module. With continuous hardware calibration, complex software intensive based calibration routines are not needed. Each eCAP module has a 128-to-1 multiplexer which is used to select a variety of input signals. External signals are routed first through the Input X-BAR and any GPIO pin can be used as an input. An event filter reset bit is now available which clears the event filter, modulo counter, and any pending interrupt flags (useful for initialization and debug), in addition to a modulo counter status bit for reading the current state of the modulo counter. Also, any one of the four available capture event interrupt triggers can be used as a trigger source for the DMA, and EALLOW protection has been added to eCAP critical registers.

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The enhanced Quadrature Encoder Pulse (eQEP) module interfaces with a linear or rotary incremental encoder for determining position, direction, and speed information from a rotating machine which is typically found in high-performance motion and position-control systems. The F28004x has a new Type 1 eQEP that includes a QEP Mode Adapter (QMA). The QMA evaluates transitions on the external EQEPA and EQEPB signal lines and generates direction and clock signals for supporting industrial drive applications. To use the QMA the eQEP module needs to be configured in the Direction-Count mode. The F28004x has up to two eQEP modules.

The sigma delta filter module (SDFM) is a four-channel digital filter designed to sense analog signals, such as shunt currents and voltages, for digital power and motor control applications. Each channel can receive an independent delta-sigma modulator bit stream which is processed individually by programmable digital decimation filters. The filters include fast comparators for immediate digital threshold comparisons for over-current and under-current monitoring. A key benefit of the SDFM is that its use in a system enables a simple and cost-effective high-voltage isolation boundary. The F28004x has a new Type 1 SDFM which adds 16-deep by 32-bit FIFOs to all data filters, and each data filter has its own data ready peripheral interrupt.

8 Communication Peripherals

The F28004x adds a new Type 0 Power Management Bus (PMBus) and a new Type 0 Fast Serial Interface (FSI). The PMBus module provides an interface for communicating between the MCU and other devices that are compliant with the System Management Interface (SMI) specification. PMBus is an open-standard digital power management protocol that enables communication between components of a power system. The FSI module is a highly reliable high-speed serial communication peripheral capable of operating at dual data rate providing 100 Mbps transfer using a 50 MHz clock. The FSI consists of independent transmitter and receiver cores that are configured and operated independently. FSI is a point-to-point communication protocol operating in a single-master/single-slave configuration. With this high-speed data rate and low channel count, the FSI can be used to increase the amount of information transmitted and reduce the costs to communicate over an isolation barrier.

9 Embedded Real-Time Analysis and Diagnostic

The embedded real-time analysis and diagnostic (ERAD) module extends the debug and system analysis capabilities of the F28004x. A standard C28x CPU includes two analysis units, where the first analysis unit counts events or monitors address buses, and the second analysis unit monitors address and data buses. The two analysis units can be configured for hardware breakpoints or hardware watch points, and additionally the first analysis unit can be configured as a benchmark counter or event counter. The ERAD module is external to the C28x CPU and further expands this capability to provide additional hardware breakpoints, hardware watch points, and counters for profiling, as well as other advanced features.

The F28004x ERAD module contains eight enhanced bus comparator units and four benchmark system event counter units. The bus comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The event counter units are used to analyze and profile the system.

Each bus comparator unit is connected to the CPU and information from the address buses, data buses, and program counter is used as inputs for comparison. The resulting events generated by the bus comparator unit can be used as debug triggers to the CPU, and may be fed to the event counter unit for additional system profiling. The event counter unit can use the output of the bus comparator unit and external system events, such as PIE interrupts, timer interrupts, and CLA task interrupts, for controlling the counter to provide benchmark and profiling analysis. The event counter unit can also generate debug triggers to the CPU.

Typically, the ERAD module is used by the debug software. However, the user application software can also be configured to use the ERAD module. This is especially useful for real-time systems where it is not possible to connect a debug probe for intrusive debug. In this case, the user software can control the ERAD module for non-intrusive debug and profiling of the system.

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10 Summary

The F28004x MCU device family offers a balance of high-performance and cost efficiency. Based on the high-performance TI C28x 32-bit CPU along with its tightly coupled accelerators, advanced control peripherals, and integrated analog functions, the F28004x is extremely capable of solving today's demanding complex real-time control systems and signal processing applications. The enhanced boot modes offer the ability to use alternate, reduce, or completely eliminate boot mode selection pins, while the new analog subsystem interconnect enables a very flexible pin usage for smaller device packages. The other F28004x architectural enhancements discussed in this document were carefully implemented to achieve the goal of optimizing the two key parameters of performance and cost.

Table 1 provides a simplified general feature comparison between the F28004x and the F2807x device families.

Table 1. Device Matrix

	F28004x	F2807x
Clock	100 MHz	120 MHz
FPU	√ (1)	√
TMU	√	√
VCU-I	√	—
CLA	√ (Type 2)	√ (Type 1)
6-Channel DMA	√	√
Flash / RAM	128Kx16 / 50Kx16	256Kx16 / 50Kx16
32-Bit CPU Timers	√	√
Watchdog Timer	√	√
On-Chip Oscillators	√	√
ADC	Three 12-bit	Three 12-bit
CMPSS with DAC	√	√
Buffered DAC	√	√
PGA	√	—
ePWM / HRPWM	√ / √	√ / √
eCAP / HRCAP	√ / √ (Type 1)	√ / — (Type 0)
eQEP	√ (Type 1)	√ (Type 0)
SDFM	√ (Type 1)	√ (Type 0)
DCAN	√	√
I2C	√ (Type 1)	√ (Type 0)
McBSP	—	√
SCI	√	√
SPI	√	√
LIN	√	—
USB	—	√
PMBus	√	—
FSI	√	—
EMIF	—	√
ERAD	√	—

(1) √ Indicates available – check specific device for details

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11 References

For more details, see the F28004x documentation listed below:

- *TMS320F28004x Piccolo Microcontrollers Technical Reference Manual*
- *TMS320F28004x Piccolo™ Microcontrollers Data Manual*

Also, additional information about the C2000 accelerators and F2807x architecture can be found in the following documents:

- *Accelerators: Enhancing the Capabilities of the C2000™ MCU Family*
- *The TMS320F2837xD Architecture: Achieving a New Level of High Performance*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2017) to A Revision **Page**

- Update was made in Section 5. 8
- Added new Section 9. 11
- Update was made to Table 1. 12

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