OMAP5910 Dual-Core Processor Inter-Processor Communication Reference Guide

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Preface

Read This First

About This Manual

This manual describes how the MPU and DSP processors communicate via a mailbox-interrupt mechanism. This mechanism provides a very flexible software protocol between the MPU and DSP processors.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

The following documents describe the OMAP5910 device and related peripherals. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

OMAP5910 Dual-Core Processor MPU Subsystem Reference Guide (literature number SPRU671)

OMAP5910 Dual-Core Processor DSP Subsystem Reference Guide (literature number SPRU672)

OMAP5910 Dual-Core Processor Memory Interface Traffic Controller Reference Guide (literature number SPRU673)

OMAP5910 Dual-Core Processor System DMA Controller Reference Guide (literature number SPRU674)

OMAP5910 Dual-Core Processor LCD Controller Reference Guide (literature number SPRU675)

OMAP5910 Dual-Core Processor Universal Asynchronous Receiver/Transmitter (UART) Devices Reference Guide (literature number SPRU676)

OMAP5910 Dual-Core Processor Universal Serial Bus (USB) and Frame Adjustment Counter (FAC) Reference Guide (literature number SPRU677)

OMAP5910 Dual-Core Processor Clock Generation and System Reset Management Reference Guide (literature number SPRU678)

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OMAP5910 Dual-Core Processor Inter-Processor Communication Reference Guide (literature number SPRU683)

OMAP5910 Dual-Core Processor Camera Interface Reference Guide (literature number SPRU684)

OMAP5910 Dual-Core Processor Multichannel Serial Interface (MCSI) Reference Guide (literature number SPRU685)

OMAP5910 Dual-Core Processor Micro-Wire Interface Reference Guide (literature number SPRU686)

OMAP5910 Dual-Core Processor Real-Time Clock (RTC) Reference Guide (literature number SPRU687)

OMAP5910 Dual-Core Processor HDQ/1-Wire Interface Reference Guide (literature number SPRU688)

OMAP5910 Dual-Core Processor PWL, PWT, and LED Peripheral Reference Guide (literature number SPRU689)

OMAP5910 Dual-Core Processor Multichannel Buffered Serial Port (McBSP) Reference Guide (literature number SPRU708)

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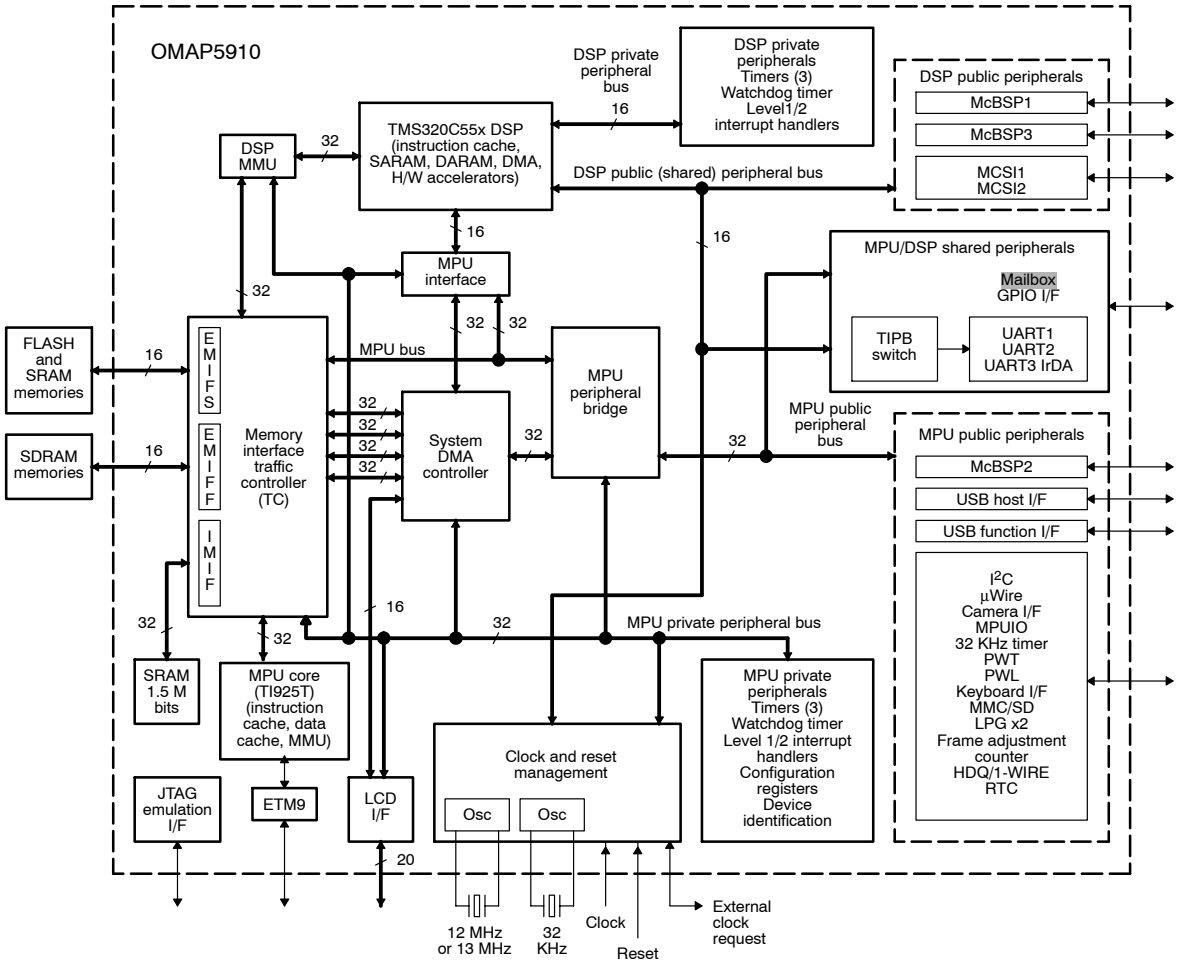
Inter-Processor Communication

1 Introduction

The MPU and DSP processors communicate via a mailbox-interrupt mechanism. This mechanism provides a very flexible software protocol between the MPU and DSP processors. The mailboxes are located in the shared memory space (byte address 0xFFFC:F000 for MPU; word address 0x0F800 for DSP).

Figure 1 shows the location of the mailbox registers at the center right located in the MPU/DSP shared peripherals module.

Figure 1. OMAP5910 Functional Overview

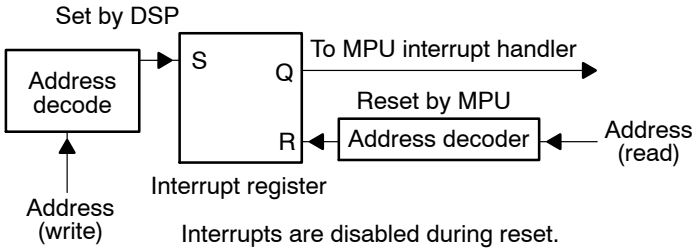


1.1 Mailbox Register Data Structure

There are four sets of mailbox registers: two for the MPU to send messages and issue an interrupt to the DSP, and two for the DSP to send messages and issue an interrupt to the MPU. Each set of mailbox registers consists of two 16-bit registers and a 1-bit flag register. The interrupting processor can use one 16-bit register to pass a data word to the interrupted processor and the other 16-bit register to pass a command word.

Table 1 shows the mailbox registers, and Figure 2 shows the interrupt generating mechanism for a DSP-to-MPU scenario. The mechanism for MPU-to-DSP interrupt generation uses identical hardware.

Figure 2. Interrupt Generating Mechanism-DSP-to-MPU Scenario



The data word from the interrupting processor is user-defined, such as an address pointer or status information.

On writing to the command word register, an interrupt is generated to the other processor and the 1-bit flag register is set. Use of the data word is optional and software controlled, but the data word must always be written before the command field. The ARM2DSP1 and ARM2DSP2 interrupts are registered as INT5 and INT19, respectively, in the DSP. The DSP2ARM1 and DSP2ARM2 interrupts are mapped to the MPU level 1 interrupt handler as IRQ10 and IRQ11, respectively.

The interrupted processor must acknowledge the interrupt by reading the data word (if necessary) and the command word for the associated interrupt. The interrupt is reset and the 1-bit flag register is cleared when the command word is read by the interrupted processor. If software uses the data word, it must always read the data field prior to the command field.

The interrupts that are generated are level-sensitive and writing to the command register of any mailbox generates an interrupt. If the interrupt is masked in the interrupt handler when the command register is written, no interrupt is generated and sent to the processor. However, the command flag for the particular mailbox is set. If the interrupt is unmasked at a later time, an interrupt is generated to the processor. Only the interrupting processor can read the corresponding flag bit (that is, only the MPU can read an ARM2DSP1_FLAG. If polling is used instead of interrupts, the command or data registers must be polled, not the flag register. The flag registers are only useful for the interrupting processor to check if the interrupted processor has responded to the interrupt by reading the command register.

By default, these interrupts are masked by the respective processor interrupt handler and must be unmasked for the mailbox mechanism to be used.

The following software setup procedures are provided as an example.

1) The system software initializes all four of the mailboxes (during powerup or when the system must put the mailboxes in a known state).
2) The system software enables the interrupt in the respective interrupt handler associated with each processor.
3) The interrupting processor writes to the mailbox data location with the data word information when it must alert to the word for the other processor (at this point, the associated word command for the other processor should not have been set yet).
4) The interrupting processor writes to the mailbox command word a predefined command (predefined and understood by both processors). This write issues the interrupt to the other processor.
5) In response to the interrupt, the interrupt handler on the interrupted processor acknowledges the interrupt by reading the mailbox registers. It must read the data first and then read the command register.
6) The interrupt handler calls an interrupt service routine (ISR) which examines the data and command words and processes the work necessary.
7) The interrupt handler returns and the interrupted normal processing continues.

Note:

For the mailbox interrupt procedure, the use of the data word is optional and can be omitted. This eliminates step 3 and the first portion of step 5.

Base Address: 0xFFFC:F000 (byte) for MPU; 0x0F800 (word) for DSP

Table 1. Mailbox Registers

Register	Description	Byte Offset	Reset Value
ARM2DSP1	Data word register for the ARM2DSP1 mailbox. It can be written to only by the MPU. Writing to this register does not generate an interrupt.	0x00	0000
ARM2DSP1b	Command word register for the ARM2DSP1 mailbox. Writing to this register generates the ARM2DSP1 interrupt and sets the ARM2DSP1_Flag. When the DSP reads this register, the interrupt and flag are cleared. It can be written to only by the MPU.	0x04	0000
ARM2DSP2	Data word register for the ARM2DSP2 interrupt. It can be written to only by the MPU. Writing to this register does not generate an interrupt.	0x24	0000
ARM2DSP2b	Command word register for the ARM2DSP2 mailbox. Writing to this register generates the ARM2DSP2 interrupt and sets the ARM2DSP2_Flag. When the DSP reads this register, the interrupt and flag are cleared. It can be written to only by the MPU.	0x28	0000
DSP2ARM1	Data word register for the DSP2ARM1 interrupt. It can be written to only by the DSP. Writing to this register does not generate an interrupt.	0x08	0000
DSP2ARM1b	Command word register for the DSP2ARM1 mailbox. Writing to this register generates the DSP2ARM1 interrupt and sets the DSP2ARM1_Flag. When the MPU reads this register, the interrupt and flag are cleared. It can be written to only by the DSP.	0x0C	0000
DSP2ARM2	Data word register for the DSP2ARM2 interrupt. It can be written to only by the DSP. Writing to this register does not generate an interrupt.	0x10	0000
DSP2ARM2b	Command word register for the DSP2ARM2 mailbox. Writing to this register generates the DSP2ARM2 interrupt and sets the DSP2ARM2_Flag. When the MPU reads this register, the interrupt and flag are cleared. It can be written to only by the DSP.	0x14	0000
ARM2DSP1_Flag	Bit 15-1: Reserved. Bit 0: Flag indicating that the ARM2DSP1 interrupt has been generated. Set by MPU writing to ARM2DSP1b; cleared by DSP reading of ARM2DSP1b. This bit can only be read by the MPU.	0x18	xxxx

Table 1. Mailbox Registers (Continued)

Register	Description	Byte Offset	Reset Value
ARM2DSP2_Flag	Bit 15-1: Reserved. Bit 0: Flag indicating that the ARM2DSP2 interrupt has been generated. Set by MPU writing to ARM2DSP2b; cleared by DSP reading of ARM2DSP2b. This bit can only be read by the MPU.	0x2c	xxxx
DSP2MPU1_Flag	Bit 15-1: Reserved. Bit 0: Flag indicating that the DSP2ARM1 interrupt has been generated. Set by DSP writing to DSP2ARM1b; cleared by MPU reading of DSP2ARM1b. This bit can only be read by the DSP.	0x1C	xxxx
DSP2MPU2_Flag	Bit 15-1: Reserved. Bit 0: Flag indicating that the DSP2ARM2 interrupt has been generated. Set by DSP writing to DSP2ARM2b; cleared by MPU reading of DSP2ARM2b. This bit can only be read by the DSP.	0x20	xxxx

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