TMS320DSC21 – A High Performance, Programmable, Single Chip Digital Signal Processing Solution to Digital Still Cameras

DSC Business Unit
Texas Instruments, Dallas, Texas

This white paper introduces the TMS320DSC21 – a high performance, programmable, single chip Digital Signal Processing (DSP) solution to Digital Still Cameras (DSCs) from Texas Instruments. The paper describes the essential architecture and modes of operations of the current DSCs in the market. It then highlights the architectural aspects of the DSC21 that make it the ideal choice for the DSC engine.

Digital Still Cameras

Digital Imaging - Capturing, Transferring, Manipulating, and Printing photographs digitally came into its own in the early 90's thanks to the foundation laid a decade earlier by desktop publishing. Consumer friendly printers, scanners, and digital cameras began infiltrating the market in 1993. Early versions of Digital Still Cameras (DSC) were expensive, poor in quality and difficult to use.

This scenario has vastly changed in the past few years. Today, dozens of manufacturers produce a variety of compelling offerings. In 1999, the total number of digital camera sold worldwide reached over 6.5 million units. This was attributed to several factors such as the drop in the PC prices, the explosion of the Internet, the ability to transfer and share pictures instantaneously over the Internet, multimedia content rich web pages and the advances in VLSI technology. The market is now expected to grow at a rapid rate in the next few years reaching over 40M units sold in 2005.

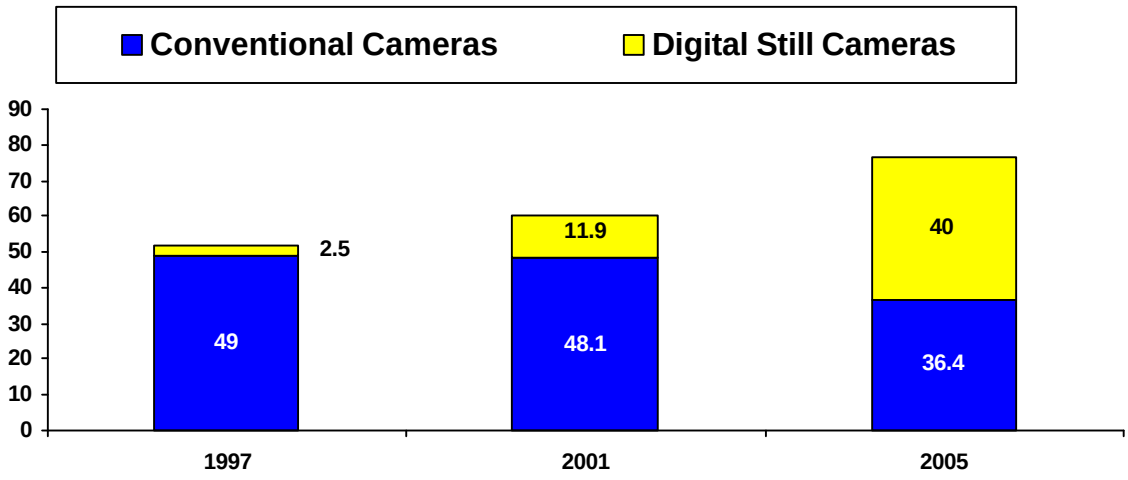

Figure 1 WW DSC shipment forecast in Millions if Units (source: Nikkei Market Access, IDC, Lyra, Data Quest, TI estimates)

Typical DSC System

Digital Still Cameras have a significant amount of silicon content, which includes the sensor (CCD or CMOS), the analog components (ADC, NTSC encoder, DAC etc.) and

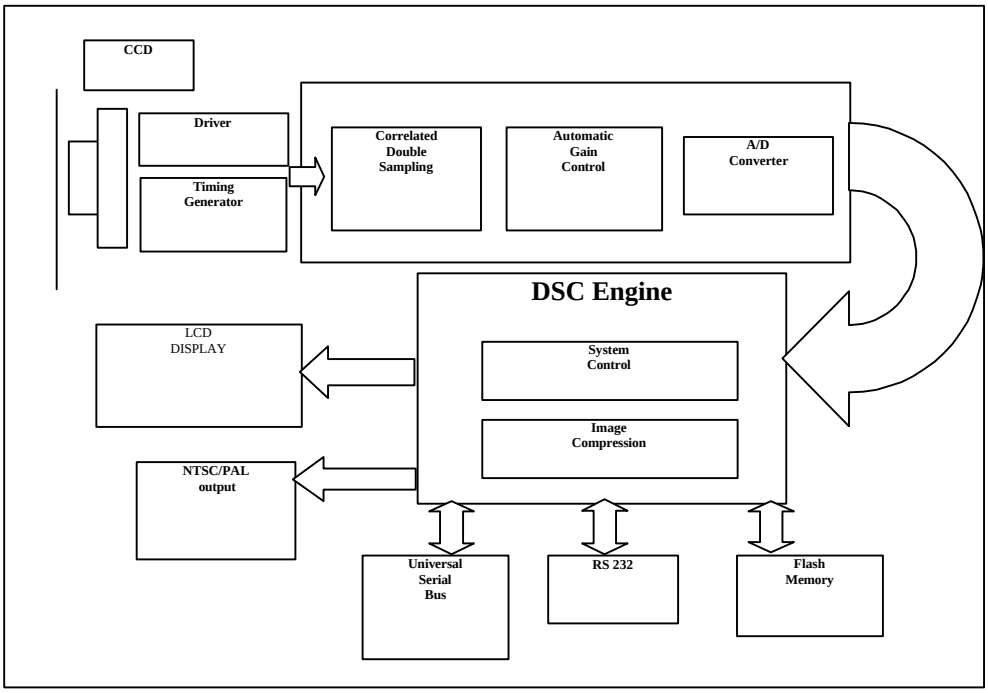

Figure 2 A Typical DSC System

the processing engine. The processing engine is the brain of the camera and responsible of performing all the computation needed to process and compress the image.

Figure 2 shows the various functional blocks in a typical DSC system. Most DSCs use a CCD imager to sense the images. The driver electronics and the Timing Generator circuitry generate the necessary signal to clock the CCD. Correlated Double Sampling and Automatic Gain Control electronics are used to get a good quality image signal from the CCD sensor. This CCD data is then digitized and fed into the DSC Engine. All the image processing and image compression operations are performed in the DSC engine. On most DSCs the user has the ability to view the image to be captured on the LCD display. The captured images are stored on the Flash memory for later use. Most DSC systems also provide an NTSC/PAL video signal to view the captured images (also the preview images) on a TV monitor. The current DSCs also provide a number of ways to connect to the external PC or printer through an RS 232 or a USB port. Future DSC systems are expected to be even more versatile including a modem and TCP/IP interface allows for directly connecting to the Internet.

DSC Modes Of Operation

Typical DSCs have multiple mode of operation. They include:

1. Video Preview
2. Image Capture
3. Image Playback
4. Video/Audio Capture
5. Video/Audio Playback
6. Communication

Preview

Most of the popular DSCs on the market today are equipped with a LCD display in addition to the optical viewfinder. Some DSCs choose to have one or the other. In the Preview Mode of operation, the DSC provides a live video of the scene to be imaged on the LCD viewfinder.

In this mode, the first step is the image acquisition. The intensity distribution reflected from the scene is mapped by an optical system onto the imager. Nowadays, most cameras use CCDs although CMOS imagers are also used in some. The image captured by the CCD sensor has each pixel masked by a color filter to provide a color image. This raw CCD image is normally referred as a Color Filtered Array (CFA). The masking pattern of the CCD array as well as the filter color primaries vary between different manufactures. In DSC applications, the CFA pattern that is most commonly used is an RGB Bayer pattern that consists of 2x2 cell elements, which are tiled across the entire CCD-array. Figure 3 depicts a subset of this Bayer pattern in the matrix block following the CCD camera. The output signal of the CCD is digitized with a 10 or 12-bit A/D converter. This raw data is then processed to produce a good quality video on the LCD screen.

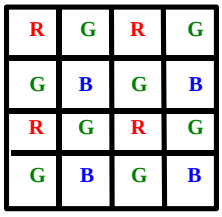

Figure 3 Bayer CFA Pattern

In this mode of operation, typically the CCD/CMOS imager is set in the fast readout mode and the raw image data from the CCD is streamed through the DSC engine, processed, and displayed on the LCD display. The exposure and the color balance values are continuously computed and updated to maintain optimal image quality on the LCD display. Typically the resolution of the LCD displays is much lower than the input CCD resolution. Hence, a high quality of image processing is not required in this preview mode.

Image Capture

One of the key functions the DSC has to perform is to "capture" a high quality digital image of the scene and store it efficiently in compressed form onto the non-volatile storage media such as the compact flash card. A typical DSC has to perform multiple processing steps before a high quality image can be stored.

The CFA data needs to undergo significant amount of image processing before the image can be finally presented in a usable format for compression. All these processing stages are collectively called as the "image pipeline". A typical image pipeline in a DSC is shown in Figure 4. As can be seen, a typical DSC has to perform multiple processing steps before a high quality image can be stored. Most of these tasks are multiply-accumulate (MAC) intensive operations. The DSP subsystem in TMS320DSC21 is well suited to perform these tasks efficiently and generate a high quality image that is close to image quality offered by traditional film from the raw CCD data.

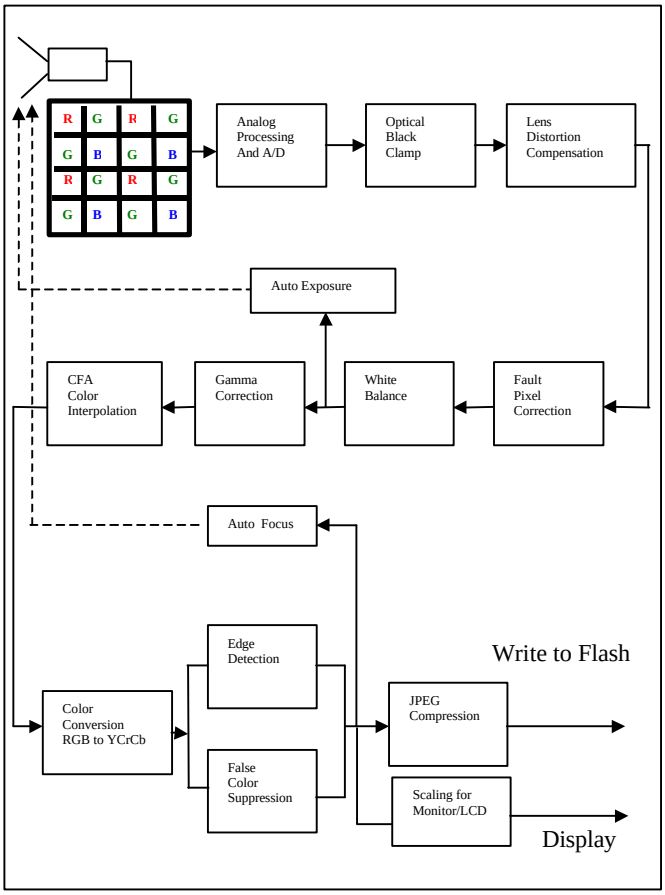

Figure 4 A Typical DSC Image Capture Pipeline

One of the key metrics of the performance of the DSC engine is the shot-to-shot delay. This is defined as the time it takes for the engine to complete processing of one image and become ready to capture the next image**.** A high degree of complexity is involved in producing a high quality digital image in the image pipeline from the raw CCD data, compressing the image, and storing it. Current DSCs mandate a high degree of computational power in the DSC engine to accommodate this complexity in order to provide the user with a low shot-to-shot delay and a pleasant usage experience. The TMS320DSC21 offers a sub 1 second shot-to-shot delay for a 2M pixel imager.

Image Playback

DSCs offer users the convenience of instant review of the stored image on the built in LCD display. This "playback" feature enables the user to quickly select his choice pictures and re-take the unsatisfactory ones. This playback operation involves image decompression, rescaling and formatting the image to fit the LCD display – operations that make extensive use of MAC operations.

Video Capture

Many of the current DSCs also offer the ability for the user to capture short video clips with associated sound. This audio-visual data is then stored in the memory in a format suitable for easy transmission and playback on PCs. Quicktime, AVI, and ASF are some of the popular media file formats used in DSCs. The video coding format is typically MPEG1, MPEG4 or Motion JPEG. Since the DSCs are usually equipped with a single low cost microphone, a simpler speech coding technique is usually sufficient to encode the sound associated with the video clip. G.711 is an example of popular speech coding standard employed in the DSCs. This same speech codec can also be used to annotate the digital images with speech.

A high frame rate and good resolution are two of the metrics used to judge the video capture performance of DSC engines. TMS320DSC21 offers the user a real-time (30 frames/sec at CIF (352 x 288)) video + audio capture. The video formats can be MPEG4, H.263, MPEG1 or Motion JPEG. G.711 is one of the speech coding standards support by TMS320DSC21.

Video Playback

Analogous to the image playback, DSCs provide the user with the ability to playback and review the video clips that are recorded. In this mode of operation, the DSC engine needs to perform the video and audio decompression and scaling to format the video to playback correctly on the LCD screen and the audio to playback though the built-in speaker.

Communication

In addition to the removable storage media such as Compact Flash cards, current DSCs come equipped with a variety of means to communicate and transfer the stored media data to a PC or some other end equipment. USB, IrDA, and Serial Port are some of the popular communication methodologies supported by current DSCs. A higher level communication protocol such as USB, TWAIN drivers, and JetSend need to be running on the DSC to effectively communicate the media data over the physical communication channel.

TMS320DSC21

TMS320DSC21 is designed to effectively support these complex operations in a DSC system. The technical specifications of the DSC21 are :

- TMS320C5000™ DSP and ARM7TDMI RISC processor
- 500 MIPS DSP Subsystem, 0.18 micron technology
- High performance 80 MHz, 32-bit wide SDRAM interface
- Programmable CCD controller, supports CCDs up to 4M pixels (2Kx2K)
- 30 frames/sec, full NTSC/PAL preview (Real-time)
- Both composite and component video outputs - integrated NTSC&PAL encoder and also three separate R,G,B DAC outputs
- Real-time, CIF resolution (352 X 288) video capture in MPEG1, MPEG4, H.263 and Motion JPEG standards
- Quicktime and AVI file media file formats
- Real-time, MP3 audio playback
- Burst Mode Capture (10 images/sec) up to the full resolution of the image sensor
- Supports programmable real-time auto exposure, auto focus, and auto white balance
- Supports CompactFlash™ and SmartMedia™ data storage media
- Supports both interlaced and progressive CCD and CMOS imagers
- Efficient support of real-time operating systems such as Nucleus and microItron
- USB, RS-232, and IrDA communication ports
- 30 user programmable general purpose serial I/Os for peripheral control
- Sub 1 second shot-to-shot delay for 2M pixel CCDs with photo-realistic image quality
- Power Consumption: 260mW Preview, 365mW Capture, 105mW MP3 playback
- 257GHK Microstar BGA package (16x16x1.4mm)

Figure 5 shows the various functional blocks in DSC21.

Functional Block Diagram of the TMS320DSC21

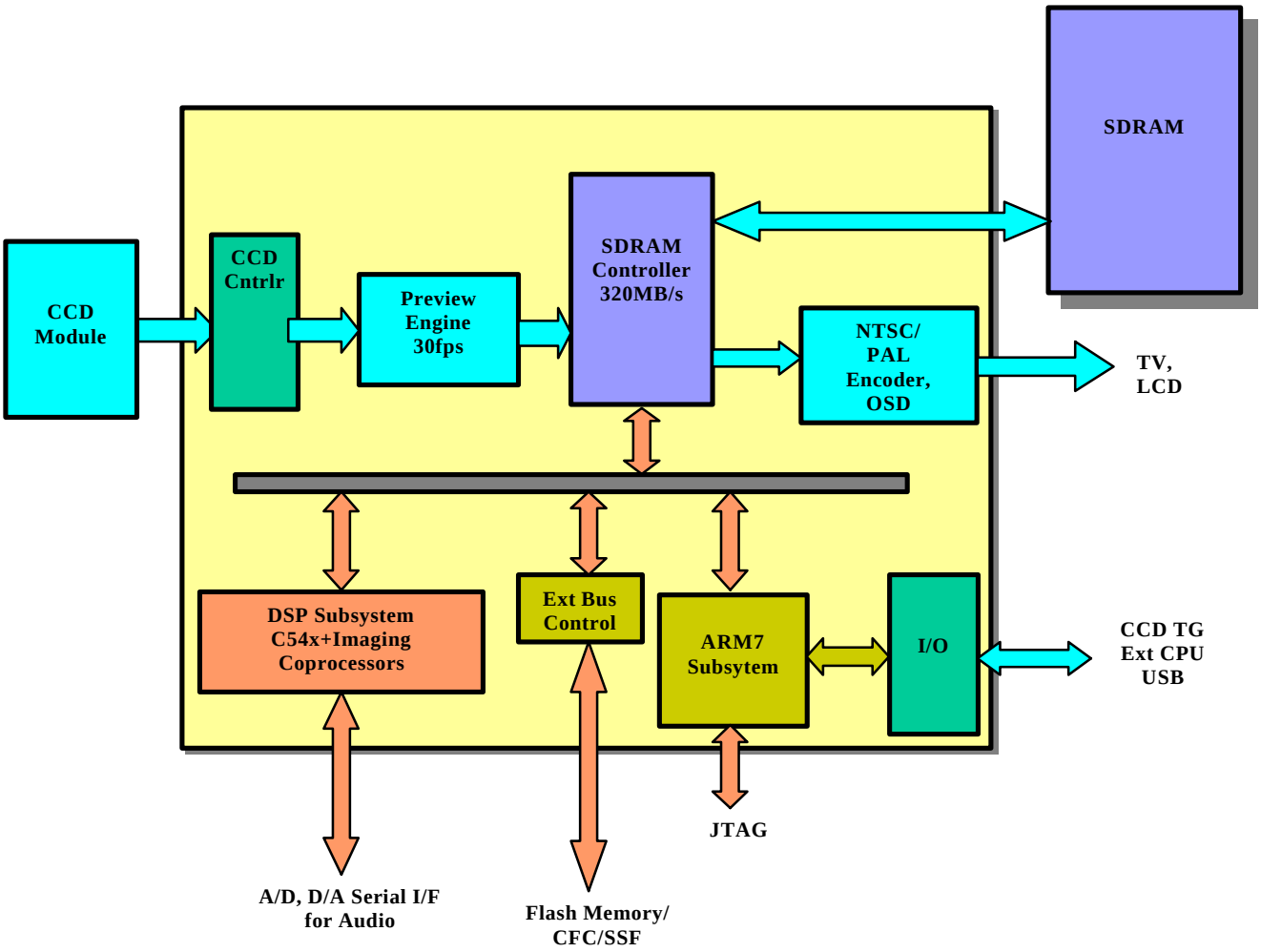

Figure 5 DSC21 System Architecture

DSC21 is a multi-processor system. All the signal and image processing tasks are accomplished by the DSP subsystem. These tasks in a DSC are dominated by multiply-and-accumulate operations (MACs). The architecture of the TI C54x family of DSPs with its single cycle MAC performance is ideally suited for these operations.

The DSC21 DSP subsystem includes the Texas Instruments C54x DSP core. The C54x is a high performance, low power, and market proven, fixed point DSP. The DSP subsystem provides about 500 MIPS of performance. The C54x DSP has 32Kx16-bit of on board SRAM for storing instructions and data. The DSP subsystem carries out auto exposure, auto focus, auto white-balance (AE/AF/AWB), most of the image/video capture and playback tasks that include CFA interpolation, color space conversion,

chroma down-sampling, edge enhancement, color suppression, DCT and IDCT, and Table lookup. Flexibility and ease of programming in the DSP enables camera makers to refine the image processing flow, adjust quality-performance tradeoffs, and introduce additional features to the camera.

The ARM7TDMI processor is a 32-bit microprocessor that is ideally suited for the system resource management, user interface, peripheral drivers and other system control tasks. Having such a multi-processor system with dedicated processors for system control and signal processing, enables DSC21 to provide optimal performance for the complex and intensive image and video processing tasks and at the same time provide a very responsive and system that enables a very compelling end-user experience for this consumer electronics space.

The ARM subsystem performs all the camera system control functions. It supports the in-camera Operating Systems (OS) such as VxWorks, microItron, and Nucleus. ARM also controls the various peripheral modules including the CCD/CMOS controller, burst compression engine, NTSC/PAL encoder, USB, CF, SmartMedia, IrDA, preview engine, and serial ports. The user interface software also runs on this processor.

In addition to these two programmable processing systems, the DSC21 also incorporates a dedicated preview engine. This preview engine enables real-time video processing for excellent quality, real-time (30 frames/sec, at full NTSC/PAL resolution) video for viewing the data before capture and for real-time video capture.

In the DSC21 system the CCD Controller provides the necessary logic to interface either to a CCD or a CMOS imager. The preview engine block converts the data from the CCD controller into a format suitable for displaying real-time 30 fames/sec at full NTSC/PAL resolution on a built-in LCD display or an external TV monitor. It has built-in hardware blocks for gain control, white balance, vertical and horizontal noise filters, CFA Interpolation, down Sampling, Gamma Correction for each of the R,G,B planes and color space conversion. All these hardware blocks in the preview engine are configurable by the ARM processor. The user can adjust the parameters of these hardware blocks to achieve optimal image quality tuned to the specific sensor and the imaging conditions.

The SDRAM controller block acts as the main interface between the SDRAM and all the function blocks such as processors (ARM, DSP), CCD controller, TV encoder, preview engine etc. It supports up to 80MHz SDRAM timing, and provides low-overhead, continuous data accesses. It also has the ability to prioritize the access units to support real-time data streams of CCD data in and TV display data out. The SDRAM controller connects to the external SDRAM via a 32-bit bus that can operate at 80 MHz providing an effective 320 MByte/sec throughput through the system. This high performance, memory access capability enables the DSC21 to support many of the bandwidth intensive video acquisition, processing and display operations at full resolution. The DSC21 is thus able to sustain real-time, full NTSC/PAL resolution CCD data acquisition, display, real-time auto exposure, auto white balance, and auto focus control, MPEG video/audio processing, low shot to delay for high resolution imagers and also concurrently meet the real-time in-camera operating system demands.

The I/O block of the DSC21 system incorporates hardware for communicating to the various external devices including USB, IrDA, Compact Flash, Smart Media, and LCD panel.

Thus the architecture of the DSC21 is ideally suited for the image and video processing requirements of DSC markets. This multi-processor engine achieves, sub 1 second image capture for 2M pixel images at photo-realistic image quality. The engine also supports real-time CIF (352 x 288) resolution video capture and playback in a variety of video compression formats including MPEG1, MPEG4, H.263, and Motion JPEG. It also supports the recording of synchronized speech with the video in G.711 format. This compressed A/V data can be written to the storage media is either Quicktime of AVI formats.

Being a fully programmable solution, DSC21 also supports the playback of compressed audio from the storage media. Real-time decoding and playback of the popular Internet audio formats such as MP3, AAC, WMF can be supported on the C54x DSP embedded in the DSC21. The programmable nature of the DSC21 also allows it to support future compression formats and video codecs.

Summary

In this paper we described the essential architecture and the various modes of operation on the Texas Instruments TMS320DSC21 – a single chip solution for the DSC markets. This high performance, low power, fully programmable, DSP solution enables the camera OEMs differentiate their product offerings by realizing their continuous innovations in image quality and product features. The DSC21 offers over 500 MIPS to fully support the extensive computational requirements of the video, audio and image processing tasks in today's DSCs. The ARM processor embedded in the DSC21 provides excellent performance for all the system control tasks concurrently while the DSP subsystem is performing the MIP intensive signal processing tasks.

This multi-processor, media processing, engine from Texas Instruments is well suited for not only the DSC markets but for the media processing requirements of many other end equipments such as Digital Video Camcorder, Photo printers, Scanners, Video enabled Cell phones and PDAs.

For more information, see: www.ti.com/sc/digitalcamera

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265